

4715

2 | 2.88
1.842
- .6

.842

September 12, 1961

MEMORANDUM TO: 1401 Stage II File
SUBJECT: Clock Control and Delays
Stage II

The following delays can be expected when starting and stopping the 1401 clock for asynchronous operation with I/O devices. The delays will first be given for the clock circuitry alone and then a detailed description of the delays encountered when using the serial I/O attachment circuitry.

	Max.	Min.
1. Clock Control Circuitry on Gate 0183		
a) Clock Control Line on 0183 to turn-on Clock Stop Trigger	.360 usec.	.120 usec.
b) Clock Stop Trigger to 1st Clock Trigger	.842 usec.	.842 usec.
c) 1st Clock Trigger (000-060) to Power Clock Pulse	.110 usec.	.020 usec.
d) 1 Oscillator cycle Delay (just miss turn off of clock stop trigger)	2.885	0.000
e) Oscillator Variation (+1% of Band-D)	-0.037	-0.008
f) Total Delay from presence of Clock Control Signal Line on 0183 to the 000-030 Clock Pulse on 0183	4.234 usec.	0.974 usec.

1.998
~~910~~
 - .842

 3.750
 2.885

 5.725

1.628
 - .842

 .786
 5.415

11. Total delay from the time a service request line is received at the Serial I/O terminator until the service response line is present at the output of the Serial I/O line driver.

		Max.	Min.
a) I/O Terminator to Clock Control	.99 + <i>Driver Terminator = cable</i>	1.200 1.33	0.500
b) Clock Control to Clock Stop Trigger		.0.360 1.49	0.120
c) Clock Stop Trigger to Turn of 1st Clock Trigger	<i>least</i>	0.842	0.842
d) 1 Oscillator Cycle Delay (just miss turn off at clock stop trigger)		2.885	0.000
e) 1st Clock Trigger to Power Clock Pulse		0.110	0.020
f) Power Clock Pulse (075 time) to output of I/O Line Driver	<i>(service response)</i>	0.860	0.590
g) Oscillator Variation ($\pm 1\%$ of C, D, H)		0.109	-0.080
h) 075 time (service response) related to 11.54 usec. cycle		7.212	7.212
i) Total Input Terminator 1401 to Output of Line Driver		13.578	9.204

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13.9

from time to clock - 2.402
5.397
2.402
5.397
.860
9
2.985
.842
.360
5.90
2.402
2.992