1401 PROCESS OVERLAP

General Description

The overlap optional feature will be designed so that processing can continue at the same time that the 1401 is executing any one of the following operations:

1. Reading from the 1402
2. Punching out on the 1402
3. Reading and Punching on the 1402
4. Reading or Writing on Magnetic Tape
5. Reading or Writing on the I/O Adapter Channel at a rate that does not exceed 25 KC.

The degree of overlapping will depend upon the particular device and the type of operation that is being performed. This feature is being designed so that it is compatible with the present 1401 programs as well as with the 1410. An "Overlap" type program, which utilizes only the 1402 being overlapped with processing, will run on a 1401 which does not have the overlap optional feature. The time required to run such a program will, of course, be longer than on a machine with the Overlap Optional Feature. In addition, the cards in the 1402 may not select correctly into the stackers if the processing time required between the feed instruction and the stacker select instruction exceeds 10 MS.

In any overlap operation, information is passed from input-output to 1401 storage by turning off the delta process latch, thus interrupting normal processing, and activating storage through special overlap controls. The address of the storage location being entered by I/O is gated from an additional STAR called the overlap storage address register, or 0-STAR, into the address register at the end of the process cycle prior to an overlap cycle. This address may be modified by -1, +1, or zero, and gated back into the 0-STAR in the normal manner. During the latter part of the overlap cycle immediately preceeding a process cycle, the delta process latch is set, and the proper address for the next sequential process cycle is gated from its respective star into the address register.

The instructions are as follows:

M (%XX) (BBB) R L W	Normal Tape or I/O instruction
M (@XX) (BBB) R L W	Overlap Tape or I/O instruction
K $	Execute all of the following Reader and/or Punch operation codes in an overlap mode until reset by the K• operation code or the load key.
K (AAA) $	Execute all of the following Reader and/or Punch operation codes in an overlap mode until reset by the K• operation code or the load key, and branch to address (AAA).
K•	Reset the overlap mode and the overlap test mode latches and execute all of the following Reader and/or Punch operation codes in their normal mode.
K (AAA)•	Reset the overlap mode and the overlap test mode latches and execute all of the following Reader and/or Punch operation codes in their normal mode, and branch to address (AAA).
K)ddBBB	Set Program Activity Recording mode for use by the Customer Engineer.
B (AAA) H	Branch on Reader Busy. Branch to address (AAA) if the 1402 reader is busy; otherwise, go to the next instruction.
B (AAA) I	Branch on Punch Busy. Branch to address (AAA) if the 1402 punch is busy; otherwise, go to the next instruction.
B (AAA) J	Branch on Tape or I/O Adapter Busy. Branch to address (AAA) if the Magnetic Tape Unit or any device attached to the I/O Adapter channel is busy; otherwise, go to the next instruction in sequence and at the same time

B (AAA) J contd. reset the B-STAR on a non-index machine. If the machine contains the index optional feature, the B-STAR is reset, and the address in the O-STAR is transferred to the B-STAR.

A number of rules apply when the 1401 is executing instructions in an Overlap Mode.

I. In general, no other "Input/Output" operation will be able to start until the preceding overlapped operation is completed. The 1401 will interlock and prevent further operation until the operation is completed. The exceptions to this rule are listed in some of the paragraphs below.

II. A one-character arithmetic operation should not be executed while an input/output device is operating in the Overlap Mode. Nothing will prevent such an instruction from being executed; however, this instruction can cause an input/output transmission error since this instruction might not allow an overlap cycle to be taken for a number of cycles as it can hold up the readdress line for more than one cycle in sequence under recomplement conditions.

III. If the 1401 contains the Print Storage optional feature, any of the following print instructions can be executed when any overlap operation is in progress:

A. 2 Print

B. 2 (AAA) Print and Branch

C. 2 ⌑ Print Word Marks

D. 2 (AAA) ⌑ Print Word Marks and Branch

IV. Certain 1402 read and punch instructions can be overlapped at the same time.

A. When executing a normal read instruction in the Overlap Mode (not including IC-Read Column Binary or 1O - Read Bill Feed), the following input/output operations can be executed at the same time without the 1401 interlocking and holding up the operation:

IV. A. contd.

1. 4 Punch

2. 4 (AAA) Punch and Branch

3. If the 1401 contains the Print Storage optional feature, the following instructions:

   a. 6 Print and Punch

   b. 6 (AAA) Print, Punch, and Branch

   c. 6 ¤ Print WM and Punch

   d. 6 (AAA)¤ Print WM, Punch, and Branch

B. When executing a normal punch instruction in the Overlap Mode (not including 4C-Column Binary or 4R Punch Feed Read), the following input/output operations can be executed at the same time without the 1401 interlocking and holding up the operation:

1. 1 Read

2. 1 (AAA) Read and Branch

3. If the 1401 contains the Print Storage optional feature, the following instructions:

   a. 3 Print and Read

   b. 3 (AAA) Print, Read, and Branch

   c. 3 ¤ Print WM and Read

   d. 3 (AAA)¤ Print WM, Read, and Branch

V. The 1401 will interlock when executing certain instructions until certain conditions are met before continuing the operation. When executing an overlap operation, the following instructions are affected:

V. contd.

A. B (AAA) ?

Branch on Reader Check
If the reader is operating when this instruction is given, the 1401 will interlock before making the test until the card has been read, and then it will test for the reader error.

B. B (AAA) !

Branch on Punch Check
If the punch is operating when this instruction is given, the 1401 will interlock before making the test until the card has been punched, and then it will test for the error.

C. B (AAA) L

Branch on Tape Check
If the Tape Adapter Unit (TAU) is busy when this instruction is given, the 1401 will interlock before making the test until the TAU is no longer busy, and then it will test for the tape error.

D. B (AAA) 1

Branch on I/O Adapter Check
If the Input/Output device attached to the I/O Adapter is busy when this instruction is given, the 1401 will interlock before making the test until the I/O unit is no longer busy, and then it will test for the I/O error.

E. B (AAA) H

Branch on Reader Busy
If the reader is busy when this instruction is given and the interlock stop condition is on in the 1402, the 1401 will hang up in this instruction until the condition is corrected. This condition will occur if:

1. a jam occurs in the 1402 read or punch feed;
2. 1402 stacker becomes full;
3. 1402 hopper becomes empty;

E. B (AAA) H contd.

4. the I/O stop switch is on and one or more of the following occur:

a. Read Check

b. Validity Check

c. Punch Check

F. B (AAA) I Branch on Punch Busy
If the reader is busy when this instruction is given and the interlock stop condition is on in the 1402, the 1401 will hang up in this instruction until the condition is corrected. This condition will occur if:

1. a jam occurs in the 1402 read or punch feed;

2. 1402 stacker becomes full;

3. 1402 hopper becomes empty;

4. the I/O stop switch is on and one or more of the following occur:

a. Read Check

b. Validity Check

c. Punch Check

VI. A number of check stop conditions will exist as described below:

A. When a Storage Address Error occurs, the processing unit will stop immediately.

B. When in an overlap read operation, it is a programming error if a process instruction addresses storage locations 000 through 080. There is no checking for this type of error, but a read check may result. When in an overlap read operation, the programmer should never address storage locations 000 through 080 in a normal read, or storage locations 000 through 080,

VI. B. contd.

401 through 480, or 501 through 580 in a column binary read operation until after he has tested for Reader busy B (AAA) H and if not busy, then proceed to utilize these locations.

C. When in an overlap punch operation, it is a programming error if a process instruction addresses storage locations 100 through 180 when in a normal punch operation or locations 000 through 080 and 100 through 180 when in a Punch Feed Read operation. There is no checking for this type of error, but a punch check may result. When in an overlap punch operation the programmer should never address the following storage locations:

1. 100 through 180 in a normal punch operation

2. 000 through 080
   100 through 180 in a Punch Feed Read operation

3. 100 through 180
   401 through 480 in a Column Binary Punch operation
   501 through 580

until after he has tested for Punch busy B (AAA) I, and if not busy then proceed to utilize these locations.

D. If in the 1402 an interlock stop occurs after an overlap operation has been completed, the 1401 will stop before executing the next Read or Punch instruction, or at the end of reading a B (AAA) H or B (AAA) I instruction.

E. If a hole count or validity error occurs and the I/O check stop switch is on, the overlap operation will continue until the feed or punch operation is completed, and then it will stop. The processing will continue until the end of the overlap operation, and then it will stop at the end of execution of the particular instruction that it is executing unless a B (AAA) H or B (AAA) I instruction has been encountered, and then the 1401 hangs up in that instruction as explained previously.

F. When reading from tape or the I/O Adapter channel, any character with an incorrect parity will set a transmission error latch. This latch can be reset by the tape unit or the I/O device. If this latch has not been reset at the end of the overlap operation, processing will stop at the completion of the current instruction, with an overlap error indication, but no process error indication.

VI. G. If a process error occurs during an actual overlap cycle, processing will stop immediately; however, the overlap operation will continue to its normal end, and then it will stop with the overlap and process error lights on, indicating that the process error occurred in the I/O operation.

H. When a process error occurs between overlap cycles, processing stops immediately, and the I/O operation continues but the I/O record may be incorrect if the inhibit error light is on and you are in a load type of I/O operation. If in a move type of I/O operation and a B register or inhibit error occurs, the I/O record may be incorrect. If in a read-punch overlap operation and any process error indication is given, the card may have been read or punched incorrectly. The error in this case is an actual process error, but this condition effectively masks a similar overlap error if one should occur.

VII. When the 1401 is operating in an overlap operation, the following operational codes will be inoperative:

8 Read Release
9 Punch Release

VIII. Overlap cycles may be taken immediately after any process cycle with these exceptions:

A. Any cycle where Readdressing occurs.

B. The dummy cycle that occurs after the all scans complete cycle on a print transfer.

When these conditions occur, overlap cycles will be held up one additional process cycle.

Reading Tape or I/O Channel

Information read from magnetic tape or the I/O channel uses the A register as its path to 1401 storage. Since useful process information may be contained in the A register, this data is gated into another register, called the O register, where it is stored until the beginning of the next process cycle. At that time it is gated back into the A register.

The storage address at which the overlap read operation will begin is gated into the B STAR during I ring 4, 5 and 6 of the instruction cycles. The first execution cycle is a "dummy" B cycle during which the address in the address register is modified by zero and read into the O STAR. The O STAR addresses storage during all other "overlap read" execution cycles.

In single cycle or I/E mode, the start key should not be depressed while the I/O device is in motion, as this may cause overlap and/or process errors.

If a "read" operation is performed in non-overlap mode, the operation is executed exactly as though overlap were not on the machine.

Writing on Tape or I/O Channel

Information being written on magnetic tape, or the I/O channel enters the B register from storage, passes through the O register, and into the I/O device. The O register is not reset until another overlap cycle is taken.

The storage address at which the overlap read operation will begin is gated into the B STAR during I ring 4, 5 and 6 of the instruction cycles. The first execution cycle is a B cycle during which the address in the address register is modified by +1 or -1, and read into the O STAR. During this cycle, the first character of the record is written into the I/O device. The O STAR addresses storage during all other overlap cycles.

In single cycle or I/E mode, the start key should not be depressed while the I/O device is in motion as this may cause overlap and/or process errors.

A "write" operation performed in non-overlap mode is executed as though the overlap option were not on the machine, except that the information being written will pass through the O register.

Reading or Punching Cards from the 1402

If the 1402 is reading cards in overlap mode, processing may occur at any time during the card cycle that data is not being read from the row bit cores into storage; that is, processing may not occur during read scans. Similarly, processing may not occur during punch scans.

At the beginning of a read or punch scan, in both overlap and non-overlap mode, the character in the A register is transferred to the O register, and the O STAR is set to address 0000. The O STAR then controls addressing throughout the read or punch scan. At the completion of the scan, the information in the O register is transferred back into the A register. If the read or punch operation is being done in overlap mode, processing will resume at this time.

set to 000 on read scans and 100 on punch scans

Program Activity Recording

The Program Activity Recording (PAR) feature is a Customer Engineering feature designed to record, in any specified area of 1401 storage, the program activity occurring in the 1401 during each process cycle.

The instruction of the operation whose data is to be recorded must be preceded by a KddBBB instruction. The PAR controls allow the BBB address to be read into the O STAR during I cycles. This address will designate the low order storage address of any data to be recorded. An overlap cycle is forced, following each process cycle, providing that a readdress cycle did not occur. The O STAR then addresses storage, but the information located in storage at that address is not read out. None of the basic character registers or address registers are altered during this cycle. If the previous cycle was an A cycle, the character in the A register is now read into storage. In any other case, the information in the B register is transferred into storage. The delta process latch is then set and the program proceeds with the next sequential process cycle.

Hardware Required for Process Overlap - Pre-Process Overlap

The additional hardware necessary for the process overlap feature is as follows:

1. One completely new chassis - 02B1
2. Approximately thirty additional signal cables.
3. Push button on console for displaying O STAR.
4. Indicator on console for display of overlap errors.

Along with this additional circuitry, modifications were necessary to other areas of the 1401 preparatory to installation of the process overlap feature. Most of these changes were not extensive, logic-wise, but due to rearrangement of present circuits, and the addition of overlap circuitry, the number of wires changed and SMS card locations changed is significant. Thus, it was necessary to repackage chassis 01B2, 01B4, 01B6, 02B6, and 02B8. Most other chassis were affected, but to a lesser degree.

The only change preparatory to process overlap (pre-process overlap) which causes an alteration in 1401 cycling concerns a recomplement add

operation. One readdress cycle has been eliminated from this operation. Prior to process overlap, a readdress cycle was taken at the completion of the reverse scan preparatory to the beginning of the second forward scan. A second readdress cycle was then taken to read into the A register and force a zero into storage preparatory to a complement add cycle. The effects of these two cycles have been combined so that on a "pre-process overlap" 1401, only one readdress cycle is necessary.

Circuit Description

1. R-P Overlap Mode Latch 74.21.01.2

When this latch is on, all reader-punch operations are performed in overlap mode. The latch is set if a dollar sign ($) is decoded in the A register while a word mark is in the B register during a K operation. It is reset if a period (.) is decoded in the A register at gated word mark time of a K operation. Note that although a K operation code is used, the 1401 does not attempt a stacker select operation because of the zone bits in the two "d" modifiers.

When power is turned on, this latch is held off. Start reset does not reset the latch.

2. Tape or I/O Mode Latch 74.21.01.2

When this latch is on, all tape or I/O devices on the system will operate in overlap mode. It is set whenever an at symbol (@) is decoded at I ring 1 time if there is no U op or No Op, and there is no word mark in the B register. It is reset when the transmission of the record is completed. Also, a storage address error, depressing the start reset key, or moving the tape mode switch to diagnostic will reset the latch.

3. Delta Overlap Cycle Latch 74.31.21.2

This latch controls the interruption of processing, and allows overlap cycles to be taken. It is set at 060 time of every clock cycle during a read or punch scan, unless the last address of the scan has been detected. It is also set at 060 time if the 1401 is in I/O or tape overlap mode, and any of the following conditions are met.

a. R-W trigger is on, and there is no forced group mark. The read-write trigger indicates that the magnetic tape is ready to accept or release a character. "Not forced group mark" indicates that there was no group mark-word mark in the storage location being addressed during a write call.

b. I-O service request trigger, and there is no forced group mark. Similar to (a) except that here, the I/O channel is in operation.

c. Force Delta Overlap Cycle (see #20)

d. Tape Readdress Latch forces an overlap cycle during which the O STAR is restored to the address at which a word separator was sensed on tape during a "load read" operation or a word mark was sensed in 1401 storage during a "load write" operation (see # 23)

e. Forced Group Mark and not overlap cycle indicates that the end of a record is sensed during a "read" operation. An overlap cycle is necessary to set the group mark into 1401 storage.

The delta-overlap latch is also held on during read or punch scans, until the end of the scan (last address) is reached. It is also set after each delta process cycle by the PAR controls.

This latch is reset at 045 time of the following cycle. It is also held reset during a readdress cycle, and during the dummy cycle which concludes the print buffer transfer.

4. Overlap Cycle Latch 74.31.21.2

This latch is set at 000 time if the delta overlap latch is on, and remains on for one clock cycle. It is a control latch to indicate that processing is stopped and overlap information is being transmitted.

5. Activate Memory Latch 74.31.21.2

This latch controls entry of 1401 storage, and the O STAR. It is turned on at 090 of a delta overlap cycle, and reset at 105 of the following cycle. It is also on during the single delta B cycle of a tape overlap operation to allow gating into the O STAR at this time.

6. Delta Process Control Latch 74.31.31.2

This latch allows delta process to be turned on following a delta overlap cycle, if the delta process latch had been reset by overlap controls. It is set if delta process is on, and reset if delta process is turned off by non-overlap controls.

7. Overlap Star Read-In

74.11.11.2

The overlap star may be entered during I ring 4, 5 and 6 of a PAR instruction. It may also be entered while the overlap activate memory latch is on.

8. Overlap Star Gate-Out

74.11.31.2

The O STAR is read into the address register at gate time (090-000) of every delta overlap cycle, providing no tape readdress is occurring, and there is no reader-punch set up condition. Also, any unsuccessful branch on tape or I/O busy will allow the overlap star to be read into the address register. (see #18). Depressing the O STAR key also gates out the O STAR.

9. A Register to O Register Gate-In

74.11.71.2

Data from the A register is allowed to enter the O register at 090-000 time during the first of any series of delta overlap cycles if the overlap write latch (see #12) is not on. During a write operation, data passes from the B register into the O register.

10. Not O Register Reset

74.11.71.2

The O register is reset at 075-105 time during the first of any series of delta overlap cycles if the overlap write latch is not on. It is also reset at 030-060 of any write tape on write I/O cycle, unless a tape readdress condition is taking place. In this case, the word separator in the O register is not allowed to reset.

A manual tape operation also holds the O register reset.

11. O to A Latch

74.11.71.2

This latch is set at 090-000 time of the last of a series of overlap cycles, if there is no write condition. At the beginning of the following process cycle, the A register is reset, and the O register character is gated into it. The latch is then reset, at 030-060 time.

12. Write Latch 74.11.71.2

This latch is set by a "write call", which means W character is in the A register at the end of a tape instruction. It is reset when the tape or I/O mode latch is off. (see # 2)

13. Overlap Busy 74.21.11.2

Overlap is busy if the tape or I/O overlap mode latch is on or if read or punch scans are not completed.

14. Overlap Scans Complete 74.21.11.2

The overlap all scans complete trigger is set at the completion of the overlap cycle during which a group mark is forced or when all read and punch scans are completed. It is reset at ØØØ time of the next clock cycle or by depressing the start reset key.

15. Overlap Load Opr 74.41.11.2

It is necessary that the 1401 "remembers" whether a tape or I/O overlap instruction has been given in the form of a load operation, since the data in the op register will be changing during the overlap execution. Thus a load tape instruction in overlap mode sets a latch, part of which is on 02B1 and part of which is on 02A2. The latch is reset when the tape or I/O mode latch is reset.

16. Branch on Reader Busy 74.21.41.2

If an H is sensed in the A register during I ring 5 of a Branch Operation, and a word mark is in the B register, the program skip latch will be set if read scans are not completed.

17. Branch on Punch Busy 74.21.41.2

If an I is sensed in the A register during I ring 5 of a Branch Operation, and a word mark is in the B register, the program skip latch will be set if punch scans are not completed.

18. Branch on Tape or I/O Overlap Busy 74.21.31.2

If a J is sensed in the A register during I ring 5 of a Branch Operation, and a word mark is in the B register, the program skip latch will be set if the tape or I/O overlap mode latch is on. If the tape or I/O overlap mode latch is not on, and the system contains the advanced programming feature, the I-B star trigger is set, gate out of the I STAR is prevented, and the contents of the O STAR is gated into the address register. Thus, the address in the O STAR is transferred to the B STAR.

19. Overlap Error Latch and Overlap Error Trigger 74.21.21.2

The overlap error latch is set if an A register check occurs during an overlap cycle. It is reset if the check was due to a tape or I/O error. This latch is necessary, since the A register check latch set signal is blocked during overlap cycles.

The overlap error trigger is set if a process check occurs during an overlap cycle if no previous process check had occurred. It is reset by depressing the check reset key.

If either the latch or trigger is on, and the process check stop switch is on, the stop latch will be set when overlap is no longer busy. This will cause processing to stop at the completion of the current instruction.

20. Force Delta Overlap Cycle 02A1

When reading or writing in high density, only the start time of the 729 tape drives may be used as 1401 process time. At the end of this start time (either end read delay or write delay 49 is reached) a latch is set which forces delta overlap cycles. This latch is reset when the 1401 is no longer in overlap mode.

When reading in high density on a 7330 tape drive, or when reading in low density on a 729 Model IV tape drive, it is necessary, because of the high speed of the device, to "pre-sense" when the tape unit is ready to deliver a character. In either case, a delta overlap cycle is forced when read clock 4 (in the tape adapter unit) is sensed. Approximately ten micro-seconds will elapse from the time the read clock 4 trigger is set until the character on tape enters the read-write register. Thus, if read clock 4 is sensed between Ø2Ø and Ø6Ø time of the 1401 cycle, the character will not be in the read-write register at ØØØ time, when the overlap cycle should begin. For this reason, the 1401 clock is stopped

until the read-write register is entered, at which time the clock is restarted. Under these conditions, the clock will be stopped approximately every fourth overlap cycle.

21. Delta Par Latch 74.11.81.2

This latch controls gating into the O STAR during I cycles of a "Program Activity Recording" operation. It is set if a comma (,) is detected in the A register at I ring 1 time of a "K" operation. It is reset when the "K" is reset out of the op register.

22. Par Latch 74.11.81.2

This latch controls the addressing of storage by the O STAR on an alternate cycle basis. It is set at I ring 7 time if the delta par latch is on. It is reset if a period is in the A register at gated word mark time of a K operation, or if the load latch is on.

An overlap cycle is requested if the par latch is on at Ø6Ø time of a non-overlap cycle. Storage read-out is blocked during a PAR overlap cycle by blocking the strobe pulse to storage. The reset of the B register is also blocked so that the character in the B register is not destroyed. If the A cycle latch is on, transfer A register is activated during the overlap cycle. Otherwise, the B register data is transferred into the storage location addressed by the O STAR.

23. Word Separator Control Latch 74.41.11.2

The purpose of this latch, along with the readdress latch and the readdress control latch, is to allow processing to continue between the time the word separator is written on or read from tape or I/O and the time that the character associated with the word separator is written on or read from tape or I/O.

If a write tape or I/O operation is performed in "overlap load" mode, the readdress latch (02A2) is set during the overlap cycle in which a B register word mark is sensed, and a word separator is set into the O register during the same cycle. The word separator control latch is also set during this cycle, a delta overlap cycle is forced, and the reset of the address register is blocked. The readdress control latch is set at the beginning of the next cycle, and the address in the address register is transferred into the O STAR. Processing now resumes until the tape

is ready to accept the character associated with the word mark. At this time a delta overlap cycle is taken, and the word separator control latch is reset. During the following cycle, the readdress latch is reset, and this allows the character associated with the word mark to enter the O register. The readdress control latch is reset at the completion of this cycle.

These controls work in a similar manner if a read tape or I/O operation is performed in "overlap load" mode. During the first overlap cycle, the word separator is read from tape. A second overlap cycle is then taken to restore the O STAR.

Processing then takes place until the next character from tape is ready to be read into storage. Another overlap cycle is taken at this time, and a word mark is inhibited along with the data character.

24. Overlap Process Interlock Latch 74.31.41.2

Under certain conditions (such as an overlap operation being called for while overlap is busy) processing is interlocked until the overlap operation is completed. When these conditions arise, the delta process latch is reset, and the overlap process interlock latch is set. Delta process is turned back on at Ø6Ø time of the cycle during which all overlap scans are completed if the overlap process interlock latch is on, the 1401 is in run mode, the stop latch is not on, and there is no process stop condition.

The overlap process interlock latch is set under any of the following conditions:

a. A gated word word mark is sensed during an I cycle with a 1 or 4 in the op register while overlap is busy and any of these conditions are met:

   1. I ring 2 or I ring 5 - Blocks a Bill Feed, Column Binary, or Punch Feed Read operation from progressing into its execution phase.

   2. Bill Feed Op Latch - Blocks a reader or punch operation from progressing while a Bill Feed operation is being run in overlap mode.

3. Column Binary Op Latch - Blocks a reader or punch operation from progressing while a Column Binary operation is being run in overlap mode.

4. PFR Op Trigger - Blocks a reader or punch operation from progressing while a Punch Feed Read operation is being run in overlap mode.

5. T or I/O Overlap Mode - Blocks a reader or punch operation from progressing while a tape or I/O channel operation is being run in overlap mode.

6. Not Punch Complete and Punch Op - Blocks a punch operation from progressing while a punch operation is already running in overlap mode.

7. Not Read Complete and Read Op - Blocks a read operation from progressing while a read operation is running in overlap mode.

b. A gated word mark is sensed during an I cycle of a non-buffered print instruction while overlap is busy.

c. A % or @ is sensed at I ring 1 time while overlap is busy.

d. A branch on reader error instruction is given before read scans are completed.

e. A branch on punch error instruction is given before punch scans are completed.

The overlap process interlock latch is reset when all overlap scans are completed or the start reset key is depressed.

25. Overlap Read Punch Interlock 74.31.51.2

This trigger controls the resetting of the read complete and punch complete triggers.

It is set when the gated word mark is reached during a read or punch instruction, if there is no print operation, overlap is not busy, and the 1401 is not in read-punch overlap mode. In the case of a 3, 5 or 7 operation, the trigger is set when print scan end is reached if the 1401 is not in read-punch overlap mode.

If the trigger is on, the read complete trigger will be reset at gated word mark time of a read operation during the process cycle in which the word mark is sensed. If the trigger is not on, the read complete trigger will be reset at gated word mark time of a read operation during the next delta process cycle. Thus, if the delta process latch had been reset by the overlap process interlock controls, the read complete trigger will not be reset until all overlap scans are completed.

The punch complete trigger is reset in a similar manner.

This interlock trigger is reset when all overlap scans are complete, or when the start reset key is depressed.

26. Overlap Interlock Stop Controls 74.31.61.2

If a reader interlock occurs (stacker full, hopper empty, etc.) between the time the feed op is given and the time the clutch actually picks, it is desirable to stop processing, since the card being fed will not actually be read into 1401 storage. However, if the interlock condition occurs after the clutch is picked, processing should continue, since the card will actually be read into storage.

The overlap interlock stop controls are "ored" with the output of the stop latch and prevent processing from progressing under the conditions described above. The "Remember Read Feed" latch is on from the time the read feed trigger is set until the first reader impulse is received after the read stacker reset cam is made. This latch blocks an interlock process stop from occurring during the first part of the card cycle, while the read stacker reset cam blocks an interlock process stop during the latter part of the cycle.

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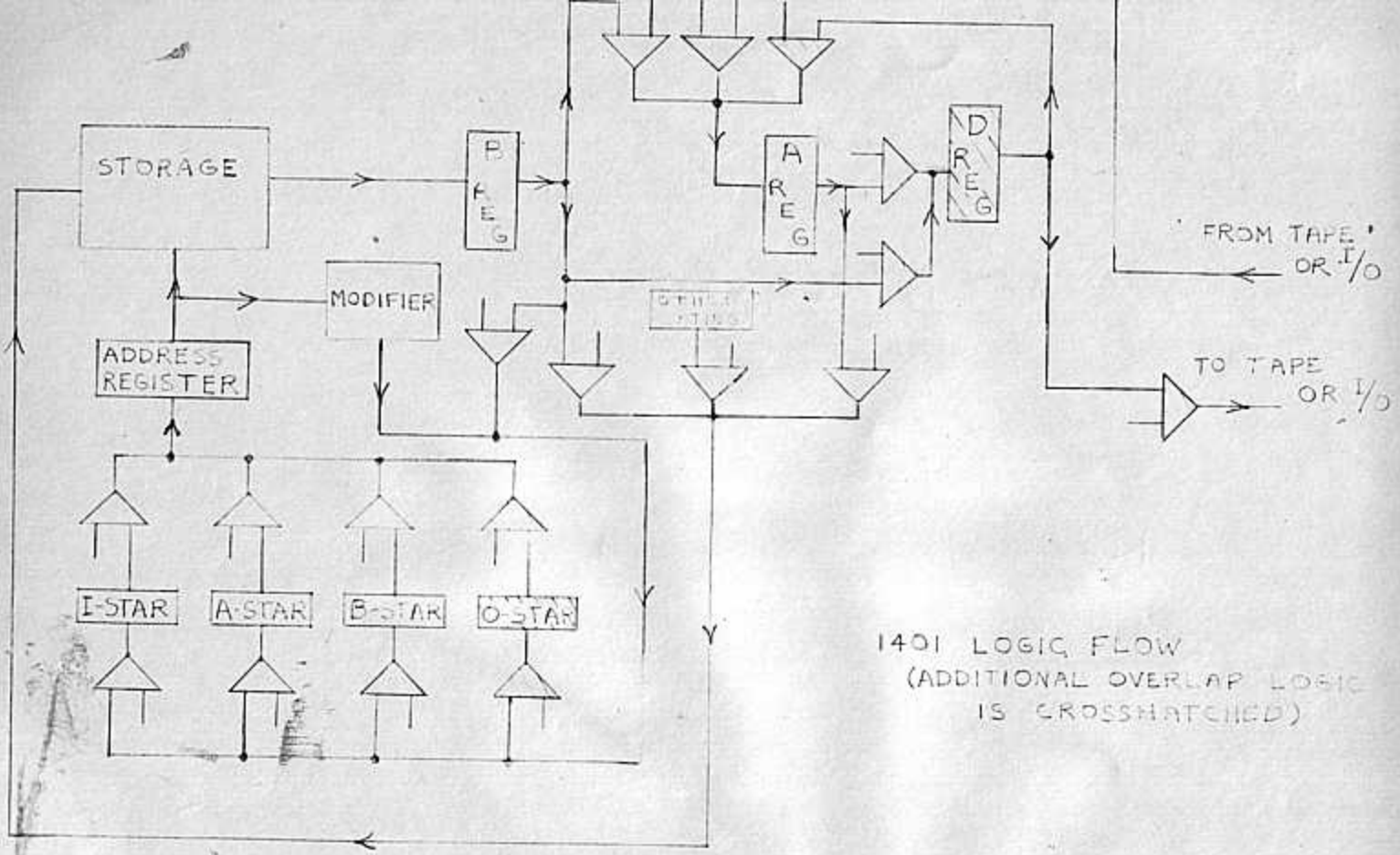
Dept. 280

JLP/ka



1401 LOGIC FLOW
(ADDITIONAL OVERLAP LOGIC IS CROSSHATCHED)