October 28, 1959

MEMORANDUM TO: 1401 File

SUBJECT: Sample Multiplication Problem
(Expanded Arithmetic)

1. The following is a sample multiplication problem, with the product status shown after each addition.

	-25	Multiplicand
	+13	Multiplier
	0000	Product
Set sign and add two x multiplicand	50	
	-0050	
Add one x multiplicand	25	
	-0075	
Shift and add one x multiplicand	25	
	-0325	

2. A more detailed description of this example will be used to demonstrate the multiplication process. The status of the A and B fields and the A and B address registers will be shown throughout the illustration.

   Suppose that the programmer desires to use storage location 526 as the low order position of the A, or multiplicand field, and location 762 as the low order position of the B, or product, field. Thus, for this problem, a word mark must be located in storage position 525 to indicate the high order position of the multiplicand. Since the product field must be at least one position larger than the maximum possible product, it must extend from position 762 through position 758. Thus, a word mark must be placed in position 758 to indicate the high order position of the product field.

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2. A more detailed description of this example will be used to demonstrate the multiplication process. The status of the A and B fields and the A and B address registers will be shown throughout the illustration.

   Suppose that the programmer desires to use storage location 526 as the low order position of the A, or multiplicand field, and location 762 as the low order position of the B, or product, field. Thus, for this problem, a word mark must be located in storage position 525 to indicate the high order position of the multiplicand. Since the product field must be at least one position larger than the maximum possible product, it must extend from position 762 through position 758. Thus, a word mark must be placed in position 758 to indicate the high order position of the product field.

STORAGE

		522	523	524	525	526
M'CAND	A	?	?	?	?	?
M'PLIER / PRODUCT	B	758 ? *	759 ?	760 ?	761 ?	762 ?

ADDRESS REGISTERS

A-AUX	?
A	?
B-AUX	?
B	?

The multiplier (+13) will then be stored in the high order position of the product field (positions 758 and 759), preferably by a "reset add" operation so that the proper sign (A and B bits in this case), is retained. B bits must not be located in positions 760 or 761.

The multiplicand (-25) is stored in positions 525 and 526 with a B bit but no A bit in position 526 to indicate the minus sign.

STORAGE

		522				B 526
A		?	?	?	*2	5
		758	A-B			762
B		1 *	3	?	?	?

ADDRESS REGISTERS

A-AUX	?
A	?
B-AUX	?
B	?

Eight I cycles are then taken to read the op code (@) into the op register and to read the storage locations used into the A and B auxiliary registers and the A and B registers.

STORAGE

		522				B 526
A		?	?	?	*2	5
		758	A-B			762
B		1 *	3	?	?	?

ADDRESS REGISTERS

A-AUX	526
A	526
B-AUX	762
B	762

One A cycle is then taken to test and record in a trigger the sign (minus) of the multiplicand.

B cycles are then taken, and the B address register addresses storage until a B bit is detected. Thus, four B cycles are taken. During the first three B cycles, storage positions 762, 761, and 760 are set to zero. During the fourth B cycle, the sign (plus) of the multiplier is determined, compared with

the sign of the multiplicand (minus) and the product sign (minus) is recorded in a trigger. Also during this fourth B cycle, the digit associated with the B zone (3) is analized with respect to magnitude. Since it is greater than 2, it is reduced by 2, and a B bit is read back into position 759, and the address (759) in the B address register is decremented by "one".

STORAGE

A	522 ?	?	?	*2	B 526 5
B	758 1 *	B 1	0	0	762 0

ADDRESS REGISTERS

A-AUX	526
A	525
B-AUX	762
B	758

Addition is now possible, and an A cycle is taken. During this cycle, the A auxiliary address register addresses storage. The decremented address (525) enters the A address register but the original address (526) remains in the A auxiliary address register. The data in location 526 (5) is entered into the A register.

Now a B cycle is taken, during which the B- auxiliary address register address storage, (762 which contains a zero in this position). The decremented address (761) enters the B-address register only. Also during this cycle, the digit (5) located in the A register is doubled and added to the zero located in the B register. This sum is entered into storage position 762. The product sign, which had been stored in a binary trigger, is entered into the low order position (762) of the B field during this cycle. In this case, the sign (minus) is designated by a B bit.

STORAGE

A	522 ?	?	?	*2	B 526 5
B	758 1 *	B 1	0	0	762 B 0

ADDRESS REGISTERS

A-AUX	526
A	525
B-AUX	762
B	761

An A cycle is again taken during which the A address register addresses storage and is reduced by one (524). The information (2 and word mark) located in storage position 525 is entered into the A register.

A B cycle is now taken during which the B address register addresses storage. The decremented address (760) is read back into the B address register. The digit (2) in the A register is doubled and added (along with the previous carry) to the data in the B register (0). Also during this cycle, the word mark in the A register is sensed, causing the elimination of succeeding A cycles.

STORAGE

A	522 ?	?	?	* 2	B 526 5
B	758 1 *	B 1	0	5	B 762 0

ADDRESS REGISTERS

A-AUX	526
A	524
B-AUX	762
B	760

B cycles will continue to be taken until a B bit is sensed in the B register. Thus, the B address register will address storage during the next two cycles. During the second B cycle, a B bit is sensed, and the magnitude of the digit (1) located in the B register is tested. Since the digit is 1, a B bit and a zero are written back into storage.

STORAGE

A	522 ?	?	?	* 2	B 526 5
B	758 1 *	B 0	0	5	B 762 0

ADDRESS REGISTERS

A-AUX	526
A	524
B-AUX	762
B	758

Onee again, addition is possible, and the A auxiliary register addresses storage. During this A cycle, the decremented address (525) enters the A address register, but the original address (526) remains in the A auxiliary register.

A B cycle is now taken during which the B auxiliary address register addresses storage, is reduced by one, and read into both the B auxiliary address register and the B address register. Also during this cycle, the digit (5) in the A register is added to the digit (0) in the B register, and the sum is entered into storage position 762.

STORAGE

A	522			*2	B 526 5
B	758 1 *	B 0	0	5	B 762 5

ADDRESS REGISTERS

A-AUX	526
A	525
B-AUX	761
B	761

An A cycle is again taken during which the A address register addresses storage and is reduced by one (524). Thus, both a 2 and a word mark enter the A register.

A B cycle is now taken during which the B address register addresses storage, and is reduced by one (from 761 to 760). The digit (5) located in storage position 761 is read into the B register and added to the digit (2) located in the A register. The word mark in the A register stops the generation of succeeding A cycles.

STORAGE

A	522 ?	?	?	*2	B 526 5
B	758 1 *	B 0	0	7	B 762 5

ADDRESS REGISTERS

A-AUX	526
A	524
B-AUX	761
B	760

The B address register then continues to address storage until the B bit (759) is sensed. In this case, after two B cycles, a zero is sensed in the storage position (759) containing the B bit, and a zero only is written back into storage. Again, the B address register continues to address storage until a significant digit is sensed. In this case, one B cycle must be taken, since a "1" is located in the next higher multiplier position. When this "1" is sensed, a B bit is written back into this position (758), along with the word mark, and a zero.

STORAGE

A	522 ?	?	?	*2	B 526 5
B	B 758 *0	0	0	7	B 762 5

ADDRESS REGISTERS

A-AUX	526
A	524
B-AUX	761
B	757

Addition is now possible, and the A auxiliary address register addresses storage. The decremented address (525) enters the A address register only.

The B address register now addresses storage, and the decremented address is written back into both the B address register and the B auxiliary address register. The digit (5) in the A register is also added to the digit (7) in the B register during this B cycle

STORAGE

A	522 ?	?	?	*2	B 526 5
B	B 758 *0	0	0	2	B 762 5

ADDRESS REGISTERS

A-AUX	526
A	525
B-AUX	760
B	760

Once again, the A address register addresses storage. Thus, a two and a word mark are read into the A register, and the decremented address re-enters the A address register.

A B cycle is taken during which the B address register addresses storage, and the digit (2) in the A register is added to the digit (0) in the B register along with the previous carry. The word mark in the A register causes the elimination of succeeding A cycles.

STORAGE

A	522 ?	?	?	*2	B 526 5
B	758 *0	0	3	2	B 762 5

ADDRESS REGISTERS

A-AUX	526
A	524
B-AUX	760
B	759

The B address register continues to address storage until the word mark and the zero in position 758 are sensed, and an I/E change is forced which ends the multiplication operation, and processes the next instruction.

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[redacted]
JLP:bd