December 15, 1958

MEMORANDUM TO: SPACE File

SUBJECT: Changes in Machine Operation

In order to simplify the machine operation, reduce the number of rules of operation, and reduce the component count, the following changes will be made:

1)   On instruction cycles, an address which immediately follows the Operation Code will enter both the A-MAR and B-MAR.

The next address of the same instruction will enter the B-MAR, as before.

2)   Word Mark Set and Clear instructions will be limited to two addresses.

3)   The Storage Clear instruction may be written either with or without an I address.

4)   Recomplementing will be accomplished by causing the B-MAR to reverse-scan until the Word Mark of the next-right field is detected, and then forward-scan to effect recomplementing.

Items 1, 2, and 3 are interrelated, and permit a reduction in component count, a simpler loading routine, and a clarification of machine operation so that program debugging is easier.

A"Word Mark set" or "Word Mark clear" instruction is now executed two addresses per instruction, one on an A cycle and one on a B cycle. If a single word mark is to be set or cleared, the instruction is so written, and the address automatically enters both the A and B MARS. As a result, the word mark is set or cleared on both the A and B cycles of the execution.

Item 4 permits perfect "chaining" of instructions and also results in a reduced component count.

Previously, it was possible to chain instructions, except when an arithmetic operation might cause the B field to change sign. In that case, it was necessary to write the complete instruction so that reference could be made to the instruction for the B field address when recomplementing was called for.

With the new scheme, the only requirement is that an accumulating field in memory have a defined field to the right. Since this is a normal occurrence, it is felt that this requirement is no burden.

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