Microminiature packaging and integrated circuitry: The work of E. F. Rent, with an application to on-chip interconnection requirements

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Research on Rent's rule in electrical engineering, the applied sciences, and technology has been based on the publication of a 1971 interpretation of Rent's memoranda by B. S. Landman and R. L. Russo. Because of the wide impact of Rent's work and requests from researchers, we present his original memoranda in this paper. We review the impact of Rent's work and present the memoranda in the context of IBM computer hardware development since the 1950s. Furthermore, because computer hardware components have changed significantly since the memoranda were written in 1960, a new interpretation is needed for today's ultra-large-scale integrated circuitry. On the basis of our analysis of the memoranda, one of the authors' personal knowledge of the 1401 and 1410 computers, and our experience in the design of high-performance circuitry for microprocessor chips, we have derived an historically equivalent interpretation of Rent's memoranda that is suitable for today's computer components. We describe an application of our historically equivalent interpretation to the problem of assessing on-chip interconnection requirements of control logic circuitry in the IBM POWER4™ microprocessor.

Introduction

The introduction and presentation of empirical rules that describe the interconnectivity of computer hardware components first appeared with the publication of a paper by Landman and Russo in 1971 [1]. This publication presented an overview of an empirical relationship understood by members of the IBM computer development groups prior to 1960, when E. F. Rent wrote two internal memoranda that describe his methods and graphical techniques to illustrate the relationship between properties of computer hardware components. The 1971 paper has been referenced extensively in the literature of several scientific fields, including semiconductor circuitry, computer systems, applied mathematics, the applied sciences, and semiconductor manufacturing technology. Specifically, as semiconductor circuitry continues to increase in complexity to ultra-large-scale integrated (ULSI) circuitry, Rent's work has provided guidance for the design and evaluation of ULSI chips and the technologies with which they are manufactured [2, 3]. As an example, researchers have derived theoretical models based on the 1971 interpretation of Rent's work [1, 4] to anticipate properties of future computer systems. In this work, the inputs to the models are empirical parameters that are referred to as *Rent parameters*.

There remains a need in the literature for the publication of the contents of the two memoranda. We have obtained copies of Rent's memoranda, and one goal of this paper is to present them for the first time within the context of the development of computer hardware components at IBM since the 1950s. To achieve this goal, we present an overview of the two IBM computers that

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Rent analyzed in the memoranda and a review of computer systems development at IBM from the 1950s to the present. A second goal of this paper is to discuss an interpretation of these memoranda that is suitable for today's computer hardware components, since the components in today's systems differ significantly from those discussed in the original memoranda. This paper also describes an application of this interpretation to the problem of assessing the extent to which estimates provided by existing wire-length distribution models agree with actual wire-length measurements. Here, the desired goal is to obtain improved estimates of wire-length requirements for circuitry on ULSI chips. For this application, we obtained model estimates for wire-length requirements and compared the estimates with measured wire-length requirements in manufactured chips.

This paper is organized as follows. We review the impact of Rent's work, followed by a review of computer systems hardware, including IBM computer systems built since the 1950s and then, more specifically, two systems that Rent discusses in his memoranda. Rent's memoranda on microminiature packaging are then presented. We describe an interpretation of the memoranda that is suitable for today's computer hardware components and then describe an application of this interpretation to existing wire-length distribution models and interconnection requirements, followed by a discussion and presentation of our conclusions.

Impact of Rent's work

Rent's work has had a significant impact in a range of scientific fields, and the literature that references the 1971 paper [1] can be broadly arranged into the following scientific areas: interconnections, semiconductor circuitry, computer systems design, applied mathematics, applied sciences, and semiconductor manufacturing technology. The purpose of this section is to provide an overview of the impact of Rent's work and to provide examples of research in each of these areas.

Several interpretations of the 1971 paper exist, including the *external interpretation* [4–8] and the *topological interpretation* [8, 9]. According to the external interpretation, the *external Rent parameters* $\{k, p\}$ are obtained from the slope and y-intercept of linear fits to log–log plots of the number of input/output pins T_{IO} as a function of the number of gates N_{gates} without further partitioning [1, 4–8, 10]. In this interpretation, k represents the Rent coefficient and p represents the Rent exponent. According to the topological interpretation, the *topological Rent parameters* $\{k*, p*\}$ are obtained by first partitioning each design hypergraph hierarchically and then extracting the slope and y-intercept from linear fits to log–log plots of the number of terminals as a function of the number of gates, as described in detail in [8–12]. In this interpretation, $k*$ represents the Rent coefficient and $p*$ represents the Rent exponent. Additional information about the external interpretation is described in [4, 5]. The literature that discusses Rent's work prior to the interpretation [13] described in this paper, including references presented in this section, is based on the 1971 interpretation [1].

Table 1 [1, 4, 5, 8, 10, 14] shows values of the Rent parameters—obtained with different interpretations of Rent's work—for several design types. In this table, the values of the Rent coefficient and Rent exponent are shown for block graphs, square arrays, static random access memory (SRAM), gate arrays, chip and module, board and system, microprocessors, application-specific integrated circuit (ASIC)-like control logic, and benchmark circuits. The date of each analysis and design names are also shown. The data in the table shows that the value of the Rent exponent tends to be less than unity for these interpretations. The data also shows that the Rent exponent can take on a range of values from 0.12 to 0.99, and that the Rent coefficient can take on a larger range of values from 0.8 to 82.

Interconnections

To describe the increasing complexity [2] of interconnections in semiconductor circuitry and to estimate the physical and electrical characteristics of chip wiring, researchers have developed models based on the 1971 interpretation of Rent's work. The purpose of this section is to discuss these characteristics, which include on-chip interconnection requirements, performance metrics for interconnections, power dissipation in interconnections, signal fan-out distributions, and interconnection congestion in a design layout.

On-chip interconnection requirements

The earliest application of the 1971 work has been the derivation of interconnection models by Donath [14, 15], Davis et al. [5–7, 16–19], and Christie and Stroobandt [9]. These interconnection models provide estimates for the wire-length distributions, average wire length, and total interconnection length required to wire chip circuitry correctly. These models assume that the designs are square, are completely tiled with square logic gates, have signals with unity fan-out, contain circuitry that is associated only with the logical function of the design, and allocate all of the available space for wire routing. The topological Rent parameters are input into the expressions provided by the Donath models [14, 15] and the Christie model [9], and the external Rent parameters

Table 1 Rent coefficient and exponent for different chip design types. The design type, date of the analysis, name of the design, and Rent parameters are shown. NA indicates that the information is not available. The ranges of the Rent parameters for benchmark circuits are shown. The Rent coefficient and exponent for individual benchmark circuits are given in [8]. ©2004 IEEE. Reprinted from [13] with permission.

Design type	*Date*	*Design name*	*Rent coefficient*	*Rent exponent*
Block graphs	1971	L1 in [1]	3.52	0.57
		L2 in [1]	4.73	0.75
		L3 in [1]	29.66	0.69
		L4 in [1]	20.12	0.66
Square arrays	1979	A in [14]	NA	0.67
		B in [14]	NA	0.59
		C in [14]	NA	0.75
		D in [14]	NA	0.57
		E in [14]	NA	0.47
		F in [14]	NA	0.75
Square arrays	1981	A in [15]	NA	0.7
		B in [15]	NA	0.7
		C in [15]	NA	0.5
SRAM	1990	Table 9.5 in [4]	6	0.12
Gate arrays	1990	Table 9.5 in [4]	1.9	0.50
Chip and module	1990	Table 9.5 in [4]	1.4	0.63
Board and system	1990	Table 9.5 in [4]	82	0.25
Microprocessors	1990	Table 9.5 in [4]	0.82	0.45
Microprocessors	1995	Figure 3 in [5]	2.09	0.36
		Figure 8 in [5]	3.8	0.75
		Figures 9–11 in [5]	5.0	0.8
ASIC-like control logic designs in a microprocessor	2004	IFU in [10]	0.8	0.69
		FPU in [10]	2.2	0.66
		FXU in [10]	4.4	0.61
		IDU in [10]	20.5	0.30
		ISU in [10]	23.3	0.31
		LSU in [10]	7.3	0.46
Benchmark circuits	2003	Table I in [8]	[2.9, 9.3]	[0.60, 0.99]
		Table III in [8]	[2.7, 7.8]	[0.26, 0.82]
		Table IV in [8] for circuits {i1, ⋯, i8}	[4.9, 11.7]	[0.55, 0.82]
		Table IV in [8] for circuits {ibm01, ⋯, ibm07}	[4.6, 9.2]	[0.57, 0.79]

are input into the expressions provided by the Davis model [5–7].

Additional work that describes interconnection requirements in large-scale integration (LSI) and very large-scale integration (VLSI) chips is provided in [10, 20–22]. Methods to extract Rent parameters are discussed in [4, 5, 8, 9, 23–25]. Interconnection requirements have been assessed in microprocessors [4], ASICs [4], memory elements [4], and control logic circuitry in high-performance microprocessors [10].

Interconnection models have also been developed for designs that are rectangular [26], designs that contain signals with multiple fan-out [27, 28], designs that contain one or more blockages [29], field-programmable gate arrays (FPGAs) [30–35], three-dimensional integrated circuits [32, 36–40], and three-dimensional anisotropic systems [41].

Performance metrics

The wiring distributions predicted by the existing wire-length distribution models in the previous section, combined with technology information (such as wire pitch and the number of available metal layers), have been used to obtain interconnection performance metrics such as the one that combines a wire distribution model with a 50% delay model for interconnections from the input of an inverter driver to the output of a inverter receiver, as discussed in [42]. These metrics have helped researchers decide how to optimize wire and inter-layer dielectric characteristics, such as metal thickness and dielectric thickness.

Power dissipation

Models for power dissipation and power estimation that take into account the impact of interconnections have been developed and are described in [43].

Fan-out distributions

Methods to estimate the number of signals with each fan-out in chip designs are described in [28, 44, 45].

Congestion

Methods to estimate interconnection congestion in chip designs are provided in [46, 47].

Semiconductor circuitry

Researchers have also developed models that are based on Rent's work to partition circuitry and to estimate additional circuitry requirements, such as switching requirements, gate count, and gate area. Bakoglu [4] and Stroobandt [48, 49] provide overviews of research in interconnection requirements in ULSI circuitry. This section provides additional references for these models. Methods to partition circuitry are discussed in [50, 51], switching requirements in circuitry are discussed in [52], and methods to estimate the number of logic gates and the gate area in chips are presented in [53, 54].

Computer systems design

The design of computer systems has changed significantly in the past 50 years [2]. Bakoglu [4], Sai-Halasz [55], and Dooijes [56] provide three discussions of trends in computer technology. Researchers in computer systems design have referenced Rent's work in several applications, such as digital information processing, estimation of system-level interconnection requirements, computer architecture, packaging, testing, interconnection requirements in systems-on-chips (SoCs), and system-cost models for evaluating the tradeoff between using off-chip interconnections and increasing chip area and the number of on-chip interconnections. In addition, a research group at the University of California at Los Angeles is collaborating with Hewlett-Packard Company to develop a chemically assembled electronic nanocomputer (CAEN) [57]. The purpose of this section is to present a discussion of some of these applications.

Digital information processing

In the field of digital information processing, Keyes [58–60] references the papers of Landman and Russo [1] in his discussions of the physics of VLSI components.

System-level interconnection requirements

Methods to estimate system-level interconnection requirements are discussed in [22, 52, 61–66]. A series of workshops to present material on the subject of system-level interconnect prediction (SLIP) was established in 1999, and additional information is available online [67].

Computer architecture

Methods to extract Rent parameters from different types of computer architectures are discussed in [24, 25]. The impact of Rent's work on strategies to design massively parallel systems is discussed in [25]. Estimates of the number of memory bits that are required to replace a *random logic* circuit are discussed in [68]. Additional applications in computer architecture for nanotechnology are discussed in [69].

Packaging

The impact of interconnections on system and packaging requirements is discussed in [4, 22, 55, 56, 70–72]. Interconnection requirements at the interfaces between chips and modules are discussed in [73].

Testing

Methods for chip testing and fault analysis are presented in [74].

SoCs

Design methodologies for SoCs and the associated interconnections, including global signals,

clock distributions, and power grids, are discussed in [40].

System-cost models

A system-cost model has been developed [75, 76] to evaluate the tradeoff between using off-chip interconnections and increasing the silicon die area, which increases the number of on-chip interconnections. In this model, there are three cost elements: the cost of processing silicon, the cost of wasted silicon that is unusable after processing, and the cost of assembly. This model assumes that the cost of assembly is proportional to the number of pins on the package, which they obtain from references to Rent's work.

Applied mathematics

Rent's work has also been discussed in the field of applied mathematics. Mandelbrot discusses this work in his book entitled *Fractals: Form, Chance, and Dimension* [77]. Ozaktas discusses additional concepts of connectivity for circuit graphs and provides generalizations for systems with a Rent exponent that takes on different values throughout the interconnection hierarchy [78, 79].

Applied sciences

Researchers have applied Rent's work to molecular electronics and optics. This section discusses these applications and provides references.

Molecular electronics

Researchers in molecular electronics have developed a cellular FPGA. Inputs to this system include Rent's parameters and information about cellular automata [80]. This work points out that cellular FPGAs differ from traditional FPGAs because they are periodic structures. Cellular FPGAs support only nearest-neighbor connections, rather than interconnections on several metal layers, as is the case for ULSI back-end-of-line chip architectures.

Optics

Rent's work has been applied to an assessment of interconnectivity requirements of free-space optical interconnections, as reported in [81, 82], where brief comparisons with conventional interconnections are provided.

Semiconductor manufacturing technology

The increasing complexity of today's manufacturing technologies makes it more and more difficult to implement innovations in manufacturing. Although innovations are costly as a result, they do allow us to manufacture chips with desirable characteristics such as higher performance, lower power dissipation, higher circuit density, and higher yield.

Recognizing the need to estimate the impact of these desirable characteristics for each technology, researchers have developed performance models for chips and systems. These models include a cycle-time model [55], SUSPENS [4, 83], AIM [84], GENESYS [85], RIPE [86], BACPAC [87, 88], and GTX [89]. The purpose of this section is to describe briefly the characteristics of three of the models: SUSPENS, BACPAC, and GTX; information about the other models is available in the references listed.

The Stanford University System Performance Simulator (SUSPENS) [4, 83] is a performance model that calculates the maximum clock frequency, chip area, and chip power dissipation as a function of a list of parameters that includes physical constants, Rent's parameters, number of logic gates on the chip, total capacitance of the interconnection per unit length, interconnect pitch, and board-level characteristics.

The Berkeley Advanced Chip Performance Calculator (BACPAC) [87, 88] is a model that calculates characteristics of system-level performance as a function of device characteristics, interconnection characteristics, and system characteristics. The device characteristics include the operating voltage, threshold voltage, gate oxide thickness, and drain current. The interconnection characteristics are the number of metal layers, metal resistivity, and interlayer dielectric constant. The system-level inputs include the design size and Rent's parameters. The outputs of the model are listed in [87] and include chip area, maximum clock frequency, wiring requirements, power dissipation, and projected yield.

The Microelectronics Advanced Research Corporation (MARCO) Gigascale Systems Research Center (GSRC) Technology Extrapolation (GTX) [89] is a system model that calculates system-level performance characteristics such as system cycle time, die size, and power dissipation.

Review of computer systems hardware

Significant changes have occurred in the development and manufacturing of computer hardware components since 1960, when Rent wrote his two memoranda. The purpose of this section is to review technical hardware innovations in computer hardware components sold in the past five decades and to describe the two computers discussed in Rent's memoranda [90–94].

Computer systems since the 1950s

Throughout much of the 1950s, as indicated in **Table 2** [3, 94–98] a key component of IBM computers was the

Table 2 Typical hardware components in IBM computers built since 1952. The SMS card refers to the IBM proprietary standard modular system (SMS) of circuit packaging. The term SLT refers to the IBM solid logic technology (SLT).

Date [94]	*Technology* [94]	*IBM system* [94]
1952	Cathode-ray vacuum tubes for storage, magnetic drum and tape storage, card reader–punch	701
1954	5 ft × 3 ft × 6 ft CPU, rotating magnetic drum, card reader–punch, magnetic core memory	650
1959	SMS circuit packaging technology with discrete transistors and resistors; jumper wires on 2.5-in. × 2.5-in. circuit cards; punched cards, magnetic tape	1401
1959	SMS circuit packaging technology	7090
1960	SMS circuit packaging technology	1410
1964	SLT hybrid solid logic technology with 1.6-in.^{2} printed circuit boards; cards with semiconductor chips, printed lines and resistors; ferrite-core memories	System/360
1968	Monolithic integrated circuits with 1–4 circuits per silicon chip; four chips per ceramic module	Model 85
1970	Monolithic systems technology; all-semiconductor main memory	System/370* Model 85
1980	Thermal conduction module (TCM) with >100 chips	3081 [3, 94]
1985	First mainframe with one-million-bit memory chips	3090* [3, 94]
1990	VLSI: four-million-bit memory chip, 800,000 transistors per chip	RISC System/6000*
1994	First complementary metal oxide semiconductor (CMOS) mainframe	System/390* G1
1997	CMOS mainframe with up to ten microprocessors	System/390 G4
2001	ULSI CMOS technology with 170 million transistors in a 2-cm × 2-cm silicon chip [95]	pSeries* 690 [95]
2004	121 million transistors in a 2-cm × 2-cm silicon chip [96]	eServer* z990 [96]
2004	276 million transistors in a 2-cm × 2-cm silicon chip [97, 98]	eServer i5 550 [97, 98]

cathode-ray vacuum tube for storage, as well as conventional switching vacuum tubes for logic circuitry; as a result, a single central processing unit (CPU) composed of many of these tubes occupied approximately 90 cubic feet of space. Table 2 lists the IBM systems and the associated innovations in these systems since the 1950s. This table shows that by 1959–1960, vacuum tube technology was superseded by the introduction of discrete transistors in such IBM computers as the 1401 and 1410—the computers that Rent discusses in his memoranda.

In 1964, discrete transistor technology was replaced by hybrid solid logic technology consisting of semiconductor chips, printed wires, and printed resistors. Computer hardware components constructed in hybrid solid logic technology appear in the IBM System/360* computer.

In 1980, IBM introduced the 3081 system. This system introduced the packaging concept of a thermal conduction module (TCM) to the marketplace. The design of the TCM ... *was driven by partitioning and wiring considerations influenced by Mr. Rent's work before semiconductor technology was able to contain an entire high-performance CPU on a single chip.*[1]

Figure 6 in the paper by Seraphim and Feinberg [3] shows a planar board of the 3081 system, and it is stated there that the TCMs plug directly into the printed circuit back panel. A review of the evolution of electronic packaging in IBM from the early 1960s through 1981 is presented in [3].

In 1985, IBM introduced its first mainframe with memory chips containing one million bits each, as indicated in Table 2. By 1990, each memory chip in the RISC System/6000 contained four million bits.

In 2001, IBM introduced computer systems based on the POWER4* chip that contained two CPUs, approximately 174 million transistors, and more than one

[1]Private communication, Gerry Kopcsay, 2005. Mr. Kopcsay is a member of the Systems Power, Packaging, and Cooling Department at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY.

mile of copper wiring on a penny-sized 4-cm^2 silicon chip [95], thereby realizing a significant volume reduction compared with the early 1950s CPU.

In 2004, IBM introduced two computer systems. The eServer z990 contains 121 million transistors, and the eServer i5 550 contains 276 million transistors.

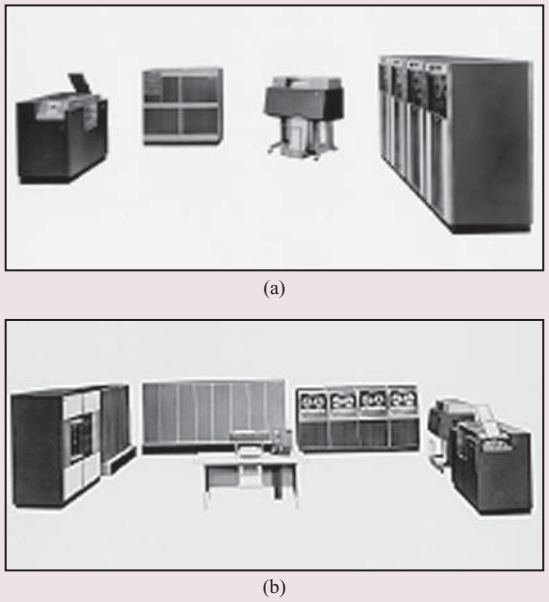
IBM 1401 Data Processing System

The 1401 [**Figure 1(a)**] was introduced in the marketplace on October 5, 1959, and was sold for nearly 12 years, until February 8, 1971. Composed entirely of discrete transistors, the main components of the IBM 1401 were a 1401 processing unit, 1402 card reader–punch, and 1403 printer. It was the first computer to sell more than 10,000 units [90, 91]. According to the IBM Corporate Archives [90], the system *performs functions previously requiring a number of separate machines: card reading and punching, separation of output cards, calculating, and printing*. Within the 1401 system itself, the IBM 1401 processing unit *controls the entire system by means of its stored program. It performs the arithmetic and logical functions, controls card reading and punching, magnetic tape input and output, and tells the printer what to print and where to print it* [90]. Regarding speed, the press datasheet reported that *in one minute, the 1401 Processing Unit can perform 193,300 additions (eight-digit numbers) or 25,000 multiplications (six-digit numbers by four-digit numbers)* [90].

IBM 1410 Data Processing System

The 1410 [**Figure 1(b)**] was introduced in the marketplace on September 12, 1960, and was sold for nearly ten years, until March 30, 1970 [92]. It was offered in three basic configurations, with an optional paper tape reader and magnetic character reader [92, 93]. These configurations are the following:

- *IBM 1410 Data Processing Card System:* This configuration was a *high-speed flexible system containing large-volume storage facilities and fast input/output units for up-to-the-minute, accurate punched card output and printed reports* [92]. It consisted of a 1402 card reader–punch, 1403 printer, 1411 processing unit, 1414 input/output synchronizer, and 1415 console.
- *IBM 1410 Data Processing Tape System:* This configuration *added to the speed and efficiency of the 1410 card system with high-volume storage capacities and increased data input/output speeds* [92]. Magnetic tape units were available with this system.
- *IBM RAMAC 1410 Data Processing System:* This configuration *provided mammoth disk storage facilities for the IBM 1410 Data Processing Systems,* [and] *consisted of the 1410 card system, with or without the tape units* [92]. The configuration also included disk storage.



(a)

(b)

Figure 1

(a) IBM 1401 Data Processing System. From left to right, the components are the 1402 card reader-punch, the 1401 computer, the 1403 printer, and the 7330 magnetic tape unit. (b) IBM RAMAC 1410 Data Processing System. From left to right, the components are 1405 disk storage; 1414 input/output synchronizer, 1411 processing unit; 1415 console; four 7330 magnetic tape units; 1403 printer; and 1402 card reader–punch. (Courtesy IBM Corporate Archives.)

Microminiature packaging: The memoranda of E. F. Rent

The previous section has presented a review of the computer hardware systems environment that existed in 1960 when Rent wrote his memoranda. The purpose of this section is to present the two memoranda within the context of this environment. In the memoranda, Rent describes his analysis of the IBM 1401 and 1410 computer systems and describes his method to deduce an empirical relationship between the properties of the hardware components in these systems. The first memorandum is shown in Appendix A on pages 784–788. This memorandum discusses the 1410 and is dated November 28, 1960. The second memorandum is shown in Appendix B on pages 789–791. This memorandum discusses the 1401 and the 1410 and is dated December 12, 1960.

Roy Russo 273 MyL

November 28, 1960

Memorandum to: File

Subject: Microminiature Packaging - Logic Block to Pin Ratio

In order to better determine the ratio of socket pins to logic blocks required for a mother board in a microminiature system, four chassis of the 1410 computer were reviewed. The review consisted of determining the number of socket pins (edge connectors) that would be required to implement all of the logic of a chassis on one mother board.

The chassis that were chosen were all in the CPU section of the computer and were:

C1 Program and address register controls
C2 Adder and controls
C3, 1401 compatibility, data registers and data assembly
D1 Op - decode matrix

The circuit count was made by card type and then a count of one given for each of the following: 2 way logic block, 3 way logic block, emitter follower, indicator driver, power inverter, line driver etc. No count was made for diode clamp cards or resistor load cards. All unused circuits on cards were removed from the count to give an actual logic circuit count for each chassis. The net edge connector count required a total for all edge connectors on a chassis less, (1) those connectors that were used to feed signals across a chassis and not go to any logic on the chassis and (2) those connectors that were used to distribute to the adjacent chassis signals that were developed on the chassis. A count was also made of the actual number of logic pins involved on the chassis. This was done to help determine the number of printed wires that would be required on the mother board for these chassis.

Figure #1 is a summary of all these counts. The most significant thing that can be derived from these figures is that the average block to pin ratio for these four chassis is 2.27/1. A close look at the block to pin ratios for these four chassis show that the three control chassis are almost identical and the adder chassis has a higher block to pin ratio. This is reasonable as the adder which is the bulk of the chassis contains a lot of logic and has a nominal amount of input output lines. Therefore, the average of the three control chassis will be considered as more typical of all chassis and will be used as the reference point in further discussions. The average block to pin ratio is 2.06/1 with an average of 848 logic blocks and 412 edge connectors per chassis. This ratio is one half the 4.2/1

obtained from the graph drawn by Mr. P. Schulz of Manufacturing Research. These figures are as expected as Mr. Schulz graph was obtained chiefly from high density packaged cards which do not represent an entire system, but only parts of the system. When an entire system must be packaged in high density cards, it is inevitable that the block to pin ratio will go down because a good many of the cards must contain the small bits and pieces of the computer controls which heretofore have not been considered or discussed when high density packaging is demonstrated. For actual systems where high density double and triple SMS cards are to be used the standard single card is also used as it is most efficient in implementing the small bits and pieces which invariably go into a computer. This fact is also brought out on page 14 by Mr. H. D. Harford in a report made by the standard circuits group dated August 24, 1960.

Conclusion from this survey is that a more realistic value for socket pins required to handle N number of logic blocks can be obtained by drawing a new line on the original graph by Mr. Schulz (Fig. #2). This line would pass through the "Single Card Unit Logic 10 Pin Avail" point and the new point generated in this report, namely 849 logic blocks and 412 pins. A few points on the graph are:

Blocks	Pins
100	95
150	125
200	152
300	200
500	280

Figure #3 shows the drastic reduction in Block to Pin ratio that occurs with an increase in pins per card when using the new curve drawn on Fig. #2.

An investigation of a number of the smaller 1401 cube chassis is planned in order to further verify the accuracy of this report. If this checks out then it can be concluded that this new curve is reasonably accurate and should be used to determine the minimum socket pins for a microminiature mother board of N logic blocks.

E. F. Rent

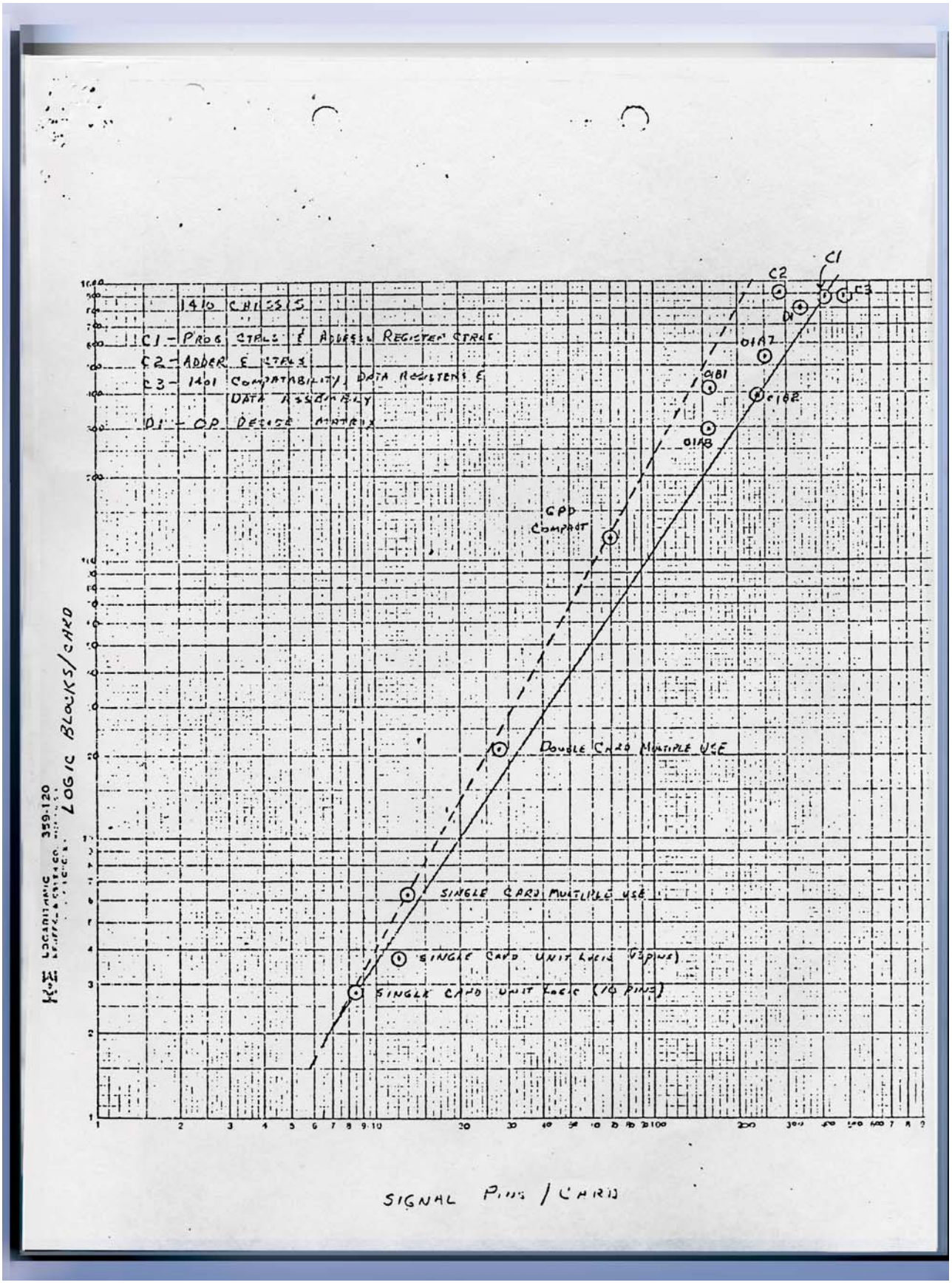
EFR/bn

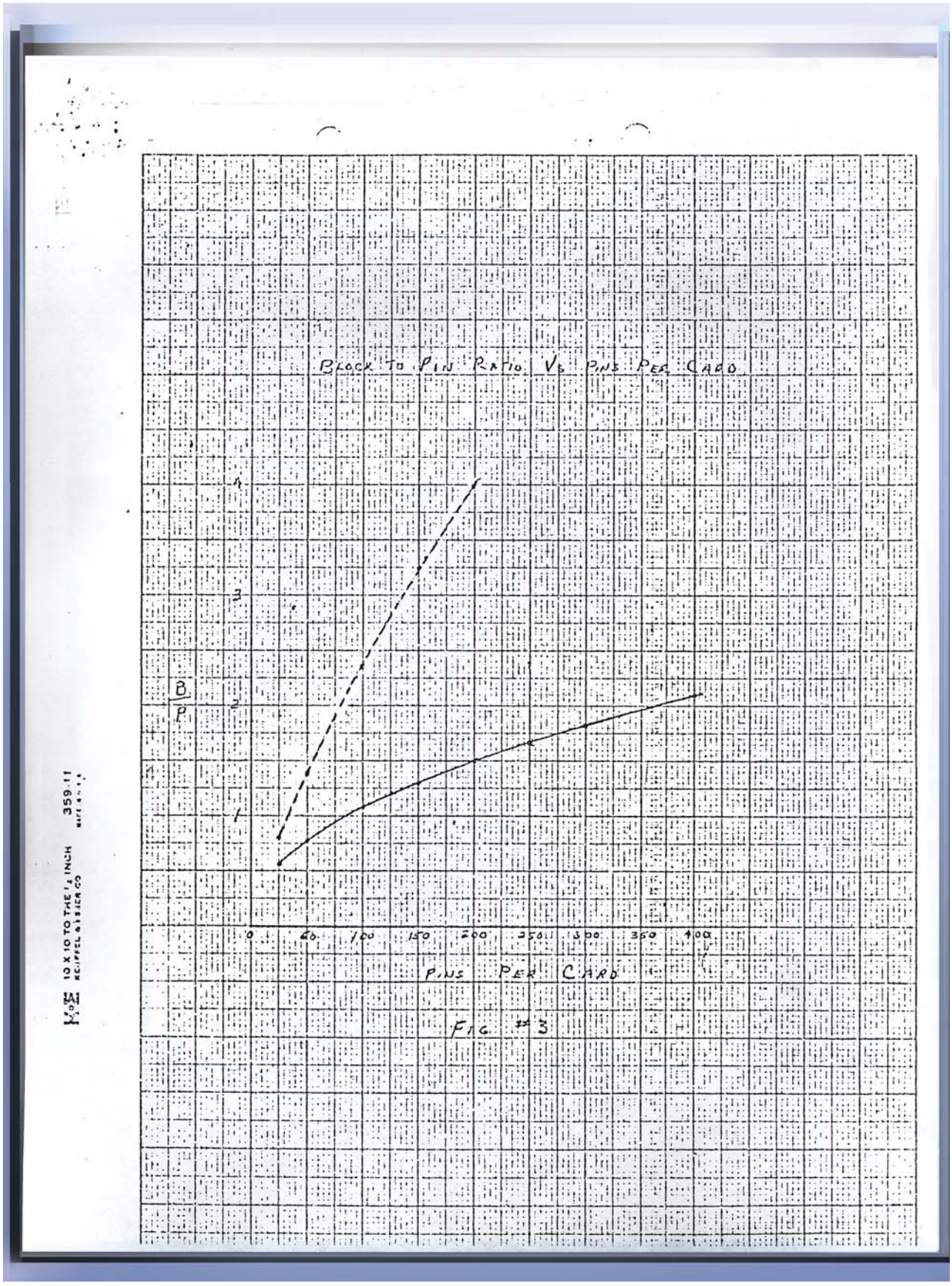
cc: Messrs: L. R. Adams
P. Schulz
W. K. Springfield

FIGURE #1

Chassis	11 C1	11 C2	11 C3	11 D1
Total Cards	225	229	216	192
Total Circuits	904	964	945	906
Circuits not used	86	56	79	102
Not Circuits Used	878	908	866	804
Total SMS Pins	2460	2515	2520	2328
Pins not used	229	134	215	277
Net Pins Used	2231	2381	2305	2051
Edge Connectors Used	647	741	611	765
Thermal E.C.	2	2		2
Feed Through	229	456	130	424
Net E.C. Needed	416	283	481	339
Block to E.C. Ratio	2.1/1	3.2/1	1.8/1	2.4/1

Total Logic Block for 4 Chassis	3456
Total Edge Connectors for 4 Chassis	1519
Average Logic Block to Edge Connector Ratio	2.27/1
Average of Control Chassis (C1,C3, and D1)	2.06/1


1410 CHIPS
C1 - PROG CTRLS & ADDRESS REGISTER CTRLS
C2 - ADDER & CTRLS
C3 - 1401 COMPATABILITY, DATA REGISTERS & DATA ASSEMBLY
D1 - OP DECODE MATRIX
C1
C2
C3
D1
01A7
01B1
01B2
01A8
GPD Compact
DOUBLE CARD MULTIPLE USE
SINGLE CARD MULTIPLE USE
SINGLE CARD UNIT LOGIC (8 PINS)
SINGLE CARD UNIT LOGIC (10 PINS)
LOGIC BLOCKS/CARD
SIGNAL PINS / CARD


BLOCK TO PIN RATIO VS PINS PER CARD
B/P
1
2
3
0
50
100
150
200
250
300
350
400
PINS PER CARD
FIG. #3
10 X 10 TO THE 1/4 INCH
359-11

Roy Russo 274
MYL

December 12, 1960

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Subject: Microminiature Packaging - Logic Block to Pin Ratio

Reference: My memorandum to File dated November 28, 1960

Four chassis of the 1401 computer were checked to determine the amount of logic on the chassis and the number of edge connectors required to communicate to it. The two main differences between this 1401 count and the 1410 count are the reduced size of the chassis and the CTDL logic. The logic count for CTDL was determined by the circuits on an SMS card and nothing was added for logic "OR" functions that are performed by tying two collectors together.

The 1401 chassis checked were:

01A7	-	Address Register
01A8	-	Address Modification
01B1	-	OP Register and Decode
01B2	-	Process Control

The pertinent data for these chassis is shown in Figure #1 and then plotted on the graph in Figure #2. It should be noted that these chassis points are quite scattered on the graph but still they fall between the curve for compact cards and the curve derived from 1410 chassis counts.

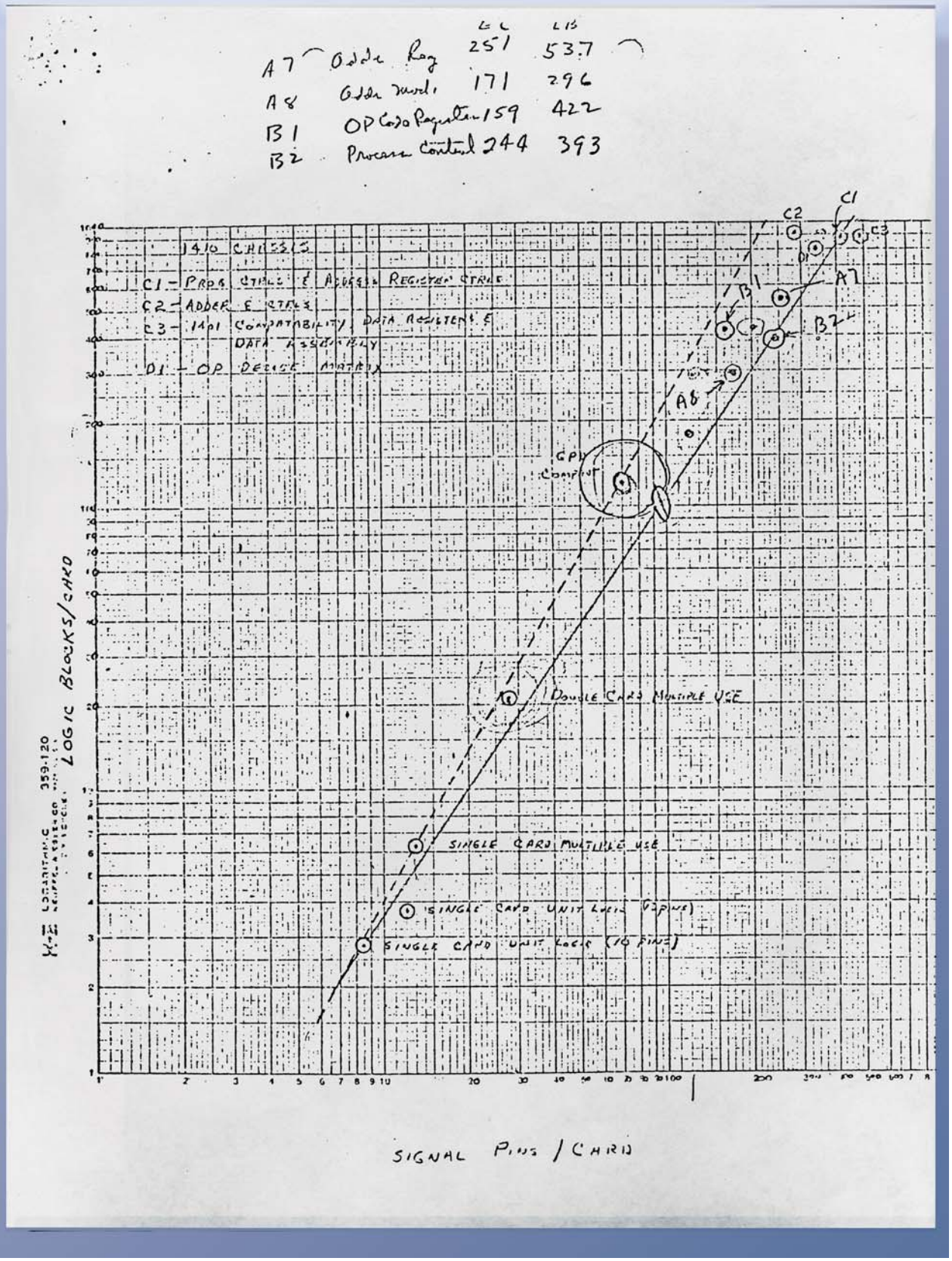
These chassis counts verify that the curve drawn from the 1410 counts when used would not pin limit the mother board. Since 120 pins is reasonably easy to obtain with double sided contacts on a triple SMS card, it was chosen. Then, from the curve it can be seen that 120 pins can handle 140 logic blocks. The mother board will provide space for 180 logic blocks in order to realize an average usage of 140 logic blocks per board, to provide more flexibility in locating the secondary cards, and also to ease the mother board printed wiring problem.

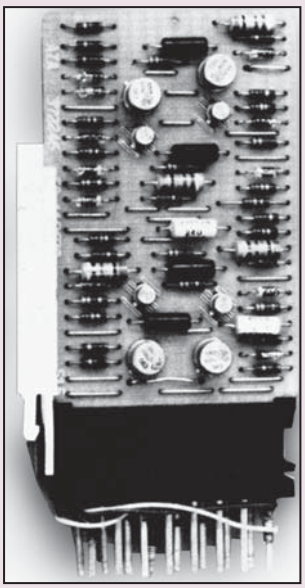
E F Rent
E. F. Rent

EFR/scf

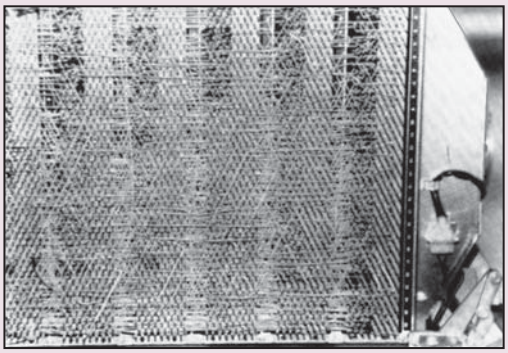
Chassis	01A7	01A8	01B1	01B2
Total Cards	132	114	145	130
Total Circuits	558	334	424	402
Circuits Not Used	21	38	19	9
Net Circuits Used	537	296	405	393
Edge Connectors Used	314	204	205	374
Feed through E. C.	63	48	46	130
Net E. C. Needed	251	156	159	244
Block to E. C. Ratio	2.14/1	1.9/1	2.54/1	1.61/1

Figure #1


LC LIS
A7 Odde Reg 251 537
A8 Odde Mod. 171 296
B1 OP Code Register 159 422
B2 Process Control 244 393
1410 CHISSIS
C1 - PROG CTRL & ADDRESS REGISTER CTRLS
C2 - ADDER & CTRLS
C3 - 1401 COMPATIBILITY, DATA REGISTERS & DATA ASSEMBLY
D1 - OP DECODE MATRIX
C1
C2
C3
D1
A7
B1
B2
A8
GPL Compiler
DOUBLE CARD MULTIPLE USE
SINGLE CARD MULTIPLE USE
SINGLE CARD UNIT LOGIC (12 PINS)
SINGLE CARD UNIT LOGIC (10 PINS)
LOGIC BLOCKS/CARD
SIGNAL PINS / CHIP



(a)



(b)

Figure 2

(a) Front side of a card and (b) back side of a chassis in the 1401. These images originally appeared in [3].

The 1401 and 1410 hardware components that Rent discusses in the memoranda are the *computer chassis*, *card*, *circuit count*, and *edge connector count*. The computer chassis contains several cards that are connected in the chassis. Each card is composed of one or more circuits; the circuits on the card are either *used circuits* or *unused circuits*. The term *used circuit* refers to a circuit that is connected and performs some function; the term *unused circuit* refers to a circuit that exists yet is not required. The purpose of edge connectors is to connect used circuits on a card with other used circuits located on other cards within the chassis. A circuit is also referred to as a *logic block*. Photographs of a *card* and the wiring on the back of a *chassis* are shown in **Figure 2**. In the earlier memo, Rent describes his method to obtain the *circuit count* and *edge connector count* of the cards on each chassis of the 1410 computer system as follows: *The circuit count was made by card type and then a count of one given for each of the following: 2 way logic block, 3 way logic block, emitter follower, indicator driver, power inverter, line driver etc. No count was made for diode clamp cards or resistor load cards. All unused circuits on cards were removed from the count to give an actual logic circuit count for each chassis. The net edge connector count required a total for all edge connectors on a chassis less, (1) those connectors that were used to feed signals across a chassis and not go to any logic on the chassis and (2) those connectors that were used to distribute to the adjacent chassis signals that were developed on the chassis.*

On pages 787 and 791 are Rent's plots of the circuit count per card as a function of the number of edge connectors per card on log–log graph paper. Rent also calculated the average block-to-edge-connector ratio, which is shown in another log–log plot on page 788. He wrote in the memorandum (page 784), *Therefore, the average of the three control chassis will be considered as more typical of all chassis and will be used as the reference point in further discussions*. On pages 787 and 791, the ordinate is labeled *logic blocks/card*, and the abscissa is labeled *signal pins/card*. Each of these plots contains several data points added by hand, where the data points are the number of logic blocks and number of edge connectors obtained according to the descriptions quoted above. A solid line is drawn by hand through several data points in these plots, and Rent pays particular attention to the solid line that connects the point labeled *C1* with the point labeled *single card unit logic (IO pins)* (see page 785 for a discussion and a listing of the points that Rent identifies on the line). An inspection of this line indicates that it may be described by the expression,

$$y = m \times x + b, \tag{1}$$

where y represents the log of the ordinate and x represents the log of the abscissa, and where we obtain $m = 1.49$, $b = -0.94$ for the line drawn on the plot. This expression may be rearranged as

$$x = m' \times y + b', \tag{2}$$

where $m' = 0.67$ and $b' = 0.63$, and also as the expression,

$$X = B' Y^{m'}, \tag{3}$$

where $b' = \log(B')$, $x = \log(X)$, $y = \log(Y)$. Y represents the ordinate, and X represents the abscissa.

In the second memo, Rent performs his analysis on the 1401 computer system and considers four separate chassis labeled *01A7*, *01A8*, *01B1*, and *01B2* in the memo. The plot of the data obtained for these four chassis is shown on page 791, which is a log–log plot similar to that on

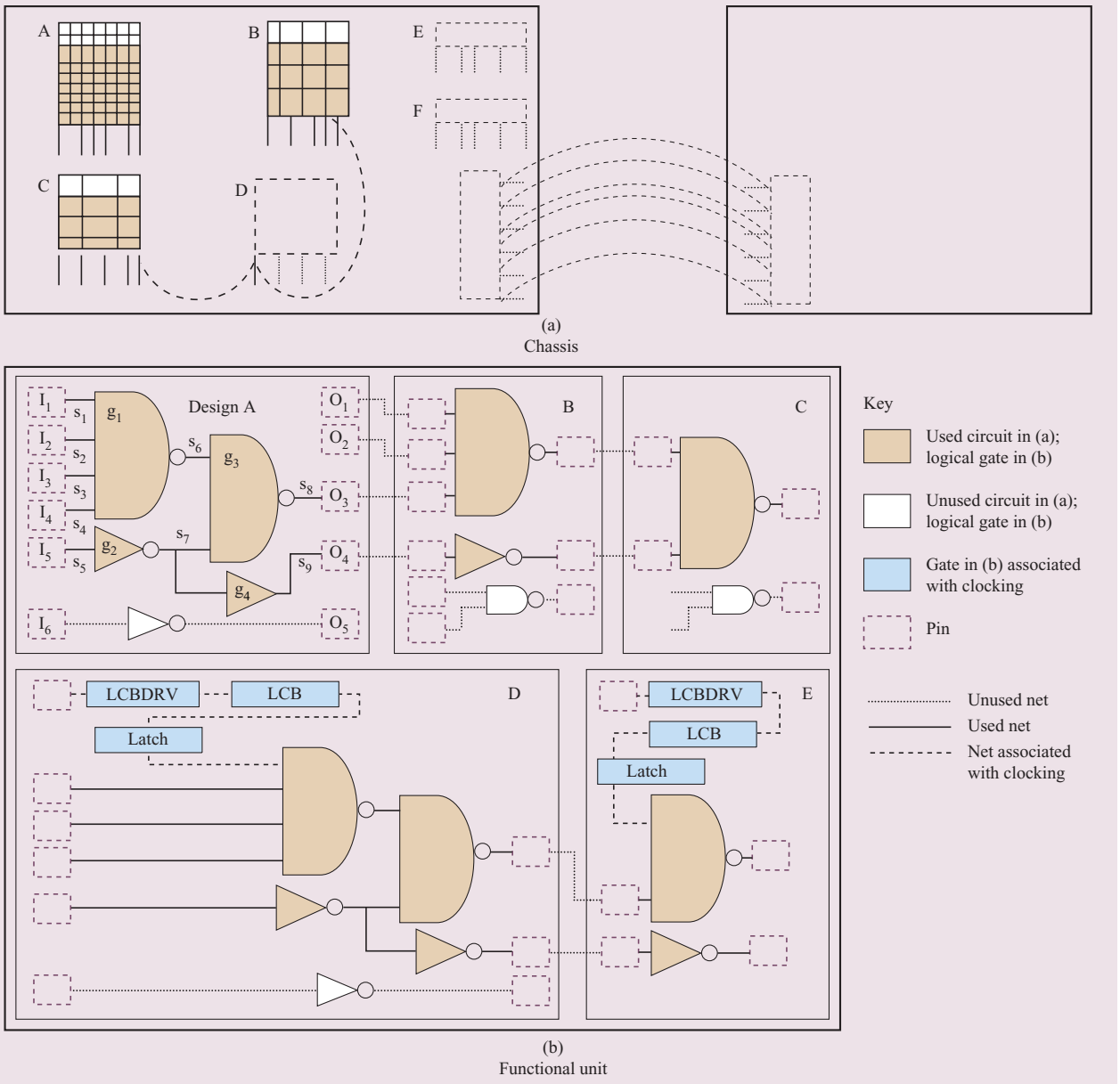


Figure 3

Schematics of (a) computer hardware described by Rent in the memoranda and (b) today's computer circuitry. LCBDRV refers to a local clock buffer driver, and LCB to a local clock buffer. The four gates in Design A in (b) are labeled g_1, g_2, g_3, g_4. The nine signals in this design are labeled s_1, ⋯, s_9, the inputs I_1, ⋯, I_6, and outputs O_1, ⋯, O_5. ©2004 IEEE. Reprinted from [13] with permission.

page 787, but with the addition of this new data. Note that a solid line also connects the two datapoints *C1* and *single card unit logic (IO pins)* in the plot of page 791, and that the locations of the datapoints *A7*, *A8*, *B1*, and *B2* are identified on the plot. In this later memo, Rent writes (page 789) that *It should be noted that these chassis points are quite scattered on the graph but still they fall between the curve for compact cards and the curve derived from 1410 chassis counts*, and that *These chassis counts verify that the curve drawn from the 1410 counts when used would not pin limit the mother board*, which indicates that the results in the first memo are verified by the results in the second memo.

Figure 3(a), prepared by the authors of this paper, is a schematic representation of a computer hardware chassis and the computer components described in the

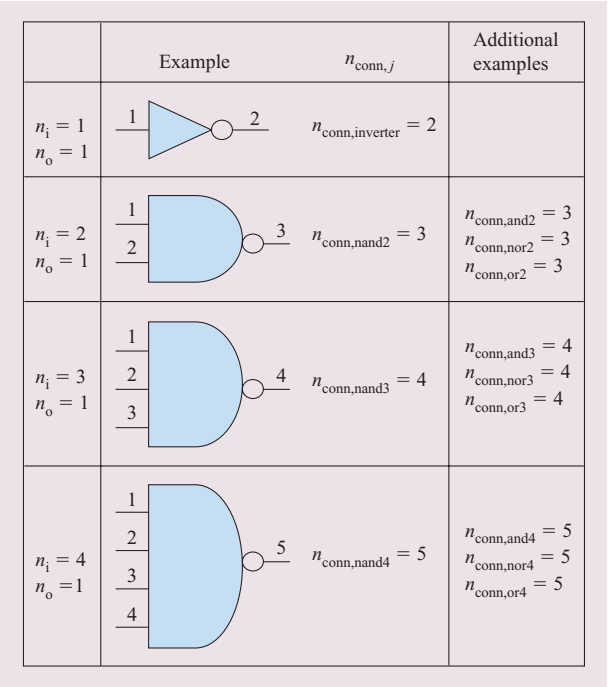


Figure 4

Number of connections $n_{conn,j}$ for a selection of gate types j. The number of connections for other gate types can be calculated by taking the sum of the number of inputs n_i and the number of outputs n_o, such that $n_{conn,j} = n_i + n_o$.

memoranda. The chassis shown in the figure contains six cards; three cards are used (A, B, C), and three cards are unused (D, E, F). Specifically, card A is a representation of the card shown in Figure 2(a), and the chassis is a representation of the chassis shown in Figure 2(b). In Figure 3(a), the dashed curved lines between the two chassis represent that these connections are excluded in Rent's calculations.

An interpretation for ULSI circuitry

Based on the previous section, the personal knowledge of one of us (R. A. Rand) of the 1401 and 1410 computers, and our experience with the design and analysis of ULSI circuitry for high-performance microprocessors [10, 99, 100], we have derived an *historically equivalent interpretation* of Rent's memoranda that is suitable for today's computer components. In this paper, the phrase *historically equivalent* refers to our mapping of each component described by Rent in the phrases for *circuit count* and *edge connector count*, as provided in the previous section, to a functionally equivalent component that exists in today's circuitry [13].

Figure 3(b) shows a schematic representation of today's computer circuitry. In Design A, shown in the figure, all inputs have unity fan-out, the used signals are labeled with notation $\{s_1, \cdots, s_9\}$, and the used gates are labeled with notation $\{g_1, \cdots, g_4\}$.

For today's designs, the historically equivalent terms for chassis and card are *functional unit* and *design*, respectively. The historically equivalent term for the building block, or circuit, is *logic gate*. The historically equivalent term for circuit count is *gate count*, which can be represented by the term N_{gates}, a quantity that describes the number of gates in a design. An expression for N_{gates} can be written according to the expression

$$N_{gates} = N_{all} - N_{unconnected} - N_{spare} - N_{filler} - N_{decap}\,, \qquad (4)$$

where the term N_{all} represents the total number of gates in a design, the term $N_{unconnected}$ represents the number of unconnected gates, the term N_{spare} represents the number of gates associated with spare logic, the term N_{filler} represents the number of filler cells, and the term N_{decap} represents the number of decoupling capacitors. To ensure an accurate count of N_{gates}, it is important to itemize carefully the contributions to the four terms $N_{unconnected}$, N_{spare}, N_{filler}, N_{decap} in Equation (4). These four terms do not contribute to the number of functional gates in a design, although they may exist for various reasons [13].

The historically equivalent term for *edge connector count* is *used connection*, which can be represented with the term N_{conn} and can be written [13] as

$$N_{conn} = \sum_{i=1}^{N_{nets}} (F_i + 1) - T_{IO} = F_{total} + N_{nets} - T_{IO}\,, \qquad (5)$$

where the sum is taken over the signal nets N_{nets}, F_i represents the fan-out of each signal net, T_{IO} represents the number of input pins and output pins in the design [5], and the total fan-out, F_{total}, is given by the expression

$$F_{total} = \sum_{i=1}^{N_{nets}} F_i\,.$$

In Equation (5), the term $(F_i + 1)$ represents the total number of connections made by a single signal net in a design; each signal net has a single driver and can have fan-out $F_i \geq 1$. Note that Equation (5) implicitly contains information about design complexity through the dependence of the historically equivalent Rent parameters k_R and p_R on the average fan-out f, which can be written as $f = F_{total}/N_{nets}$, since values for the Rent parameters $\{k_R, p_R\}$ are obtained through least-square linear fits to log–log plots of N_{conn} as a function of N_{gates}.

For the case of Design A in Figure 3(b), the value of $N_{gates} = 4$. The value for N_{conn} is obtained with Equations (4) and (5), where $N_{gates} = 4$, $F_{total} = 10$, $N_{nets} = 9$, and $T_{IO} = 7$. Substituting these values into Equation (5), we obtain the number of connections for Design A as

Table 3 Number of connections for five designs in [13] with Equation (6), where the coefficients in each equation are given in Figure 4 in this paper.

Design	*Reference*	N_{conn} *value*	*Gate allocation*	N_{conn}, *with Equation (6)*
A	Figure 3 in [13]	12	$N_{inv} = 2$	$N_{conn,A} = 2N_{inv} + 5N_{nand4} + 3N_{nand2}$
			$N_{nand2} = 1$	
			$N_{nand4} = 1$	
F	Figure 4 in [13]	24	$N_{inv} = 6$	$N_{conn,F} = 2N_{inv} + 3N_{nand2} + 3N_{nor2} + 3N_{and2}$
			$N_{nand2} = 1$	
			$N_{nor2} = 1$	
			$N_{and2} = 2$	
F1	Figure 5 in [13]	4	$N_{inv} = 2$	$N_{conn,F1} = 2N_{inv}$
F2	Figure 5 in [13]	9	$N_{and2} = 2$	$N_{conn,F2} = 3N_{and2} + 3N_{or2}$
			$N_{or2} = 1$	
F3	Figure 5 in [13]	11	$N_{inv} = 4$	$N_{conn,F3} = 2N_{inv} + 3N_{nand2}$
			$N_{nand2} = 1$	

$N_{conn,A} = 12$, as can be verified by a direct count of the connections in Design A. Additional examples of designs with inputs that have multiple fan-outs and designs that are partitioned into several subdesigns are given in [13].

A second method of obtaining the number of connections N_{conn} in a design is to count the number of gates N_j of each logic type j, such as the inverter (`inv`) and `nand2`. The total number of connections N_{conn} can also be written according to the expression,

$$N_{conn} = \sum_{j=1}^{G} n_{conn,j} \cdot N_j , \tag{6}$$

where $n_{conn,j}$ represents the number of connections of gates of type j, and where the sum is taken over all of the gate types G in a design. Note that the total number of gates N_{gates} can be written as the expression

$$N_{gates} = \sum_{j=1}^{G} N_j . \tag{7}$$

Examples of the number of connections per gate $n_{conn,j}$ are shown in **Figure 4**. The number of connections for a gate type j can be calculated by taking the sum of the number of inputs n_i and the number of outputs n_o, such that $n_{conn,j} = n_i + n_o$.

As an example, we consider the case of Design A shown in Figure 3(b). Design A contains three types of logic gates: `inv`, `nand2`, and `nand4`. From Figure 4, we see that each `inv` contributes two connections, each `nand2` contributes three connections, and each `nand4` contributes five connections. With these substitutions, Equation (6) takes the form for the number of connections for Design A, $N_{conn,A}$, as the expression

$$N_{conn,A} = 2 \cdot N_{inv} + 3 \cdot N_{nand2} + 5 \cdot N_{nand4} . \tag{8}$$

Next, Figure 3(b) shows that the number of `inv` is $N_{inv} = 2$, the number of `nand2` is $N_{nand2} = 1$, and the number of `nand4` is $N_{nand4} = 1$. Substituting these values into Equation (8), we obtain $N_{conn,A} = 12$, which is the same value previously obtained with Equation (5), as described above.

Additional examples for Designs F, F1, F2, and F3 in [13] are shown in **Table 3** [13]. This table shows the value for N_{conn} and the allocation of gates in each design for each of the different gate types: `inv`, `nand2`, `nand4`, `nor2`, `and2`, and `or2`. Equation (6) can be evaluated for each design, with Figure 4, to obtain the expressions for each design:

$$N_{conn,F} = 2 \cdot N_{inv} + 3 \cdot N_{nand2} + 3 \cdot N_{nor2} + 3 \cdot N_{and2} , \tag{9}$$

$$N_{conn,F1} = 2 \cdot N_{inv} , \tag{10}$$

$$N_{conn,F2} = 3 \cdot N_{and2} + 3 \cdot N_{or2} , \tag{11}$$

$$N_{conn,F3} = 2 \cdot N_{inv} + 3 \cdot N_{nand2} . \tag{12}$$

In this paper, the parameters k_R and p_R represent the inverse log of the intercept and the slope, respectively, of a linear fit to N_{conn} as a function of N_{gates} in a log–log plot, according to the expression

$$\log(N_{conn}) = \log(k_R) + p_R \cdot \log(N_{gates}) , \tag{13}$$

which can also be expressed as

$$N_{\text{conn}} = k_{\text{R}} \cdot N_{\text{gates}}^{p_{\text{R}}} . \tag{14}$$

Each datapoint in such a plot is generated from one design within a functional unit, and the series of datapoints considered for a fit according to Equation (14) is generated from the set of all designs within the unit.

An inspection of Equation (6) shows that N_{conn} tends to increase linearly with N_{gates} for 1) the case in which each design in a set of designs is composed of the same type of gate, 2) the case in which each design in a set of designs contains the same allocation of gates, and 3) the case in which one gate type is the primary constituent of all of the designs in the group. For example, consider a set of designs {a, b, c} in which all of the designs are composed of a different number of `nand2` gates. For these designs, the number of connections can be written in a straightforward fashion as the expressions

$$N_{\text{conn,a}} = 3 \cdot N_{\text{nand2}} , \tag{15}$$

$$N_{\text{conn,b}} = 3 \cdot N_{\text{nand2}} , \tag{16}$$

$$N_{\text{conn,c}} = 3 \cdot N_{\text{nand2}} , \tag{17}$$

where the terms $N_{\text{conn,a}}$, $N_{\text{conn,b}}$, and $N_{\text{conn,c}}$ represent the number of connections in designs a, b, and c, respectively, and the term N_{nand2} represents the number of `nand2`. A plot of these three datapoints would produce an exponent with value $p_{\text{R}} = 1$.

As a second example, consider a set of designs {d, e, f} in which all of the designs contain the same proportion of gates, such as 80% `inv`, 15% `nand2`, and 5% `nand4` gates, or 30% `inv`, 30% `nand2`, and 40% `nor2`. For the first example of these designs, the number of connections can be written as the expressions,

$$\begin{aligned} N_{\text{conn,d}} &= 2 \cdot N_{\text{inv}} + 3 \cdot N_{\text{nand2}} + 5 \cdot N_{\text{nand4}} \\ &= \{2 \cdot 0.80 + 3 \cdot 0.15 + 5 \cdot 0.05\} N_{\text{gates}} , \end{aligned} \tag{18}$$

$$\begin{aligned} N_{\text{conn,e}} &= 2 \cdot N_{\text{inv}} + 3 \cdot N_{\text{nand2}} + 5 \cdot N_{\text{nand4}} \\ &= \{2 \cdot 0.80 + 3 \cdot 0.15 + 5 \cdot 0.05\} N_{\text{gates}} , \end{aligned} \tag{19}$$

$$\begin{aligned} N_{\text{conn,f}} &= 2 \cdot N_{\text{inv}} + 3 \cdot N_{\text{nand2}} + 5 \cdot N_{\text{nand4}} \\ &= \{2 \cdot 0.80 + 3 \cdot 0.15 + 5 \cdot 0.05\} N_{\text{gates}} , \end{aligned} \tag{20}$$

where the term N_{gates} represents the total number of gates. An inspection of the expressions in Equations (18)–(20) shows that they can be written in the same form as Equations (15)–(17), as shown on the right-hand side of the expressions above. The expressions also show that, for these designs, the number of connections increases linearly with the number of gates; for this case, it is expected that the exponent has value $p_{\text{R}} = 1$ and that the uncertainty in the value of the exponent is zero.

For the cases in which other sets of designs contain similar allocation of gates in each design, it is expected that the exponent will also tend to approximate unity, with $p_{\text{R}} \sim 1$ with a low value of uncertainty in the value of p_{R}. For other cases in which the designs contain disparate allocations of gates in each design, it is expected that the expressions for the number of connections in each design will take on a more complicated relationship for the designs; for these cases, the value of the exponent is obtained from the log–log plot, and it is expected that the uncertainty in the value of the exponent will increase.

Application to wire-length distribution models

This section presents an application of the interpretation of microminiature packaging described in the previous section to the problem of interconnection requirements in ULSI circuitry [13]. The designs selected for this study are all of the control logic designs in the IBM POWER4 core [95]. Here, the goal is to obtain improved estimates of wire-length requirements for circuitry on ULSI chips. A discussion of the limitations of these wiring estimates and a comparison with prior work are presented in [13].

For each design, estimates and ranges for the normalized probability density function $p_{\text{int}}(L)$, cumulative distribution function $P(L)$, average wire length $L_{\text{avg}}(p_{\text{R}})$, and total wire length $L_{\text{tot}}(p_{\text{R}})$ are obtained. To obtain these estimates, we first extract values for the parameters $\{k_{\text{R}}, p_{\text{R}}\}$ for the designs in each functional unit with Equation (13). As discussed in an earlier section, each design provides one datapoint on the log–log plot for each functional unit; for this datapoint, the value for N_{gates} takes into careful account the values of N_{all}, $N_{\text{unconnected}}$, N_{spare}, N_{filler}, and N_{decap}, and the value of N_{conn} is obtained from a count of F_{total}, N_{nets}, and T_{IO}.

Figure 5 shows a log–log plot of N_{conn} as a function of N_{gates} for each of the six units in the POWER4 core. For example, in this figure, the 18 datapoints for the IFU are provided by the 18 individual designs in the IFU. Linear fits of the design data to Equation (13) for each unit provide the appropriate values of $\{k_{\text{R}}, p_{\text{R}}\}$, where the value of k_{R} falls roughly in the range of 1 to 4, as shown in **Table 4** [10] and $p_{\text{R}} \sim 1$. Complete listings of the estimates and ranges within one standard deviation for k_{R} and p_{R} are given in [13]. For comparison, Table 4 also lists the values of the Rent parameters $\{k, p\}$ that are obtained with the external interpretation of Rent's memoranda [1, 5–8, 10]. The results in Table 4 show that the value of p_{R} is close to unity for each of the six functional units in the core, which suggests that the number of connections in all of the designs in the core tends to increase linearly with the number of gates. Since these

designs are composed mainly of `inv`, the choices of gates in all of the designs are generated with the same set of sophisticated computer-aided design (CAD) software programs, and since it has been observed that designs that contain both one type of gate and a similar gate allocation are expected to exhibit a linear dependence of the number of connections as a function of the number of gates, as discussed in a previous section, it is expected that $p_R \sim 1$.

Table 5 [5] compares the values of the average wire-length estimates $L_{ave}(p_R)$ obtained with the Davis model [5] for each design with the measured average wire length L_a and with the prior estimate $L_{ave}(p)$ for the control logic designs in the POWER4 IFU. Table 4 compares the total wire-length estimate $L_T(p_R)$ for each design with the measured total wire length L_T and with the prior estimate $L_T(p)$, where $L_T(p_R)$ and $L_T(p)$ are given by the expressions,

$$L_T(p_R) = N_{nets} \times L_{avg}(p_R),$$

$$L_T(p) = N_{nets} \times L_{avg}(p), \tag{21}$$

where the term N_{nets} represents the number of connected nets in the design. Table 4 compares estimates of the total wire length $L_{tot}(p_R)$ in the entire POWER4 core with the measured requirement and with the prior estimate $L_{tot}(p)$, where $L_{tot}(p_R)$ and $L_{tot}(p)$ are given by the expressions,

$$L_{tot}(p_R) = \sum_{j=1}^{N_{designs}} N_{nets}^{j} \times L_{avg}^{j}(p_R),$$

$$L_{tot}(p) = \sum_{j=1}^{N_{designs}} N_{nets}^{j} \times L_{avg}^{j}(p), \tag{22}$$

where the sums are taken over all control logic designs $N_{designs}$ in each unit, $L_{avg}^{j}(p_R)$ represents the average wire length provided for design j by the Davis model [5] as a function of p_R, $L_{avg}^{j}(p)$ represents the average wire-length estimate for design j provided by the Davis model evaluated as a function of p, and N_{nets}^{j} represents the number of connected nets in design j.

The results presented in Tables 4 and 5 show that the estimates obtained by evaluating the expressions in the models as functions of $\{k_R, p_R\}$ show improved agreement with the real wire-length requirements compared with the agreement obtained with prior

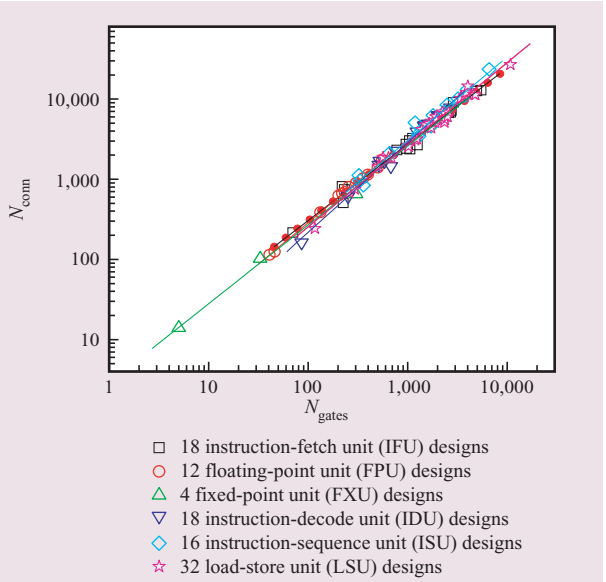


Figure 5

Number of used connections N_{conn} as a function of used gates N_{gates} for 100 control logic designs in the six units in the POWER4 core. Linear fits to the data provide values of the parameter pair $\{k_R, p_R\}$ for each unit and are listed in Table 4. ©2004 IEEE. Reprinted from [13] with permission.

Table 4 Values of the parameter pairs $\{k, p\}$ and $\{k_R, p_R\}$for the six POWER4 functional units [10]. Comparisons of the measured wire-length requirements L_T with estimates $L_{tot}(p)$ and $L_{tot}(p_R)$ are also shown for each unit. Wire lengths are shown in gate pitches. The range for the estimates is shown in brackets.

Unit	k	p	k_R	p_R	L_T	$L_{tot}(p)$ *[range] (Error*[a]*)*	$L_{tot}(p_R)$ *[range] (Error*[b]*)*
IFU	0.79	0.69	3.82	0.95	226,826.9	141,256.9 [106,962.1, 192,256.1] (−38)	249,497.0 [234,517.7, 265,301.2] (10)
FPU	2.21	0.66	2.4	1.03	21,915.9	11,886.8 [10,244.9, 13,999.2] (−46)	19,046.1 [18,685.9, 19,412.3] (−13)
FXU	4.36	0.61	2.91	0.98	26,030.9	10,380.8 [8,991.9, 12,140.4] (−60)	21,818.4 [20,098.3, 23,659.3] (−16)
IDU	20.5	0.30	1.24	1.12	148,700.6	59,240.1 [52,017.7, 69,503.6] (−60)	243,123.7 [230,804.0, 255,815.9] (63)
ISU	23.3	0.31	2.31	1.04	309,901.8	92,190.1 [77,970.2, 114,605.0] (−70)	390,247.9 [356,529.6, 426,134.9] (26)
LSU	7.33	0.46	2.28	1.02	553,852.8	220,556.9 [183.878.7, 274,265.0] (−60)	747,767.6 [709,590.4, 787.415.6] (35)
Core	—	—	—	—	1.29×10^6	535,511.6 [440,066.5, 676,769.3] (−58)	1.67×10^6 [1.57×10^6, 1.78×10^6] (30)

[a] $E[L_{tot}(p)]\ (\%) = 100 \cdot [L_{tot}(p) - L_T]/L_T$ [b] $E[L_{tot}(p_R)]\ (\%) = 100 \cdot [L_{tot}(p_R) - L_T]/L_T$

Table 5 Comparison of the estimate of the measured average wire length L_a and L_T (in gate pitches) for 18 IFU designs with average wire-length estimates obtained with the Davis model [5]. Wire lengths are given in gate pitches. Ranges for the estimates are shown in brackets.

IFU	L_a	$L_{avg}(p)$ *[range] (Error[a])*	$L_{avg}(p_R)$ *[range] (Error[b])*	L_T	$L_T(p)$ *(Error[c])*	$L_T(p_R)$ *[range] (Error[d])*
i1	3.3	2.4 [2.2, 2.6] (−28)	2.8 [2.8, 2.9] (−13)	305.5	220.5 [201.3, 243.2] (−28)	264.7 [259.3, 270.1] (−13)
i2	5.5	3.0 [2.6, 3.5] (−46)	3.9 [3.8, 4.1] (−28)	1,745.8	944.4 [822.1, 1,098.0] (−46)	1,249.8 [1,211.5, 1,289.4] (−28)
i3	4.2	3.0 [2.6, 3.5] (−29)	4.0 [3.8, 4.1] (−5)	847.6	605.6 [526.6, 704.9] (−29)	803.1 [778.3, 828.8] (−5)
i4	4.0	3.0 [2.6, 3.5] (−24)	4.0 [3.9, 4.1] (0)	1,011.2	764.7 [664.1, 891.3] (−24)	1,016.7 [985.0, 1,049.4] (1)
i5	3.7	3.8 [3.1, 4.8] (2)	5.8 [5.5, 6.0] (54)	2,999.5	3,063.3 [2,500.1, 3,826.1] (2)	4,623.4 [4,418.9, 4,836.7] (54)
i6	6.2	4.0 [3.2, 5.1] (−36)	6.2 [5.9, 6.5] (−1)	6,218.3	3,982.3 [3,211.3, 5,041.1] (−36)	6,159.2 [5,871.5, 6,459.8] (−1)
i7	5.7	4.0 [3.2, 5.1] (−29)	6.2 [5.9, 6.5] (10)	4,731.2	3,348.7 [2,699.9, 4,239.9] (−29)	5,181.1 [4,938.9, 5,434.2] (10)
i8	4.1	4.1 [3.3, 5.2] (0)	6.3 [6.0, 6.7] (56)	4,261.1	4,269.2 [3,427.3, 5,431.2] (0)	6,663.1 [6,345.9, 6,994.9] (56)
i9	4.8	4.1 [3.3, 5.2] (−16)	6.4 [6.1, 6.7] (32)	4,472.9	3,769.5 [3,024.3, 4,798.8] (−16)	5,890.5 [5,609.3, 6,184.6] (32)
i10	3.6	4.1 [3.3, 5.3] (14)	6.5 [6.2, 6.8] (80)	4,140.6	4,726.3 [3,778.8, 6,040.3] (14)	7,438.1 [7,077.7, 7,815.1] (80)
i11	4.2	4.2 [3.3, 5.4] (1)	6.7 [6.4, 7.1] (61)	4,312.9	4,341.7 [3,448.7, 5,589.4] (1)	6,924.2 [6,579.5, 7,285.1] (61)
i12	9.3	4.8 [3.7, 6.4] (−49)	8.2 [7.8, 8.7] (−11)	19,794.9	10,193.4 [7,795.5, 13,691.2] (−49)	17,556.1 [16,549.2, 18,615.9] (−11)
i13	9.5	4.9 [3.7, 6.6] (−49)	8.5 [8.0, 9.0] (−11)	21,765.9	11,159.9 [8,481.9, 15,094.0] (−49)	19,464.1 [18,323.9, 20,665.0] (−11)
i14	7.0	4.9 [3.7, 6.7] (−30)	8.7 [8.1, 9.2] (23)	16,555.1	11,623.6 [8,806.3, 15,777.1] (−30)	20,403.4 [19,195.5, 21,676.2] (23)
i15	8.1	4.9 [3.7, 6.7] (−39)	8.7 [8.2, 9.3] (7)	20,318.6	12,374.6 [9,363.1, 16,821.1] (−39)	21,779.1 [20,484.2, 23,143.9] (7)
i16	10.4	5.0 [3.8, 6.8] (−52)	8.8 [8.3, 9.4] (−15)	31,544.6	15,215.2 [11,479.4, 20,749.2] (−52)	26,934.8 [25,318.2, 28,639.2] (−15)
i17	8.7	5.6 [4.1, 7.9] (−36)	10.6 [9.9, 11.4] (22)	38,034.0	24,362.2 [17,730.2, 34,593.6] (−36)	46,383.4 [43,276.3, 49,674.5] (22)
i18	9.5	5.7 [4.1, 8.2] (−40)	11.0 [10.3, 11.8] (16)	43,767.3	26,291.6 [19,002.1, 37,625.6] (−40)	50,762.3 [47,294.7, 54,438.6] (16)

[a] $E[L_{avg}(p)]\ (\%) = 100 \cdot \{[L_{avg}(p) - L_a]/L_a\}$
[b] $E[L_{avg}(p_R)]\ (\%) = 100 \cdot \{[L_{avg}(p_R) - L_a]/L_a\}$
[c] $E[L_T(p)]\ (\%) = 100 \cdot \{[L_T(p) - L_T]/L_T\}$
[d] $E[L_T(p_R)]\ (\%) = 100 \cdot \{[L_T(p_R) - L_T]/L_T\}$

estimates [10]. Note that the estimates are within 10% of L_T for the IFU. Wire-length estimates are also improved [10, 13] for the designs in the other five units; specifically, wire-length estimates are improved for 13 of 18 IFU designs, all 12 FPU designs, 3 of 4 FXU designs, 10 of 18 IDU designs, 14 of 16 ISU designs, and 28 of 32 LSU designs, compared with prior work.

Table 4 shows that when all of the designs in the POWER4 core are considered as a group, the wire-length estimate for the interconnection requirement in the core is within 30% of the measured requirement. This result also compares favorably with the result obtained in prior work in which agreement between the estimate of total wire length is within 58% of the total wire-length measurement [10].

We now discuss the wire-length requirements for one design, i9, in the IFU. The area occupancy [100] of the design is 74%, which is near the median occupancy of all of the IFU designs; here the term *area occupancy* refers to the ratio of the area occupied by the used gates to the total area allocated to the design in the silicon die, as described in [100]. **Figure 6** shows a histogram of the area occupancy of all 18 IFU designs. The area occupancy of the IFU designs ranges from 28% to 85%, with a mean occupancy of 65%.

Figure 7 compares measurements and estimates of the normalized probability density function $p_{int}(L)$ and cumulative distribution function $P(L)$ for design i9. In this figure, the estimates are provided by the Davis model [5–7] as functions of the parameter pairs $\{k, p\}$ and $\{k_R, p_R\}$, where the measured values of $p_{int}(L)$ are shown with solid circles and the measured values of $P(L)$ are shown with hollow squares. The dotted lines indicate distributions that are obtained by evaluating the Davis model as functions of $\{k, p\}$ [10], and where the upper range and lower range are obtained with the values for the ranges of k and p. The solid lines indicate the distributions that are obtained by evaluating the Davis model as functions of the historically equivalent Rent parameters $\{k_R, p_R\}$. The figure shows that the curves obtained with $\{k_R, p_R\}$ exhibit qualitatively better agreement with the measured curves compared with the curves obtained with parameter pair $\{k, p\}$ [10].

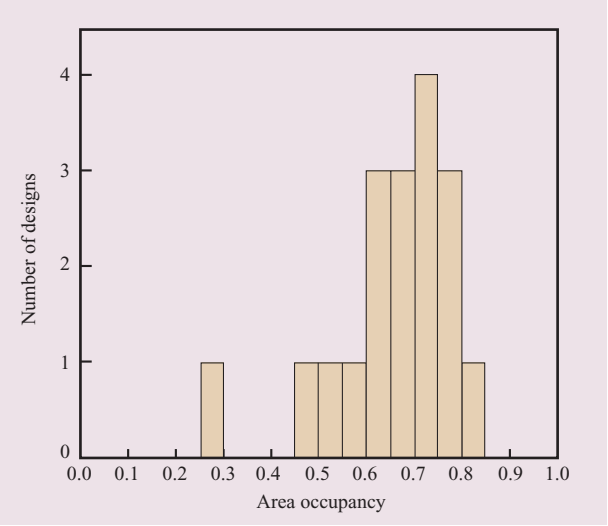


Figure 6

Distribution of the area occupancy of IFU designs.

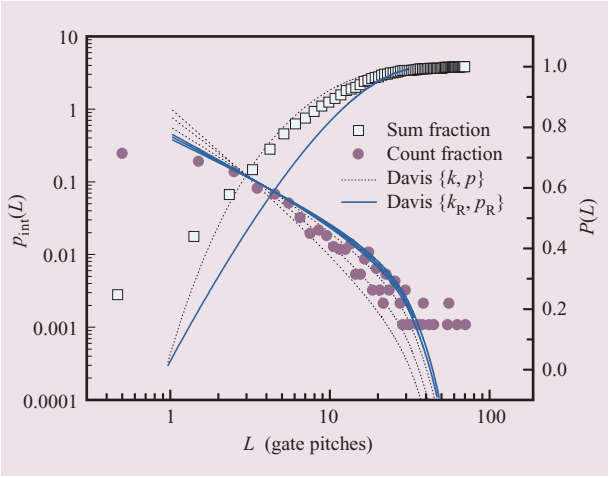


Figure 7

Normalized probability density function $p_{int}(L)$ (solid circles) and cumulative distribution function $P(L)$ (hollow squares) for design i9 in the POWER4 IFU. The dotted lines represent the distributions obtained for $p_{int}(L)$ (shown on the left-hand ordinate) and $P(L)$ (shown on the right-hand ordinate) by evaluating expressions provided by the Davis model [5–7] as functions of the parameter pair $\{k, p\}$. The solid lines represent the curves for $p_{int}(L)$ and $P(L)$ obtained by evaluating expressions provided by the Davis model as functions of the parameter pair $\{k_R, p_R\}$ [13]. ©2004 IEEE. Reprinted from [13] with permission.

Discussion

The approach presented in this paper is intended to provide information for future research and additional applications of Rent's work. To date, Rent's work has been referenced in research and development of a variety of scientific and technical fields, including the following: on-chip interconnections, semiconductor circuitry, computer systems design, applied sciences, and semiconductor manufacturing technology. Examples of applications in each of these fields were provided in an earlier section of this paper. With Rent's work now available in the literature, one is able to study the original sources within the context of the development of computer hardware components. Because prior work was based on the 1971 interpretation of the two Rent memoranda and because significant changes have occurred in the development of computer systems hardware since Rent wrote the two memoranda in 1960, it is necessary to provide an interpretation of these memoranda that is suitable for today's ULSI circuitry.

For the example of on-chip interconnections in ULSI circuitry described in this paper, this approach provides chip designers with techniques to obtain wire-length estimates and distributions that exhibit improved agreement with measured interconnection requirements. These methods help achieve the goal of buildable and functional chip designs in spite of increasingly severe chip-design constraints that include the following: restrictive real-estate specifications, the limited number of metal layers available in the manufacturing technology, aggressive operating frequencies, and power dissipation limits [4, 42, 48, 49, 61–63, 70].

In principle, the development of an interpretation of the memoranda that is applicable for today's ULSI circuitry is essentially the development of a technique to describe more generally the connectivity of nanoscale components, of which integrated circuitry is one specific example. This paper has presented a description of the connectivity of nanoscale components in the silicon brain, where the term *silicon brain* refers to the high-performance central processing unit (CPU) that contains the specific chip designs examined in this study. Note that this interpretation does not concern itself with the two-dimensional nature of chip layouts, since this constraint is imposed by the current manufacturing processes. Thus, the interpretation of connectivity presented in this paper can, in principle, be applied to descriptions of connectivity in other complex systems; these systems include, for example, the connectivity in the human brain [101–104].

Considered as a complex circuit, the design of the human brain can be described as a network of neurons in conjunction with chemicals that enable a progression of electrical signals and chemical signals to connect the appropriate set of neurons. One may relate the components of the silicon brain and the human brain with the following mapping: The term *circuit* is understood to be the logic gate in the silicon brain and

the neuron in the human brain; the term *interconnection* is understood to be the wire in the silicon brain and axons in the human brain; the signal inputs are the logic gate inputs in the silicon brain and dendrites in the human brain; the signal outputs are the logic gate outputs in the silicon brain and axon synaptic knobs in the human brain. Specifically, the interpretation for nanoscale components described in this paper provides a technique to quantify the connectivity in the human brain at the neuron level, for example to quantify differences among different brain regions and to distinguish different stages of development, aging, and disease that occur as the result of neural degradation, such as Alzheimer's disease, for which the underlying cause remains unknown at this time.

In this example, this mapping suggests that values of the Rent parameters to quantify the connectivity of components in each region of the human brain can be obtained with the following steps: First, the neurons in one region of the brain are grouped into subregions of neurons; second, a count is obtained of the number of dendrites and axon synaptic knobs and the number of neurons in each subregion; third, the number of potential connections (sum of the number of dendrites and axon synaptic knobs) is plotted on a log–log plot as a function of the number of neurons for each subregion; fourth, a least-square linear fit is made to the graphed data, and the empirical values of the Rent parameters can be extracted from the fit parameters, where the value of the Rent exponent is the value of the slope of the line, and the value of the Rent coefficient is the value of the inverse log of the intercept. Cox–Golgi preparations may provide one technique to visualize these components (neurons, axons, and dendrites) [101–104]. One may use values of the Rent parameters in each region of a normal human brain as a basis for comparison with the corresponding region in other human brains to establish baselines for and quantify the progression of different stages of development, aging, and disease.

Conclusions

To provide background for the extensive body of research based on a 1971 interpretation of the work of E. F. Rent and to satisfy requests from researchers for these memoranda, this paper presents the original work of Rent and an historically equivalent interpretation of these memoranda that is suitable for today's computer hardware components. The interpretation that we introduce for today's computer components is needed because computer components have changed significantly compared with the discrete-transistor-based hardware components that are considered in Rent's original work. This paper also applies this interpretation to existing on-chip wire-length distribution models and presents estimates of interconnection requirements that demonstrate improved agreement to within 30% with actual wire-length requirements compared with prior methods, which obtained agreement with measurements to within 58%.

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References

1. B. S. Landman and R. L. Russo, "On a Pin Versus Block Relationship for Partitions of Logic Graphs," *IEEE Trans. Computers* **C-20**, No. 12, 1469–1479 (December 1971).
2. "International Technology Roadmap for Semiconductors (ITRS)," 2003 edition, Semiconductor Industry Association (SIA); see *http://public.itrs.net/*.
3. D. P. Seraphim and I. Feinberg, "Electronic Packaging Evolution in IBM," *IBM J. Res. & Dev.* **25**, No. 5, 617–629 (September 1981).
4. H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley Publishing Co., Reading, MA, 1990; ISBN 0-201-06008-6.
5. J. A. Davis, V. K. De, and J. D. Meindl, "A Stochastic Wire-Length Distribution for Gigascale Integration (GSI). I. Derivation and Validation," *IEEE Trans. Electron Devices* **45**, No. 3, 580–589 (March 1998).
6. J. A. Davis, V. K. De, and J. D. Meindl, "A Stochastic Wire-Length Distribution for Gigascale Integration (GSI). II. Applications to Clock Frequency, Power Dissipation, and Chip Size Estimation," *IEEE Trans. Electron Devices* **45**, No. 3, 590–597 (March 1998).
7. J. A. Davis, "A Hierarchy of Interconnect Limits and Opportunities for Gigascale Integration (GSI)," Ph.D. thesis, Georgia Institute of Technology, 1999.
8. J. Dambre, P. Verplaetse, D. Stroobandt, and J. V. Campenhout, "A Comparison of Various Terminal-Gate Relationships for Interconnect Prediction in VLSI Circuits," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **11**, No. 1, 24–34 (February 2003).
9. P. Christie and D. Stroobandt, "The Interpretation and Application of Rent's Rule," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **8**, No. 6, 639–648 (December 2000).
10. M. Y. Lanzerotti, G. Fiorenza, and R. Rand, "Assessment of On-Chip Wire-Length Distribution Models," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **12**, No. 10, 1108–1112 (October 2004).
11. J. Dambre, "Prediction of Interconnect Properties for Digital Circuit Design and Exploration," Ph.D. dissertation, University of Ghent, Belgium, July 2003.

12. P. Verplaetse, D. Stroobandt, and J. Van Campenhout, "A Stochastic Model for the Interconnection Topology of Digital Circuits," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **9**, No. 6, 938–942 (December 2001).
13. M. Y. Lanzerotti, G. Fiorenza, and R. A. Rand, "Interpretation of Rent's Rule for Ultralarge-Scale Integrated Circuit Designs, with an Application to Wirelength Distribution Models," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **12**, No. 12, 1330–1347 (December 2004).
14. W. E. Donath, "Placement and Average Interconnection Lengths of Computer Logic," *IEEE Trans. Circuits & Syst. (CAS)* **CAS-26**, No. 4, 272–277 (April 1979).
15. W. E. Donath, "Wire Length Distribution for Placements of Computer Logic," *IBM J. Res. & Dev.* **25**, No. 2/3, 152–155 (May 1981).
16. J. A. Davis, V. K. De, and J. D. Meindl, "Optimal Low Power Interconnect Networks," *Proceedings of the IEEE Symposium on VLSI Technology, Digest of Technical Papers*, 1996, pp. 78–79.
17. J. A. Davis, V. K. De, and J. D. Meindl, "A Priori Wiring Estimations and Optimal Multilevel Wiring Networks for Portable VLSI Systems," *Proceedings of the 46th Electronic Components and Technology Conference*, 1996, pp. 1002–1008.
18. J. A. Davis, V. K. De, and J. D. Meindl, "A Stochastic Wire Length Distribution for Gigascale Integration (GSI)," *Proceedings of the Custom Integration Circuits Conference (CICC)*, 1997, pp. 145–150.
19. J. D. Meindl, V. K. De, D. S. Wills, J. C. Eble, X. Tang, J. A. Davis, B. L. Austin, and A. J. Bhavnagarwala, "The Impact of Stochastic Dopant and Interconnect Distributions on Gigascale Integration," *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*, 1997, pp. 232–233.
20. W. R. Heller, "Wirability of Logic Circuit Packages in LSI and VLSI," *Proceedings of the 3rd IEEE International Computer Software and Applications Conference*, 1979, pp. 95–100.
21. W. R. Heller, "Contrasts in Physical Design Between LSI and VLSI," *Proceedings of the 18th IEEE Conference on Design Automation*, 1981, pp. 676–683.
22. W. R. Heller, C. G. Hsi, and W. F. Mikhaill, "Wirability—Designing Wiring Space for Chips and Chip Packages," *IEEE Design & Test Magazine* **1**, 43–51 (August 1984).
23. J. Dambre, D. Stroobandt, and J. Van Campenhout, "Fast Estimation of the Partitioning Rent Characteristic Using a Recursive Partitioning Model," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, 2003, pp. 45–52.
24. T. Ahonen, T. Nurmi, J. Nurmi, and J. Isoaho, "Block-Wise Extraction of Rent's Exponents for an Extensible Processor," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, 2003, pp. 193–199.
25. P. J. Koopman and D. P. Siewiorek, "The Impact of Rent's Rule on Massive Parallelism," *Proceedings of the 2nd Symposium on the Frontiers of Massively Parallel Computation (FMPC)*, 1988, pp. 59–62.
26. J. Dambre, P. Verplaetse, D. Stroobandt, and J. Van Campenhout, "On Rent's Rule for Rectangular Regions," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, 2001, pp. 49–56.
27. D. Stroobandt, "Multi-Terminal Nets Do Change Conventional Wire Length Distribution Models," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, 2001, pp. 41–48.
28. D. Stroobandt, "A Priori Wire Length Distribution Models for Multiterminal Nets," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **11**, No. 1, 35–43 (February 2003).
29. C.-K. Cheng, A. B. Kahng, L. Bao, and D. Stroobandt, "Toward Better Wireload Models in the Presence of Obstacles," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **10**, No. 2, 177–189 (April 2002).
30. M. Marek-Sadowska, "Interconnect Planning for Hierarchical FPGAs," Final Report 2002–2003 for MICRO Project 02-046, Collaborating Companies: Xilinx and Mentor Graphics, 2003; see *http://www.ucop.edu/research/micro/02_03/02_046.pdf*.
31. G. Parthasarathy, M. Marek-Sadowska, A. Mukherjee, and A. Singh, "Interconnect Complexity-Aware FPGA Placement Using Rent's Rule," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, 2001, pp. 115–121.
32. A. Rahman, S. Das, A. P. Chandrakasan, and R. Reif, "Wiring Requirement and Three-Dimensional Integration Technology for Field Programmable Gate Arrays," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **11**, No. 1, 44–54 (February 2003).
33. A. DeHon, "Balancing Interconnect and Computation in a Reconfigurable Computing Array (or, Why You Don't Really Want 100% LUT Utilization)," *Proceedings of the 7th International Symposium on Field-Programmable Gate Arrays (FPGA) Conference*, 1999, pp. 69–78.
34. A. DeHon, "Unifying Mesh- and Tree-Based Programmable Interconnect," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **12**, No. 10, 1051–1065 (October 2004).
35. M. deLorimier and A. DeHon, "Floating-Point Sparse Matrix-Vector Multiply for FPGAs," *Proceedings of the 13th International Symposium on Field-Programmable Gate Arrays (FPGA) Conference*, 2005, pp. 75–85.
36. J. W. Joyner, R. Venkatesan, P. Zarkesh-Ha, J. A. Davis, and J. D. Meindl, "Impact of Three-Dimensional Architectures on Interconnects in Gigascale Integration," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **9**, No. 6, 922–928 (December 2001).
37. J. W. Joyner, P. Zarkesh-Ha, and J. D. Meindl, "Global Interconnect Design in a Three-Dimensional System-on-a-Chip," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **12**, No. 4, 367–372 (April 2004).
38. S. Das, A. P. Chandrakasan, and R. Reif, "Calibration of Rent's Rule Models for Three-Dimensional Integrated Circuits," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.* **12**, No. 4, 359–366 (April 2004).
39. S. J. Souri, K. Banerjee, A. Mehrotra, and K. C. Saraswat, "Multiple Si Layer ICs: Motivation, Performance Analysis, and Design Implications," *Proceedings of the Design Automation Conference (DAC)*, 2000, pp. 213–220.
40. J. D. Meindl, J. A. Davis, P. Zarkesh-Ha, C. S. Patel, K. P. Martin, and P. A. Kohl, "Interconnect Opportunities for Gigascale Integration," *IBM J. Res. & Dev.* **46**, No. 2/3, 245–263 (March/May 2002).
41. H. Van Marck, D. Stroobandt, and J. Van Campenhout, "Interconnection Length Distributions in 3-dimensional Anisotropic Systems," *Proceedings of the 13th IASTED Conference on Applied Informatics*, 1995, pp. 98–101.
42. I. Young and K. Raol, "A Comprehensive Metric for Evaluating Interconnect Performance," *Proceedings of the IEEE International Interconnect Technology Conference*, 2001, pp. 119–121.
43. K. M. Buyuksahin and F. N. Najm, "High-Level Power Estimation with Interconnect Effects," *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, 2000, pp. 197–202.
44. P. Zarkesh-Ha, J. A. Davis, W. Loh, and J. D. Meindl, "Stochastic Interconnect Network Fan-Out Distribution Using Rent's Rule," *Proceedings of the IEEE International Interconnect Technology Conference (IITC)*, 1998, pp. 184–186.
45. P. Zarkesh-Ha, J. A. Davis, W. Loh, and J. D. Meindl, "Prediction of Interconnect Fan-Out Distribution Using Rent's Rule," *Proceedings of the International Workshop on System-Level Interconnect Prediction (SLIP)*, 2000, pp. 107–112.
46. X. Yang, R. Kastner, and M. Sarrafzadeh, "Congestion Estimation During Top-Down Placement," *Proceedings of*

the International Symposium on Physical Design (ISPD), 2001, pp. 164–169.
47. X. Yang, R. Kastner, and M. Sarrafzadeh, "Congestion Estimation During Top-Down Placement," *IEEE Trans. Computer-Aided Design Integrated Circuits & Syst.* **21**, No. 1, 72–80 (January 2002).
48. D. Stroobandt, "A Priori Wire Length Estimates Based on Rent's Rule," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, 1999, pp. 1–96.
49. D. Stroobandt, *A Priori Wire Length Estimates for Digital Design*, Kluwer Academic Publishers, Boston, 2001.
50. L. Hagen, A. B. Kahng, F. J. Kurdahi, and C. Ramachandran, "On the Intrinsic Rent Parameter and Spectra-Based Partitioning Methodologies," *IEEE Trans. Computer-Aided Design Integrated Circuits & Syst.* **13**, No. 1, 27–37 (January 1994).
51. C. J. Alpert, A. E. Caldwell, A. B. Kahng, and I. L. Markov, "Hypergraph Partitioning with Fixed Vertices," *IEEE Trans. Computer-Aided Design Integrated Circuits & Syst.* **19**, No. 2, 267–272 (February 2000).
52. A. DeHon, "Rent's Rule Based Switching Requirements," *Proceedings of the International Workshop on System-Level Interconnect Prediction (SLIP)*, 2001, pp. 197–204.
53. R. Tessier and H. Giza, "Balancing Logic Utilization and Area Efficiency in FPGAs," *Proceedings of the 10th International Conference on Field-Programmable Logic and Applications*, 2000, pp. 535–544.
54. P. M. B. Vitanyi, "Area Penalty for Sublinear Signal Propagation Delay on Chip," *Proceedings of the 26th Annual IEEE Symposium on Foundations of Computer Science*, 1985, pp. 197–207.
55. G. A. Sai-Halasz, "Performance Trends in High-End Processors," *Proc. IEEE* **83**, No. 1 20–36 (January 1995).
56. E. H. Dooijes, "Trends in Computer Technology," *Technical Report CS-94-17*, Department of Computer Systems, Faculty of Mathematics and Computer Science, University of Amsterdam, The Netherlands, November 1994 and October 1999.
57. J. R. Heath, "Wires, Switches, and Wiring. A Route Toward a Chemically Assembled Electronic Nanocomputer," *Pure Appl. Chem.* **72**, No. 1/2, 11–20 (2000); see *http://www.iupac.org/publications/pac/2000/7201/7201pdf/2_heath.pdf*.
58. R. W. Keyes, *The Physics of VLSI Systems*, Addison-Wesley Publishing Co., Reading, MA, 1986.
59. R. W. Keyes, "Fundamental Limits in Digital Information Processing," *Proc. IEEE* **69**, No. 2, 267–278 (February 1981).
60. R. W. Keyes, "The Evolution of Digital Electronics Towards VLSI," *IEEE Trans Electron Devices* **26**, No. 4, 271–279 (April 1979).
61. J. D. Meindl, "Opportunities for Gigascale Integration," *Solid State Technol.* **30**, 84–89 (December 1987).
62. M. T. Bohr, "Interconnect Scaling—The Real Limiter to High Performance ULSI," *Proceedings of the International Electron Devices Meeting*, 1995, pp. 241–244.
63. A. K. Stamper, "Interconnection Scaling 1 GHz and Beyond," *IBM MicroNews* **4**, No. 2, 1–12 (1998).
64. W. J. Dally, J. Poulton, and S. Tell, "Multi-Gigabit Signaling with CMOS," *Proceedings of the IEEE Conference on Lasers and Electro-Optics (LEOS)*, 1997.
65. J. E. Harlow III, "Toward Design Technology in 2020: Trends, Issues, and Challenges," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, 2003, pp. 3–4.
66. D. C. Schmidt, "Circuit Pack Parameter Estimation Using Rent's Rule," *IEEE Trans. Computer-Aided Design Integrated Circuits & Syst.* **1**, No. 4, 186–192 (October 1982).
67. Workshop on System-Level Interconnect Prediction (SLIP); see *http://www.sliponline.org*.
68. W. E. Donath, "Equivalence of Memory to Random Logic," *IBM J. Res. & Dev.* **18**, No. 5, 401–407 (September 1974); see *http://www.research.ibm.com/journal/rd/185/ibmrd1805D.pdf*.
69. J. R. Heath, P. J. Kuekes, G. S. Snider, and R. S. Williams, "A Defect-Tolerant Computer Architecture: Opportunities for Nanotechnology," *Science* **280**, 1716–1721 (June 1998).
70. H. B. Bakoglu and J. D. Meindl, "Optimal Interconnection Circuits for VLSI," *IEEE Trans. Electron Devices* **ED-32**, 903–909 (May 1985).
71. *Materials for High-Density Electronic Packaging and Interconnections*, National Materials Advisory Board, Commission on Engineering and Technical Systems, National Research Council, Washington, DC, 1990.
72. W. V. Vilkelis, "Lead Reduction Among Combinatorial Logic Circuits," *IBM J. Res. & Dev.* **26**, No. 3, 342–348 (May 1982); see *http://www.research.ibm.com/journal/rd/263/ibmrd2603I.pdf*.
73. D. P. Seraphim, "Chip-Module Package Interfaces," *IEEE Trans. Components, Hybrids, & Manuf. Technol.* **CHMT-1**, No. 3, 305–309 (September 1978).
74. A. Kumar and S. Tiwari, "Testing and Defect Tolerance: A Rent's Rule Based Analysis and Implications on Nanoelectronics," *Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, 2004, pp. 280–288.
75. C. A. Warwick and A. Ourmazd, "Trends and Limits in Monolithic Integration by Increasing the Die Area," *IEEE Trans. Semicond. Mfg.* **6**, No. 3, 284–289 (August 1993).
76. C. A. Warwick, R.-H. Yan, Y. O. Kim, and A. Ourmazd, "Toward Giga-Scale Silicon Integrated Circuits," *AT&T Tech. J.* **72**, No. 5, 50–59 (September/October 1993).
77. B. B. Mandelbrot, *Fractals: Form, Chance, and Dimension*, W. H. Freeman and Co., San Francisco, 1977, pp. 237–248.
78. H. M. Ozaktas, "Paradigms of Connectivity for Computer Circuits and Networks," *Opt. Eng.* **31**, No. 7, 1563–1567 (1992).
79. H. M. Ozaktas, "Information Flow and Interconnections in Computing: Extensions and Applications of Rent's Rule," *J. Parallel & Distr. Computing* **64**, 1360–1370 (2004).
80. J. C. Lyke, G. W. Donohoe, and S. P. Karna, "Cellular Automata Based Reconfigurable Systems as a Transitional Approach to Gigascale Electronic Architectures," *Proceedings of the 4th Military and Aerospace Applications of Programmable Devices and Technologies International Conference*, 2000.
81. H. M. Ozaktas, "Connectivity Models for Optoelectronic Computing Systems," *Proceedings of the 14th International Parallel and Distributed Processing Symposium, Workshop on Optics and Computer Science*, 2000, pp. 1072–1088.
82. A. Dickinson and M. E. Prise, "Free-Space Optical Interconnection Scheme," *Appl. Opt.* **29**, No. 14, 2001–2005 (May 1990).
83. Stanford University System Performance Simulator (SUSPENS); see *http://public.itrs.net/Files/2001ITRS/Links/design/GTX/PER_STUDY_DOCS/GTX_SUSPENS_doc.html*.
84. P. Raje, "A Framework for Insight into the Impact of Interconnect on 0.35-μm VLSI Performance," *Hewlett-Packard J. Online* **46**, No. 1 (February 1995); see *http://www.hpl.hp.com/hpjournal/95feb/feb95a15.htm*.
85. J. C. Eble, V. K. De, D. S. Wills, and J. D. Meindl, "A Generic System Simulator (GENESYS) for ASIC Technology and Architecture Beyond 2001," *Proceedings of the Ninth Annual IEEE International ASIC Conference*, Best Paper Award, 1996, pp. 193–196.
86. Rensselaer Interconnect Performance Estimator (RIPE); see *http://public.itrs.net/Files/2001ITRS/Links/design/GTX/RULES/ripe40-1.pdf*.
87. D. Sylvester and K. Keutzer, "System-Level Performance Modeling with BACPAC—Berkeley Advanced Chip Performance Calculator," *Proceedings of System-Level Interconnect Prediction (SLIP)*, 1999, pp. 109–114; see *http://www.eecs.umich.edu/~dennis/bacpac/*.

88. D. Sylvester and K. Keutzer, "Getting to the Bottom of Deep Submicron," *Proceedings of the International Conference on Computer Aided Design*, 1998, pp. 203–211.
89. The GTX Framework, "GSRC Technology Extrapolation (GTX)"; see *http://vlsicad.ucsd.edu/GSRC/GTX/*.
90. IBM Corporate Archives: 1401 Data Processing System; see *http://www-03.ibm.com/ibm/history/exhibits/mainframe/mainframe_PP1401.html*.
91. F. da Cruz, "The 1401"; see *http://www.columbia.edu/acis/history/1401.html*.
92. IBM Corporate Archives: 1410 Data Processing System; see *http://www-03.ibm.com/ibm/history/exhibits/mainframe/mainframe_PP1410.html*.
93. F. da Cruz, "The 1410"; see *http://www.columbia.edu/acis/history/1410.html*.
94. E. W. Pugh, *Building IBM: Shaping an Industry and Its Technology*, The MIT Press, Cambridge, MA, 1995, pp. 167–177, 234–236, 265–276, 285–288, and 301–305.
95. J. D. Warnock, J. M. Keaty, J. Petrovick, J. G. Clabes, C. J. Kircher, B. L. Krauter, P. J. Restle, B. A. Zoric, and C. J. Anderson, "The Circuit and Physical Design of the POWER4 Microprocessor," *IBM J. Res. & Dev.* **46**, No. 1, 27–51 (January 2002).
96. T. J. Slegel, E. Pfeffer, and J. A. Magee, "The IBM eServer z990 Microprocessor," *IBM J. Res. & Dev.* **48**, No. 3/4, 295–309 (May/July 2004).
97. P. N. Glaskowsky, "IBM Raises Curtain on POWER5," *Microproc. Rep.* **17**, Archive 10, 13–14 (October 2003).
98. J. Clabes, J. Friedrich, M. Sweet, J. DiLullo, S. Chu, D. Plass, J. Dawson, P. Muench, L. Powell, M. Floyd, B. Sinharoy, M. Lee, M. Goulet, J. Wagoner, N. Schwartz, S. Runyon, G. Gorman, P. Restle, R. Kalla, J. McGill, and S. Dodson, "Design and Implementation of the POWER5 Microprocessor," *Proceedings of the IEEE International Solid-State Circuits Conferemce (ISSCC)*, 2004, pp. 56–57.
99. M. Y. L. Wisniewski, E. Yashchin, R. L. Franch, D. P. Conrady, G. Fiorenza, and I. C. Noyan, "Estimating the Efficiency of Collaborative Problem-Solving, with Applications to Chip Design," *IBM J. Res. & Dev.* **47**, No. 1, 77–88 (January 2003); see *http://www.research.ibm.com/journal/rd/471/wisniewski.pdf*.
100. M. Y. L. Wisniewski, E. Yashchin, R. L. Franch, D. P. Conrady, D. N. Maynard, G. Fiorenza, and I. C. Noyan, "The Physical Design of On-Chip Interconnections," *IEEE Trans. Computer-Aided Design* **22**, No. 3, 254–276 (March 2003).
101. E. R. Kandel, J. Schwartz, and T. M. Jessell, *Principles of Neural Science*, Fourth Edition, McGraw-Hill Book Co., Inc., New York, 2000.
102. S. M. Breedlove and C. L. Jordan, "The Increasingly Plastic, Hormone-Responsive Adult Brain," *Proc. Natl. Acad. Sci.* **98**, No. 6, 2956–2957 (2001).
103. J. M. J. Murre and D. P. F. Sturdy, "The Connectivity of the Brain: Multi-Level Quantitative Analysis," *Biol. Cybern.* **73**, 529–545 (1995).
104. B. James, "The Basic Wiring Diagram of the Brain," *Kybernetes* **27**, No. 1, 88–89 (1998).

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