Transistorized Calculator

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The first fully operative transistorized calculator complete with automatic input and output is described. This compact "all-transistor" unit requires 95 per cent less power than a vacuum-tube unit of comparable capacity. Present operating experience indicates the important role which transistors will play in the computers of the future.

THIS TRANSISTORIZED CALCULATOR is the first completely transistorized calculator with automatic input-output. The experimental engineering model, shown in Fig. 1, contains over 2,100 transistors and is functionally identical to the International Business Machines Corporation (IBM) Type *604* electronic calculating punch, a vacuum tube machine of which over 2,000 are in use. The Type *604* serves as an excellent basis for comparing a complete machine system using tubes, to a functionally identical system using only transistors and other solid state devices. In the power supply and in all the switching circuits, each function of the model is performed without the use of any tubes.

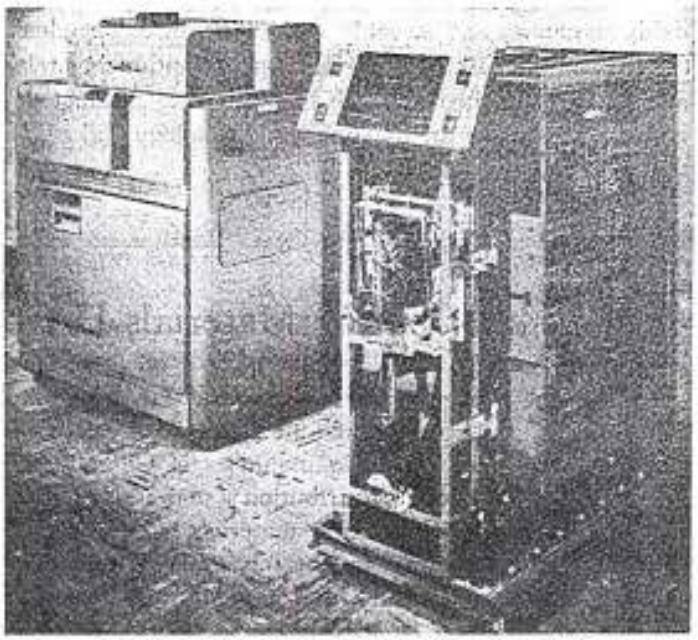

Fig. 1. The experimental transistorized computer is composed of a high-speed punching unit (left), and the transistorized calculating unit (right). The calculating unit is uncovered to show the bank of printed wiring panels on which the transistors are mounted

SYSTEM DESCRIPTION

THE CALCULATOR has a decimal arithmetic unit and decimal storage. It operates in the 1, 2, 4, 8 binary coded decimal system, with numbers transferred in parallel by decimal digit. The machine has a 13-digit decimal accumulator which is used to add and subtract. An 8-digit multiplicand can be multiplied by a 5-digit multiplier to develop a 13-digit product, and a 12-digit dividend can be divided by an 8-digit divisor to develop a 5-digit quotient. Provision is made for 32 digits of decimal storage. These are divided into 3-digit and 5-digit groups which may be combined by "assignment" into either 6- or 8-digit units. The transfer of information and the arithmetic operations are under the control of programing circuits.

The programing circuits provide an automatic sequence of 60 program steps to control the mode of operation. The machine is instructed to perform a desired computation by wiring a pluggable control panel. Sixty program step exit hubs control sequentially the execution of arithmetic and logical functions which have been wired on the control panel. These panels can be interchanged to alter the calculations. Another control panel is used to direct the operation of the input-output unit.

The input-output is by punched cards. A card punch is used for reading and punching at 100 cards per minute. Cards are fed first to a reading station, then to a punching station, and finally past a second reading station before being stacked. A total of 37 digits plus signs can be read into the calculator, and 29 digits plus signs can be punched out. Calculations are performed at a basic pulse repetition rate of 50 kc. The computer cycle occurs between the time a card is completely read at the first reading station and before it arrives at the punching station. Thus, the calculated result is being punched in one card while the next is being read. As a service check, the calculator should operate without failures at 70 kc.

TRANSISTOR CIRCUIT DESCRIPTION

THE GERMANIUM JUNCTION TRANSISTORS used in this experimental machine are fairly low frequency response units. Some of the first transistors used had a 700-kc minimum alpha cutoff frequency, but later transistors were specified for a 1-mc alpha cutoff frequency. The grounded emitter current gain of the junction transistors was specified as 40 minimum and 90 maximum, although some of the transistors used had grounded emitter current gains as

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Junction transistors have characteristics that make them very satisfactory for use in switching circuits. One desirable characteristic is that they approach an ideal switch. While they are more temperature sensitive than point-contact transistors, their cutoff collector current is two or three orders of magnitude smaller than that which point-contact transistors exhibit. This feature, plus their high current gain in the grounded-emitter configuration, makes them applicable to this type of machine, which uses an essentially d-c type of logic with a signal range of 5 volts. The decision to use a signal with a 5-volt excursion, from −5 volts to ground, was made for several reasons. First and most important of these was the necessity for reliability. Early experience indicated that the cutoff current of a transistor had a higher rate of increase with time at the higher collector voltages than it did at the lower collector voltages. This indicated that a low collector voltage, and hence a low signal swing should be maintained.

The use of low signal levels introduces several problems, one of these being in respect to the use of visual indicators. The *NE2* neon indicator is a rather efficient light producer but requires a voltage change of at least 20 volts for operation. This voltage is obtained with separate voltage amplifiers, hence lower signals can be used for the switching circuits. Another problem is that the signal level also influences the speed of operation and energy required in a transistor switching circuit. The alpha cutoff frequency of a transistor is directly related to the collector voltage, and the collector capacitance is inversely related to the collector voltage. Both of these factors indicate that a high signal level is best for high-speed operation. However, the larger the signal excursion, the larger is the energy stored on stray capacitance. A system with 20-volt signals has 16 times as much energy stored on the stray capacitance as is stored on the stray capacitance of a 5-volt system. In addition, the "punch-through" voltage which can limit the peak inverse voltage rating of a transistor, bears an inverse relationship to the alpha cutoff frequency. These factors indicated that future high-speed machines would of necessity operate with low signal swings. In addition, a collector supply voltage could be used which is three times the collector clamp voltage. This would achieve reasonably short recovery times without the use of excessively large supply voltages. Another benefit derived from the use of low voltages is that the power supply voltages can be applied or removed in a random sequence, and that cards can be removed without the necessity of removing power. As a result of all these considerations, it was felt that a 5-volt signal swing should be reasonably close to optimum.

Various types of basic circuits are employed to accomplish the necessary switching and control functions. Included among these circuits are inverters, emitter followers, triggers, logical circuits, and output drivers.

Inverter. The inverter is shown in Figs. 2*A* and 2*B*, using both *PNP* and *NPN* types of junction transistors. This gives the system designer an advantage not realized with

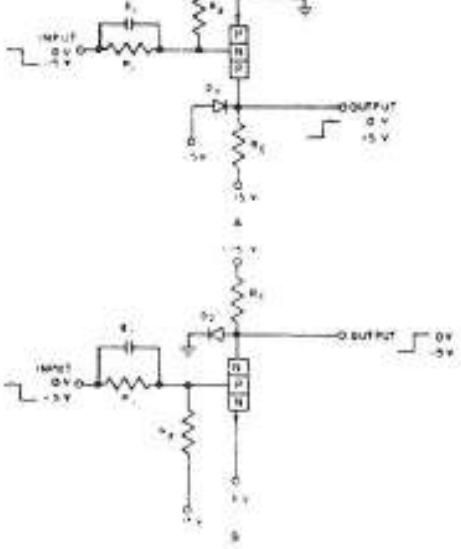


Fig. 2. Inverter

vacuum tubes. The *PNP* inverter is capable of charging a capacitive load rapidly when a positive output is required. Conversely, the *NPN* inverter can be used when a capacitive load must be driven rapidly in a negative direction.

The diode clamps, D_1 and D_2, are used for two reasons. They reduce by a factor of two the turn-off time of the output signal when the inverter is driving a capacitive load. Also, the clamps firmly establish the OFF level, and make this level less dependent on the type of load being driven. Inverter circuits are particularly susceptible to minority carrier storage effects, which can cause an excessive turn-off delay. These effects can be controlled by means of resistor R_1 and capacitor C_1. Resistor R_1 is chosen so that a transistor with a minimum acceptable grounded-emitter current gain will be just held in saturation, when the input is at −4 volts for a *PNP* transistor. This means that for the same conditions, a transistor with a high grounded-emitter current gain will be driven further into saturation. The minority carrier storage delay time will be abnormally long if a large transient current is not caused to flow into the base terminal when the transistor is turned off. The capacitor C_1 causes this transient current to flow into the base when the input is returned to ground, thus supplying an adequate charge with which to turn off the transistor. It was found that a 2.5 to 1 spread in grounded-emitter current gain gave a reasonable turn-off time with a moderate

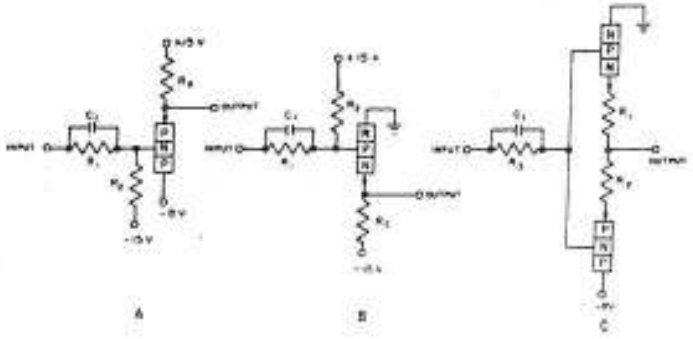


Fig. 3. Emitter follower

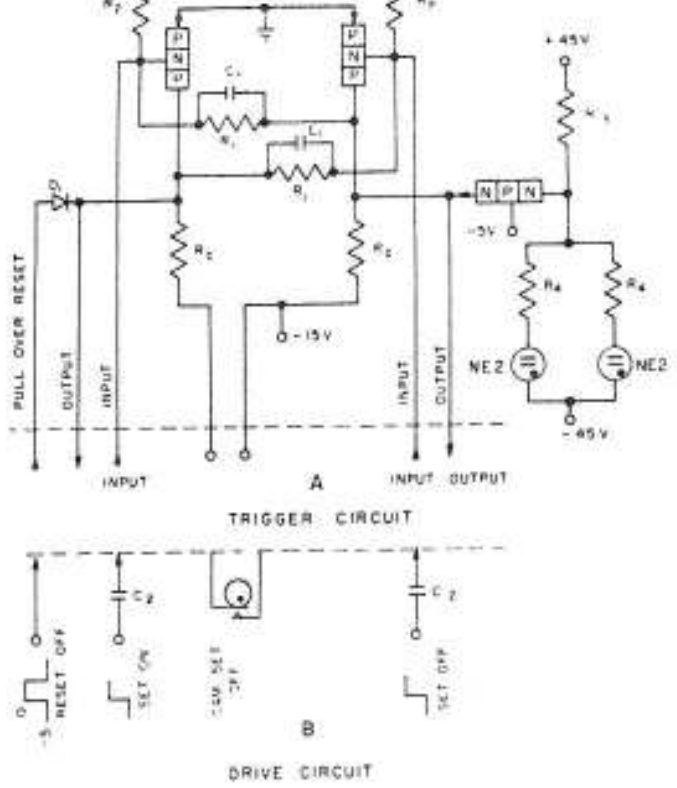


Fig. 4. Ring counter

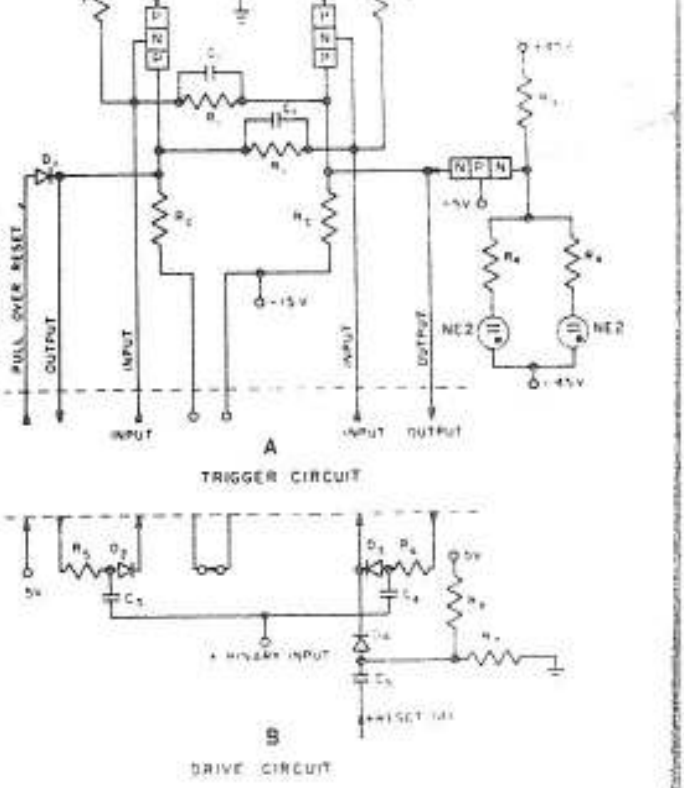


Fig. 5. Counter trigger

value of capacitance for capacitor C_1. The value of the load resistor R_e is chosen so as to limit the maximum collector current to 5 milliamperes.

Emitter Follower. The circuit for the emitter follower is shown in Figs. 3*A* and 3*B*. It is desirable, as in the case of the inverter, to use both a *PNP* and an *NPN* type of emitter follower. The characteristics of the emitter follower cause the signal to suffer a loss in amplitude and a shift in level. After the signal is lowered by several stages of emitter followers or diode logic, the loss in amplitude is corrected by passing the signal through an inverter or level resetter. The shift in level, on the other hand, is compensated for at each emitter follower. This is achieved by means of resistors R_1 and R_2, and the voltage to which R_2 is returned. One serious difficulty encountered with an emitter follower when driving a capacitive load is an overshoot in the output waveform. If the resistor R_1 is not by-passed, this overshoot can be quite objectionable, but by shunting R_1 with capacitor C_1 the overshoot can be minimized.

The collector of the *PNP* emitter follower is returned to a potential of -8 volts rather than -5 volts. This is done to prevent minority carriers from being injected into the base region from the collector, when the input to the emitter follower is at -6 volts. This reduces the loading that the emitter follower presents to its driving stage, and reduces the rise time of the output. Because the *NPN* emitter followers in this calculator are used to drive loads with long time constants, the minority carrier effects are not appreciable.

When fast rise and fall times are required with capacitive loads, a complemented emitter follower (Fig. 3*C*) is used. Positive-going input waveforms cause the *PNP* transistor to cut off and the *NPN* transistor to supply the load current. If the input waveforms are negative-going, the *NPN* transistor cuts off and the *PNP* transistor discharges the capacitive load. This circuit can drive 12 triggers in parallel at a pulse repetition of 50 kc.

Trigger. The basic (Eccles-Jordan) trigger is shown in Figs. 4*A* and 5*A*. The collectors are clamped at -5 volts by means of diode D_1 on the left side, and the emitter to base junction of the *NPN* indicator transistor on the right side. As was mentioned previously, the signal swing is too low to ignite a neon indicator and, therefore, a larger signal is developed by means of the *NPN* neon indicator transistor. The collector of this transistor can achieve a voltage excursion of 40 volts for operating the neons.

A total of five different types of triggers are used in the machine, differing only in how they are driven. Some are reset ON, while others are reset OFF. The basic drive circuits are shown in Figs. 4*B* and 5*B*. Fig. 4*B* is the type of input used when a trigger is operated in a ring circuit. The trigger can be reset by means of a cam-driven contact which opens the collector supply on one side of the trigger. It can also be reset by means of diode D_2 when the input is driven positive by a *PNP* inverter which is normally off. This input is at -5 volts until the inverter conducts and resets the trigger off. Positive-going waveforms on the SET ON or SET OFF inputs set the trigger in the ON (right transistor conducting) or OFF (left transistor conducting) state, respectively.

volts and no cam reset is required. The purpose of R_5, D_2, C_2 and R_6, D_3, and C_4 is to act as gates or "steering" circuits. Capacitor C_3 and diode D_4 provide a reset off input. These binary triggers are cascaded, with blocking feedback from the fourth stage to the second stage, to form a binary-coded decimal counter.

Decimal Counter. The decimal counter is used for the 13-digit accumulator, a 5-digit MQ, and the 32 digits of storage, for a total of 50 decimal counter positions in the machine. The timing conditions in this counter are aggravated by the low frequency response of the early junction transistors that were used. One frequency limitation that became apparent is the delay accumulated in the "carry" from a 4-stage decimal counter. This delay was avoided by using a circuit (Fig. 6) that detects if a 9 is contained in the 1-2-4-8 counter. The tenth input pulse is gated directly through the counter to produce a "carry" with no delay due to the transition time of the triggers. This "fast carry" is accomplished by a three-way OR circuit. The inputs to the OR circuit are from the counter input and from the first (1 *TR*) and fourth (8 *TR*) stages of the counter. The output of the OR circuit can swing negatively only if the counter contains a 9 and the input is negative. When the tenth input pulse goes positive, an immediate output occurs from the OR circuit to indicate the presence of a carry.

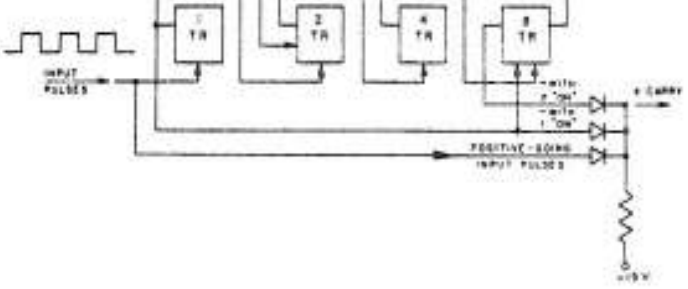


Fig. 6. Coded decimal counter

Timing Ring. An application of the ring trigger circuit discussed previously is in a timing ring shown in Fig. 7. This ring has its alternate stages driven by two separate "advance" lines. The ring is arranged so that the "odd" stages are driven OFF on one "advance" signal and the "even" stages are driven OFF on the next successive signal. Any stage that is being driven OFF can be coupled to the next stage to turn it ON. The two advance lines are each coupled to alternate triggers by a common line driven by an inverter; these lines clamp every other stage of the ring in the OFF state. The outputs of each trigger are capacitively coupled to the corresponding bases of the transistors in the next stage. Therefore, any trigger in the ring that is pulled OFF will drive the next successive trigger ON with a fast regenerative action.

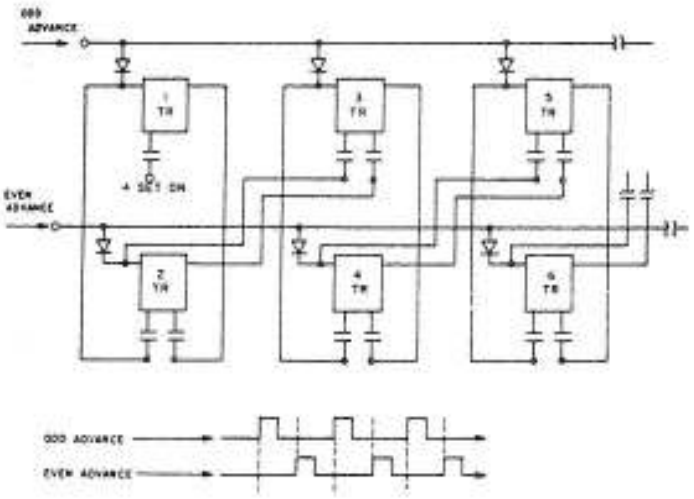


Fig. 7. Timing ring

Logical Circuits. Logic is performed both with diodes and with transistors. Transistor logic is used wherever the requirements of speed dictate. The AND operation is performed by means of *PNP* emitter followers paralleled with a common load resistor as shown in Fig. 8*A*. The output is at ground if X and Y and Z are each at ground level. The OR operation is performed by the circuit shown in Fig. 8*B*, with the output at ground level if either X or Y or Z is at ground.

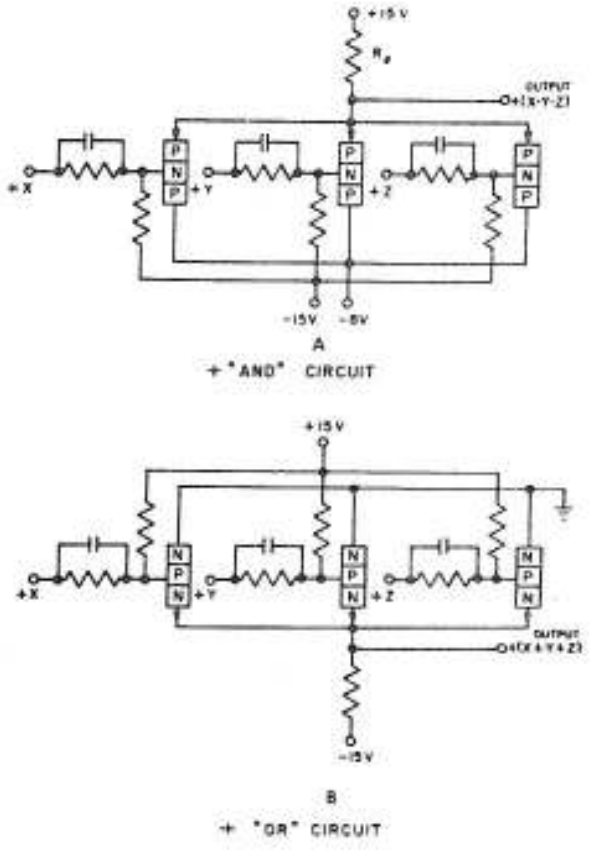


Fig. 8. Transistor logic

Output Driver. The relays and other electromagnetic devices in the calculator are driven by a power transistor developed and fabricated by IBM.[1] This transistor exhibits a negative resistance characteristic and is used in a manner very similar to the use of a thyratron tube. The relay driver circuit is shown in Fig. 9. The thyratron-like transistor will "latch on" with a short duration input pulse and the collector circuit is opened mechanically in order to return

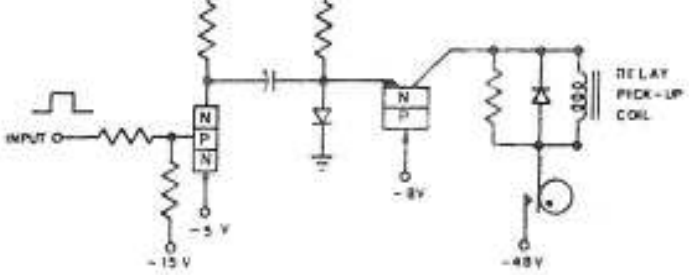


Fig. 9. Relay driver

the transistor to its state of low conduction. The average emitter-to-collector current gain of the power transistor is four and indicates the current multiplying property of the device. The average collector voltage drop at 100 milliamperes is 2 volts, and the transistor can be triggered ON with a pulse duration of about 1 microsecond. This device is used for all the output circuitry to the card punch.

Packaging. The transistorized model occupies less than one half the volume of the vacuum tube *604*, although the packaging was not directed toward extreme miniaturization. Printed wiring techniques are used for assembly of the transistor circuitry. A pluggable unit arrangement is used to facilitate assembly and servicing of the machine. The basic circuit package consists of circuit components soldered on a printed wiring card, 3 by $5^1/_2$ inches, with 18 terminals. The 595 cards in the calculator are composed of a total of 40 different types.

The supply voltages used are 15, −5, −8, and −15 volts for the transistor circuits. In addition, 45 and −45 volts are supplied for the neon indicators. The power supply has a tuned transformer input which enables the circuits to operate satisfactorily with a line voltage variation of from 90 to 125 volts at 60 cycles per second.

The total power consumption of the transistorized calculator is only 310 watts. This is a power reduction of 95 per cent from the vacuum-tube machine.

Operating Experience. The transistorized calculator has undergone tests to study machine operation at elevated temperatures and it has been displayed and operated under adverse conditions in several different cities. A total of 5 per cent of the transistors have been replaced. Four per cent were caused by: (1) initial wiring errors; (2) accidental short circuits when servicing; (3) improper insertion of cards; (4) card at wrong location; or (5) errors on the cards, such as incorrect resistor values. Of the additional 1 per cent, half of these failures were due to either increased reverse current or current gain out of specifications. The others were due to miscellaneous troubles, such as a high noise figure or instability. Probably most of these were damaged during testing periods, but were not detected immediately.

Although quite low signal levels are used, no difficulty is experienced with "pickup" and related troubles, even with 40-volt relay circuitry physically located near some of the electronic circuits. Since careful consideration was given to relay and electronic ground return isolation, no out flor from other transient voltages.

Special precautions are not taken when transistors or printed wiring cards are removed or inserted with all voltages on the machine. Also, any voltage can be removed from the electronic circuits without damaging transistors, and the voltages can be removed or applied in any sequence.

The transistor machine can be readily serviced, and the circuitry is easily understood by engineers familiar with vacuum tube machines. It even offers a few additional servicing advantages because the lower voltages are somewhat safer and no filament warm-up time is required.

CONCLUSION

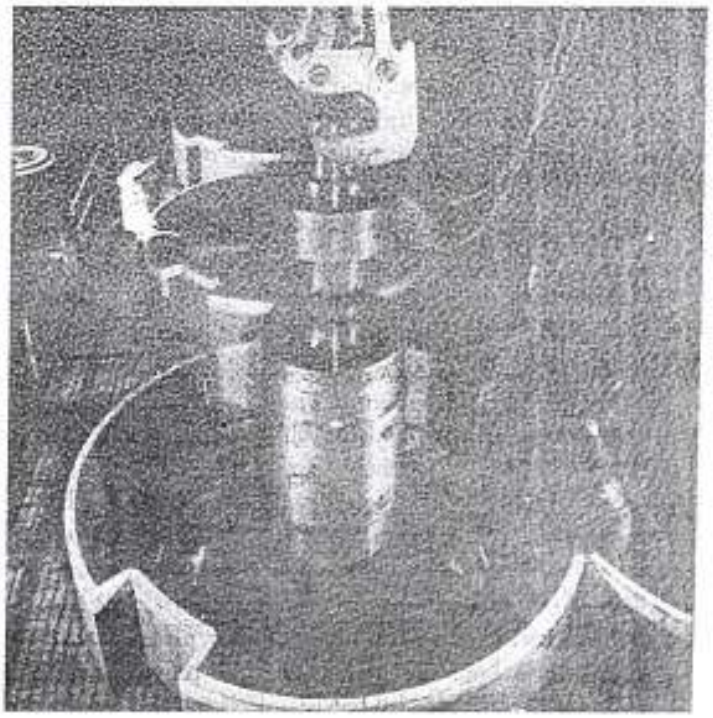
THE EXPERIMENTAL transistorized calculator contains 2,165 transistors and 3,600 germanium diodes, with no vacuum tubes. Operating experience has proved very satisfactory and indicates that the transistor will play an important part in the computers of tomorrow.

The use of transistors in future computers promises many advantages. In addition to the obvious advantages of transistors in providing size and power reduction, the most important factor is the expected long life of transistors, which should provide a much higher degree of system reliability.

REFERENCE

1. A New Transistor with Thyratron-Like Characteristics, R. F. Rutz, A. W. Berger, *Proceedings*, 1955 IRE-AIEE Electronic Components Conference, May 26-27, 1955.

Production Flexibility Attained



A 90-ton generator rotor descends into one of three new heat treating furnaces installed at U. S. Steel's Homestead District Works, Pittsburgh, Pa., forging facilities recently expanded. A quenching tower adjacent to furnaces prevents excessive cooling of forgings in transfer.