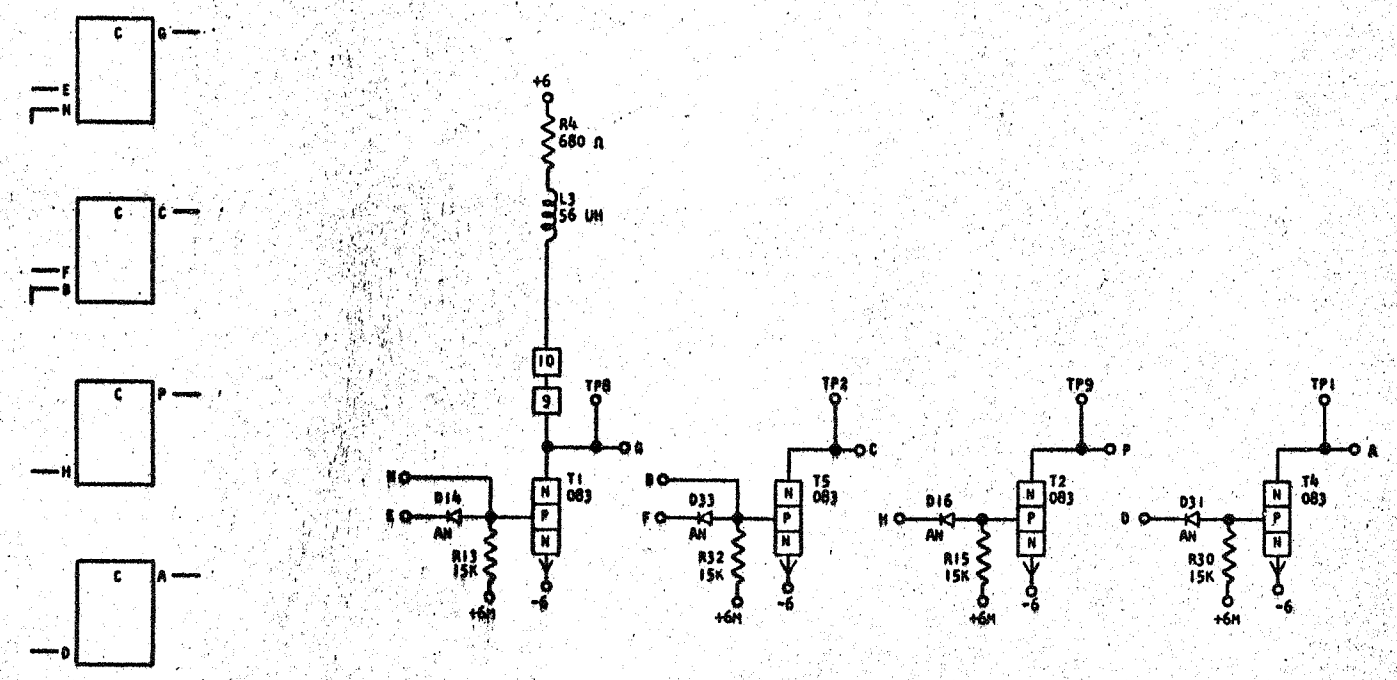
729850 STANDARDS CODE

CARD CODE 729850
CR YG

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371277

CTDL - ONE WAY NPN I LOAD - FOUR ON CARD



SEQUENCE OF OPERATION

1. UP INPUT TRANSISTOR ON OUTPUT DOWN
2. DOWN INPUT TRANSISTOR OFF OUTPUT UP
3. INPUTS ON EXTENDER CARD UP IN COINCIDENCE WITH UP INPUT ON CARD FOR DOWN OUTPUT
4. T2, T4, T5 COLLECTORS MUST BE LOADED
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

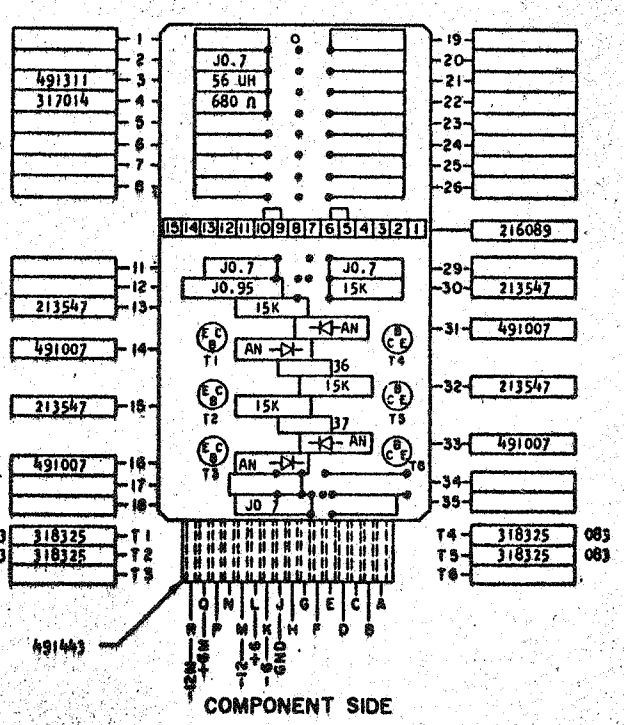
PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, H,D	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
H,B		EXTENDER INPUT		UP	-6.	
				DOWN	-12	
G,C, P,A	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE, SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF 'OR'.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL - ONE WAY NPN L LD.-FOUR ON CARD					6-29-62	9C115599					
						30-4-63	TT83687					
DESIGN				MODEL	SMS							
DETAIL	RO	3-1-62		SCALE	NONE							
CHECK	WH	3-1-62		DRAW	LIS	3-17-62						
APPRO				CHECK								

729850

C

STANDARDS CODE 729851

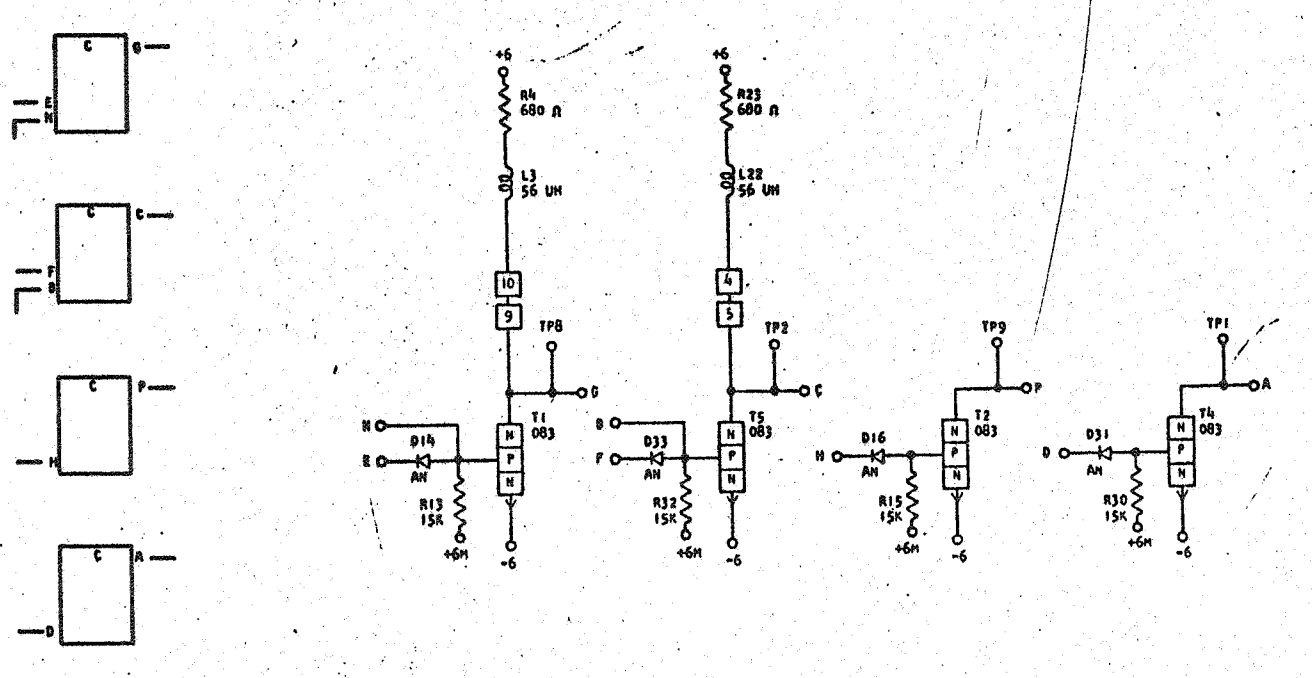
CARD CODE 729851

CR ZT

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371275

CTDL - ONE WAY NPN



SEQUENCE OF OPERATION

1. UP INPUT TRANSISTOR ON OUTPUT DOWN
2. DOWN INPUT TRANSISTOR OFF OUTPUT UP
3. INPUTS ON EXTENDER CARD UP IN COINCIDENCE WITH UP
4. T2, T4 COLLECTORS MUST BE LOADED
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

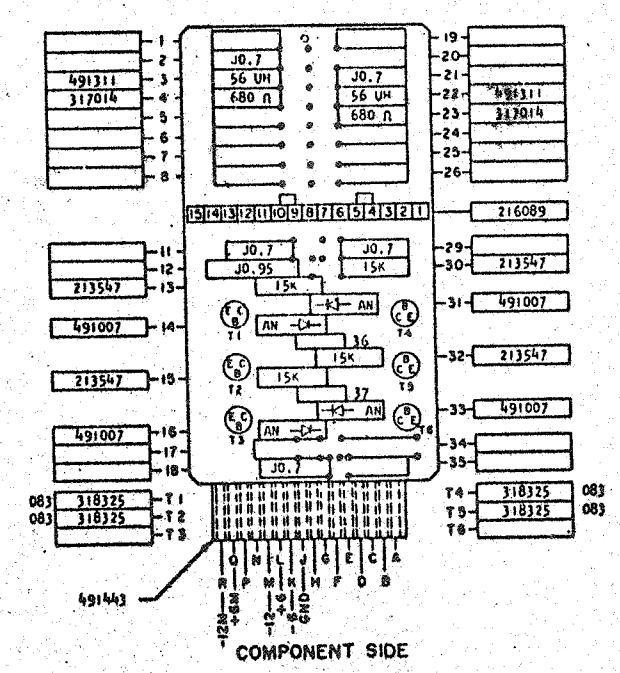
PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, H,D	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
A,B		EXTENDER INPUT		UP		-6.0
				DOWN		-12.5
G,C, P,A	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING BF 'OR'.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL-ONE WAY NPN		MODEL	SMS	2-*-62	EC115599					729851
DESIGN					30-4-63	JT83687					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WM	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

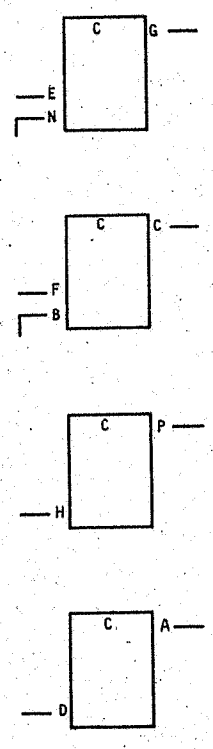
729851

STANDARDS CODE	729852

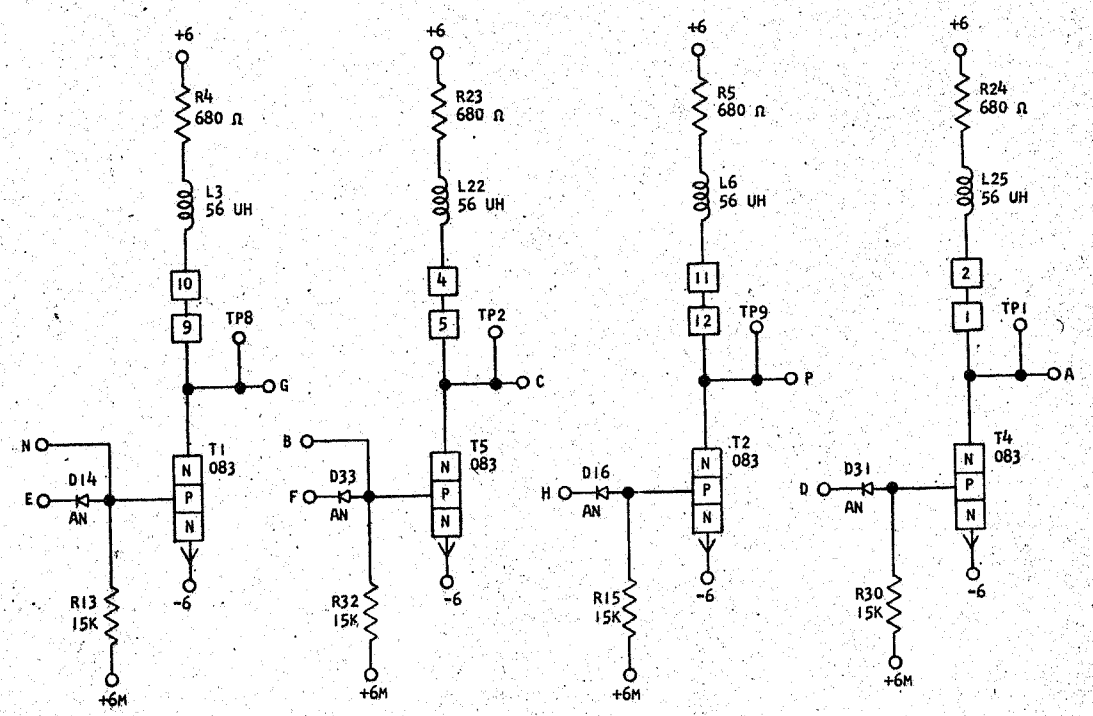
CARD CODE	729852
CR ZV	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371274



CTDL-ONE WAY NPN FOUR LOADS



SEQUENCE OF OPERATION

1. UP INPUT TRANSISTOR ON OUTPUT DOWN
2. DOWN INPUT TRANSISTOR OFF OUTPUT UP
3. INPUTS ON EXTENDER CARD UP IN COINCIDENCE WITH UP INPUT ON CARD FOR DOWN OUTPUT
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

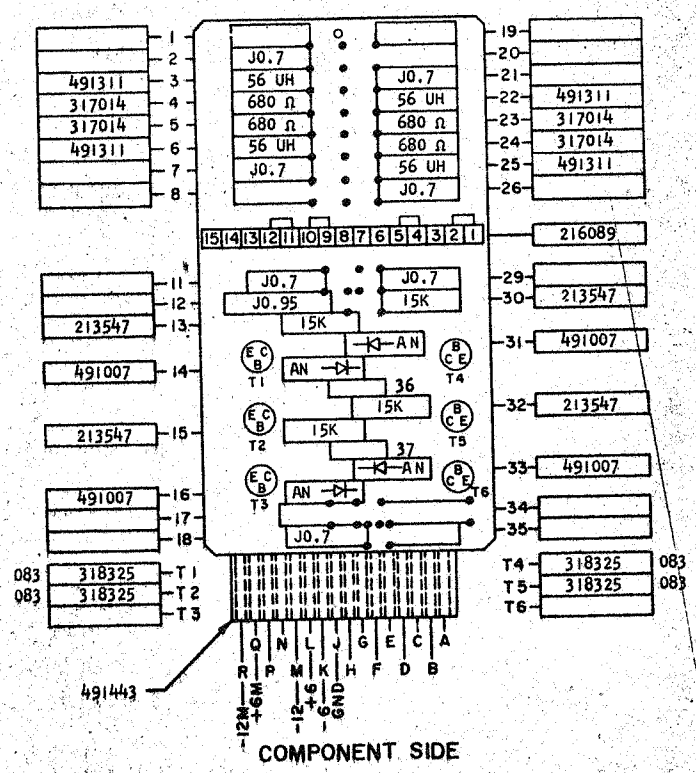
PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E, F, H, D	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
N,B		EXTENDER INPUT		UP		-6.0
				DOWN		-12.5
G,C, P,A	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS.
EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR -CTDL- ONE WAY NPN FOUR LOADS				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6 ''-62	115599					

729852

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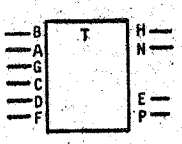
729852

STANDARDS CODE 729853

CARD CODE 729853
CW --

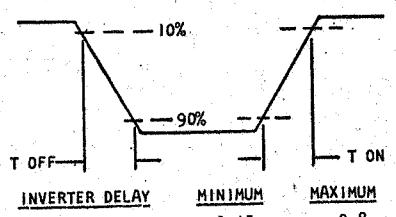
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371534



DELAY - USEC

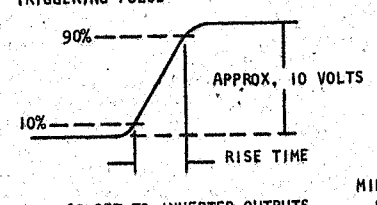
TYPICAL INVERTER AND EF OUTPUT WAVEFORM



INVERTER DELAY	MINIMUM	MAXIMUM
T OFF	0.15	0.8
T ON	0.10	0.3
EF DELAY	**MINIMUM**	**MAXIMUM**
T OFF	0.05	0.1
T ON	0.10	0.4

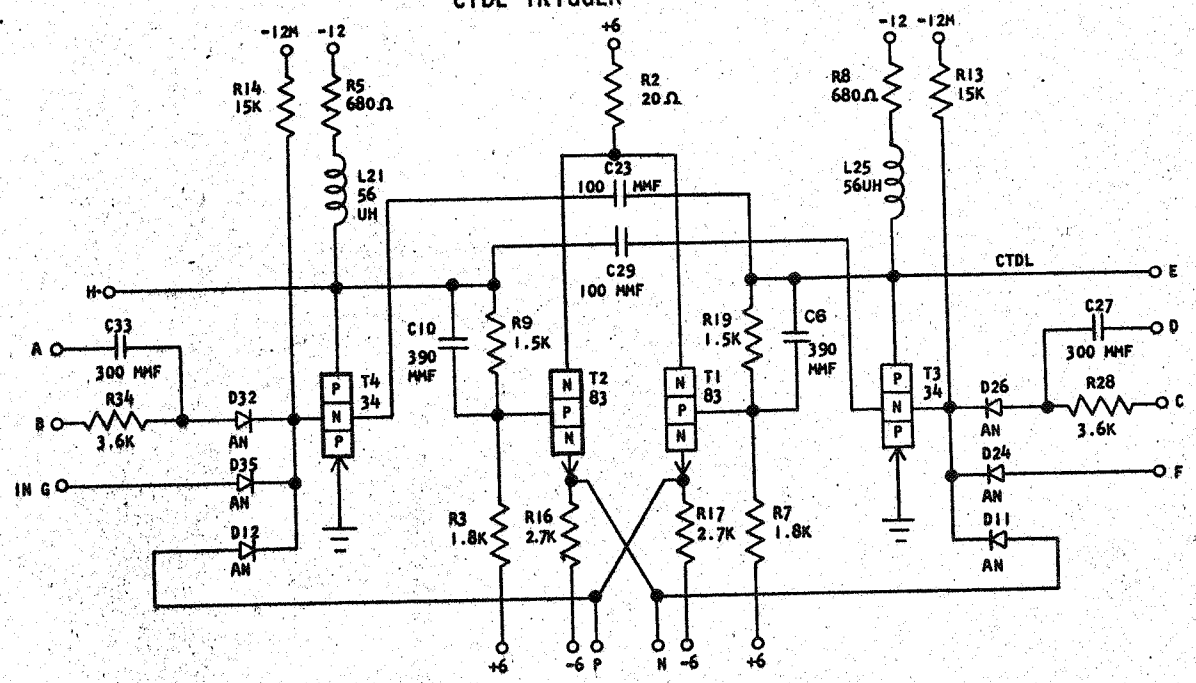
THE FOLLOWING DELAY INFORMATION APPLIES WHEN THE AC TRIGGERING INPUT PULSE HAS A RISE TIME OF 0.45 USEC. (SEE FOLLOWING FIGURE)

TRIGGERING PULSE



	MINIMUM	MAXIMUM
FROM AC SET TO INVERTER OUTPUTS	0.10	0.40
FROM AC SET TO EF OUTPUTS	0.10	0.30

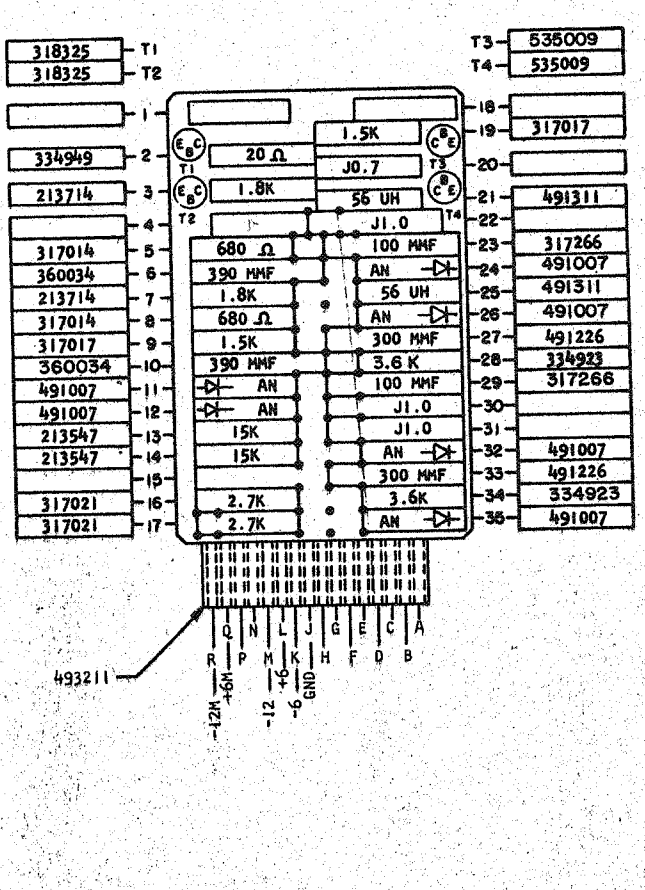
CTDL TRIGGER



SEQUENCE OF OPERATION

1. T4, T2 ON, T3, T1 OFF
2. GATE UP TO PIN B, AC SET TO PIN A T3, T1 ON T4, T2 OFF
3. GATE UP TO PIN C, AC SET TO PIN D T3, T1 OFF T4, T2 ON
4. GATE MUST BE UP 3.75 U SEC BEFORE AC SET
5. DC SET PIN G, T3, T1 ON T4, T2 OFF
6. COLLECTIVE PULLOVER MAY BE USED TO TURN T3 OR T4 ON
7. DC SET ON PIN F UP WHEN T1, T3 ARE ON WILL RESET TO CONDITION 1
8. DC SET OR RESET PULSE WIDTH: 0,5 USEC MINIMUM.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
B	U	GATE		UP	-0.54	0.24
				DOWN	-7.44	-12.4
A,D	U	AC SET		UP	-0.54	0.24
				DOWN	-7.44	-12.4
G	T	DC SET		UP	1.44	6.24
				DOWN	-0.74	-6.24
E	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
N	T	OUTPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C	U	GATE		UP	-0.54	0.24
				DOWN	-7.44	-12.4
F	T	DC SET		UP	1.44	6.24
				DOWN	-0.74	-6.24
P	T	OUTPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
H	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL TRIGGER					6 62	115599					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729853

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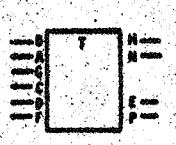
CW --

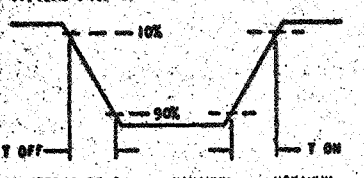
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371534



DELAY = USEC

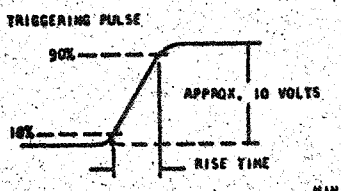
TYPICAL INVERTER AND EF OUTPUT WAVEFORM



INVERTER DELAY	MINIMUM	MAXIMUM
T OFF	0.15	0.8
T ON	0.10	0.3
EF DELAY	**MINIMUM**	**MAXIMUM**
T OFF	0.05	0.1
T ON	0.10	0.4

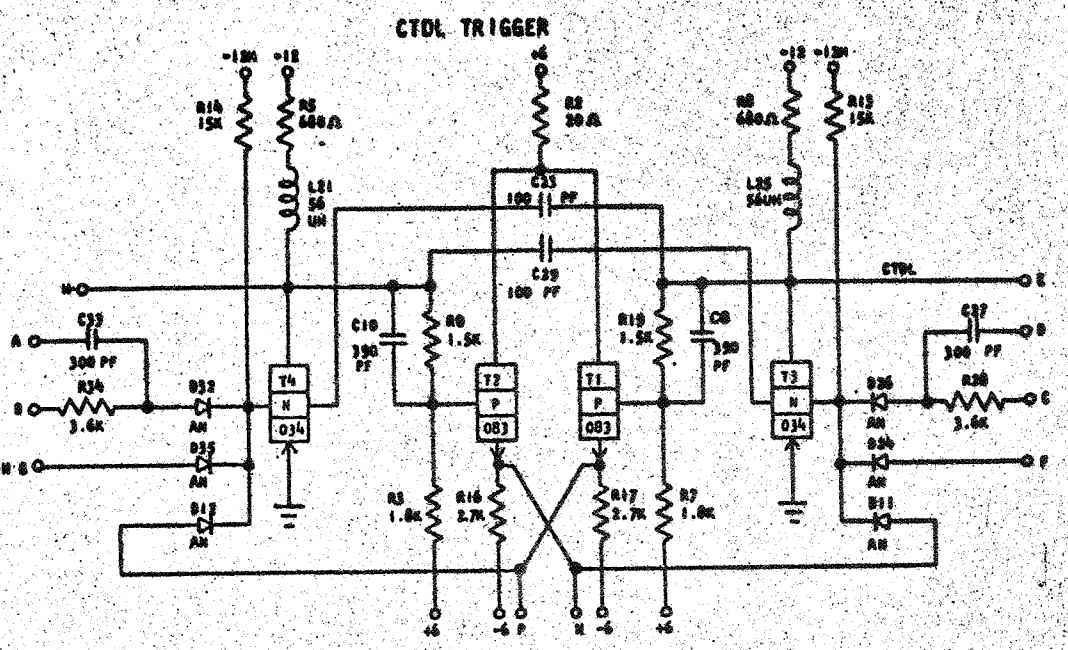
THE FOLLOWING DELAY INFORMATION APPLIES WHEN THE AC TRIGGERING INPUT PULSE HAS A RISE TIME OF 0.45 USEC. (SEE FOLLOWING FIGURE)

TRIGGERING PULSE



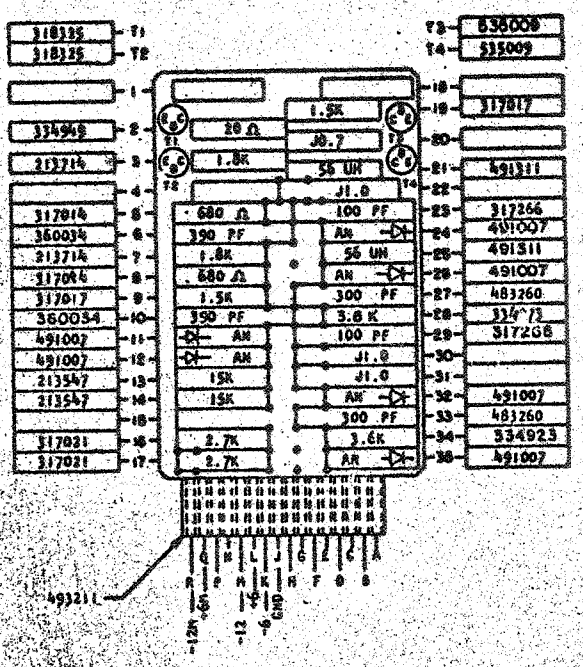
	MINIMUM	MAXIMUM
FROM AC SET TO INVERTER OUTPUTS	0.10	0.40
FROM AC SET TO EF OUTPUTS	0.10	0.30

CTDL TRIGGER



SEQUENCE OF OPERATION

1. T4, T2 ON, T3, T1 OFF
2. GATE UP TO PIN B, AC SET TO PIN A T3, T1 ON T4, T2 OFF
3. GATE UP TO PIN C, AC SET TO PIN B T3, T1 OFF T4, T2 ON
4. GATE MUST BE UP 3.75 U SEC BEFORE AC SET
5. DC SET PIN G, T3, T1 ON T4, T2 OFF
6. COLLECTIVE PULLOVER MAY BE USED TO TURN T3 OR T4 ON
7. DC SET ON PIN F UP WHEN T1, T3 ARE ON WILL RESET TO CONDITION 1
8. DC SET OR RESET PULSE WIDTH: 0.5 USEC MINIMUM.



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B	U	GATE		UP	-0.54	0.24
				DOWN	-7.44	-12.4
A,B	U	AC SET		UP	-0.54	0.24
				DOWN	-7.44	-12.4
G	T	DC SET		UP	1.44	6.24
				DOWN	-0.74	-6.24
E	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
N	T	OUTPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C	U	GATE		UP	-0.54	0.24
				DOWN	-7.44	-12.4
F	T	DC SET		UP	1.44	6.24
				DOWN	-0.74	-6.24
P	T	OUTPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
N	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.													
NAME CARD ASM EXTR-CTDL TRIGGER													
DESIGN			MODEL	SMS									
DETAIL	RG	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	ETC	3-17-62								
APPRD			CHECK										

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4-19-62	E15899					
1-4-63	EC11605					
10-6-63	TT 8868T					

729853

C

STANDARDS CODE 729854

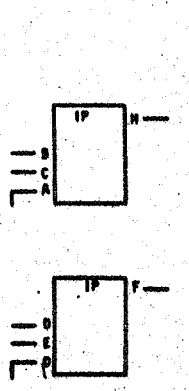
CARD CODE 729854

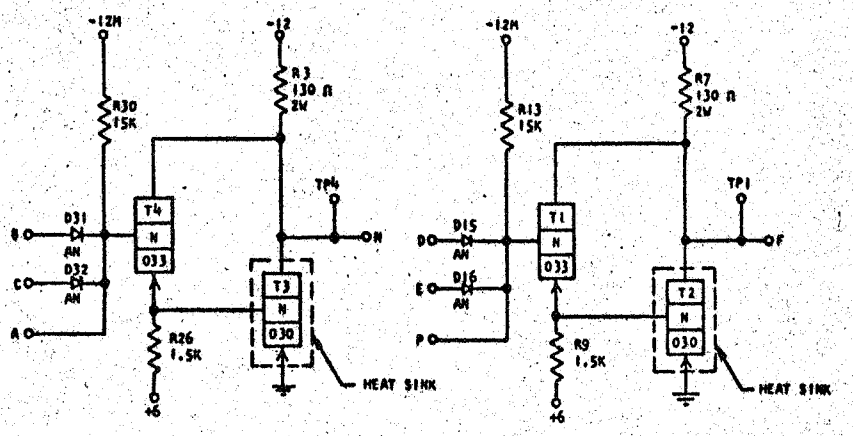
CY --

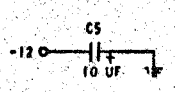
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371542

CTDL POWER INVERTER







SEQUENCE OF OPERATION

1. ALL INPUTS DOWN T4, T1 ON; T3, T2 OFF OUTPUT UP
2. ANY INPUTS UP T4, T1, OFF; T3, T2 ON OUTPUT DOWN
3. DOWN INPUT OF AT LEAST 1 U SEC REQUIRED TO TURN T4 OR T1 ON
4. EXTENDER INPUTS MUST BE DOWN IN COINCIDENCE WITH INPUTS ON CARD FOR UP OUTPUT

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
B,D	T	INPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
C,E	T	INPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
A,P		EXTENDER INPUT		UP	-6	
				DOWN	-12	
N,F	U	OUTPUT		UP	-5.2	0.8
				DOWN	-7.4	-9.2

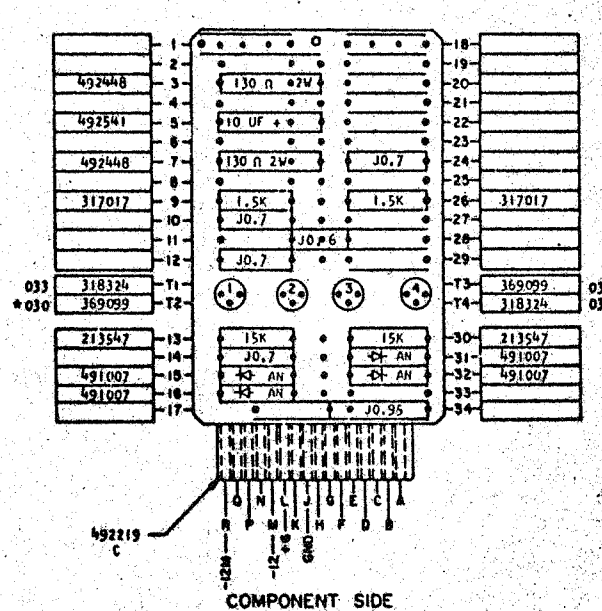
DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.20	0.60*
TURN OFF	0.25	0.40**

*THIS DELAY CAN INCREASE TO 0.75 USEC FOR CAPACITIVE LOAD.

**THIS DELAY CAN INCREASE TO 0.55 USEC FOR CAPACITIVE LOAD.

NOTE: LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL POWER INVERTER				6-19-62	EC 115599					
DESIGN			MODEL	SMS	30.4.63	TT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	L16 3-17-62							
APPRD			CHECK								

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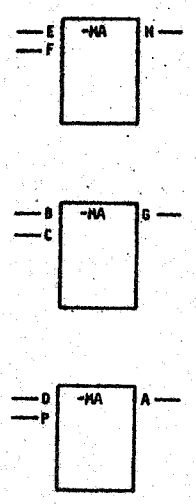
729855 STANDARDS CODE

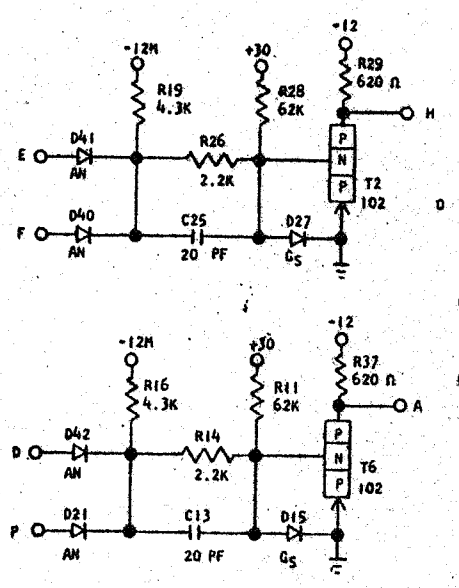
CARD CODE D A B - 729855

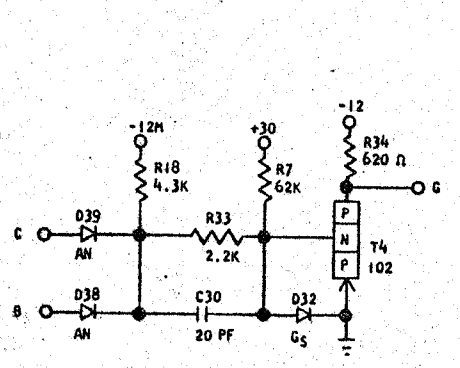
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371924

DTDL - AND GATE





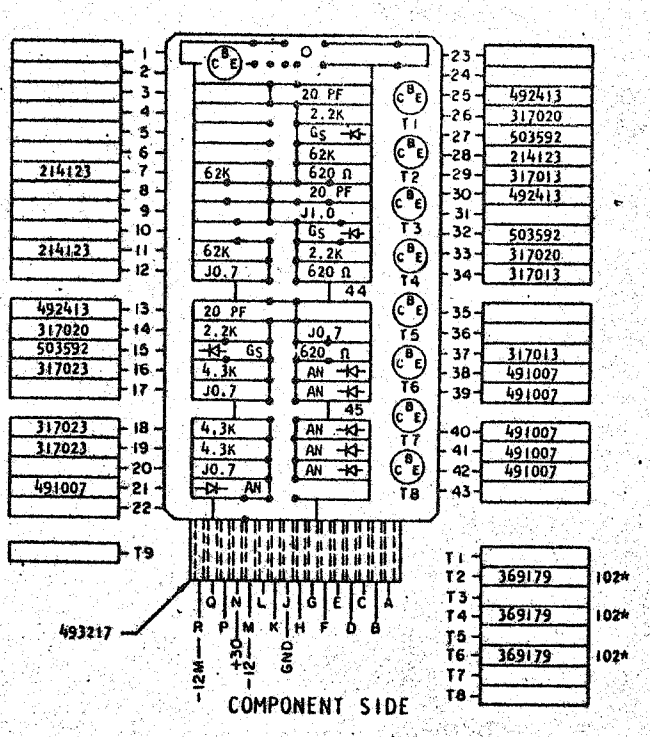


SEQUENCE OF OPERATION

1. INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. EITHER OR BOTH INPUTS UP TRANSISTOR OFF AND OUTPUT IS DOWN
3. DRIVING CTOL LOADS:
   MAXIMUM TURN ON DELAY - .28 USEC
   MAXIMUM TURN OFF DELAY - .09 USEC

   DRIVING WORST CASE CLOCK LOAD
   MAXIMUM TURN ON DELAY - .15 USEC
   MAXIMUM TURN OFF DELAY - .144 USEC

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, D,P, C,B	T	INPUTS		UP	+1.44	+6.24
				DOWN	-4.46	-6.24
H A G	U	OUTPUTS		UP	-.89	+.24
				DOWN	-7.44	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729855
NAME	CARD ASM TSTR - DTDL- AND GATE					4-2-62	115599						
DESIGN			MODEL	SMS									
DETAIL	RO	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRD			CHECK										

C

729855

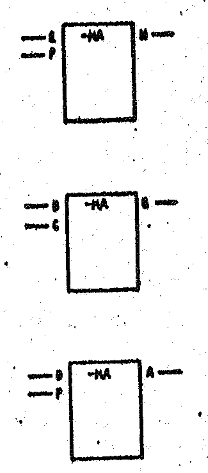
STANDARDS CODE

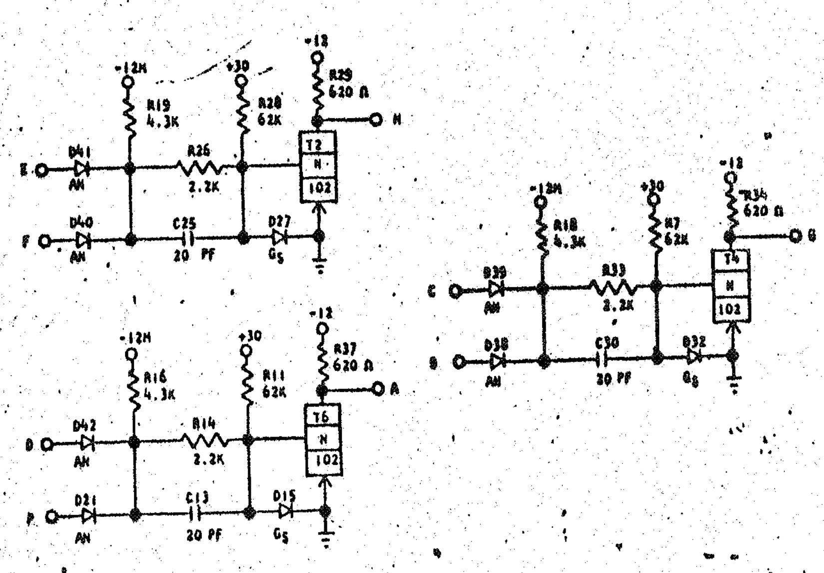
CARD CODE	729855
D A B -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371924

DTDL - AND GATE



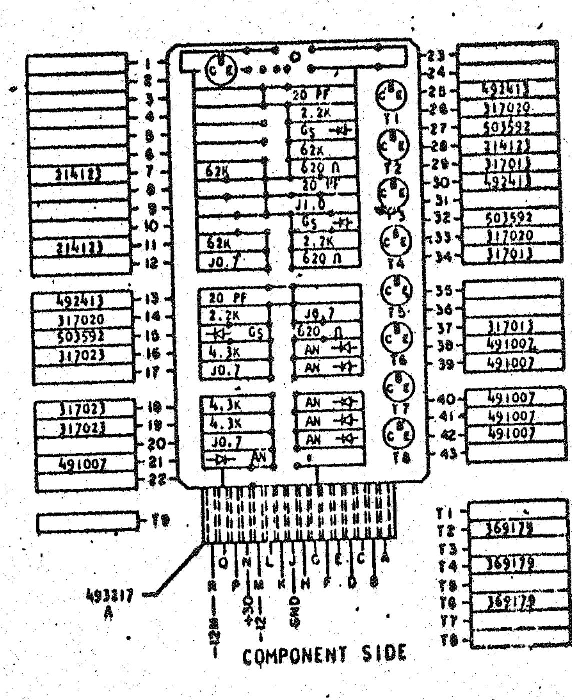


SEQUENCE OF OPERATION

1. INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. EITHER OR BOTH INPUTS UP TRANSISTOR OFF AND OUTPUT IS DOWN
3. DRIVING CTDL LOADS:
   MAXIMUM TURN ON DELAY = .28 USEC
   MAXIMUM TURN OFF DELAY = .09 USEC

   DRIVING WORST CASE CLOCK LOAD
   MAXIMUM TURN ON DELAY = .15 USEC
   MAXIMUM TURN OFF DELAY = .144 USEC

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E,F,D,P,C,B	T	INPUTS		UP	+1.44	+6.34
				DOWN	-4.46	-6.24
N,A,G	U	OUTPUTS		UP	-.89	+.24
				DOWN	-7.44	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - DTDL- AND GATE					6-19-62	115599					
DESIGN			MODEL	SMS		1-3-63	EC116034					
DETAIL	RQ	3-4-62	SCALE	NONE		30.4.63	JT83687					
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									729855

C

729855

729856

STANDARDS CODE

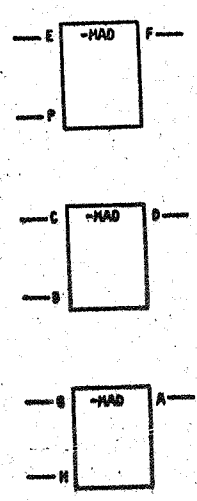
CARD CODE 729856

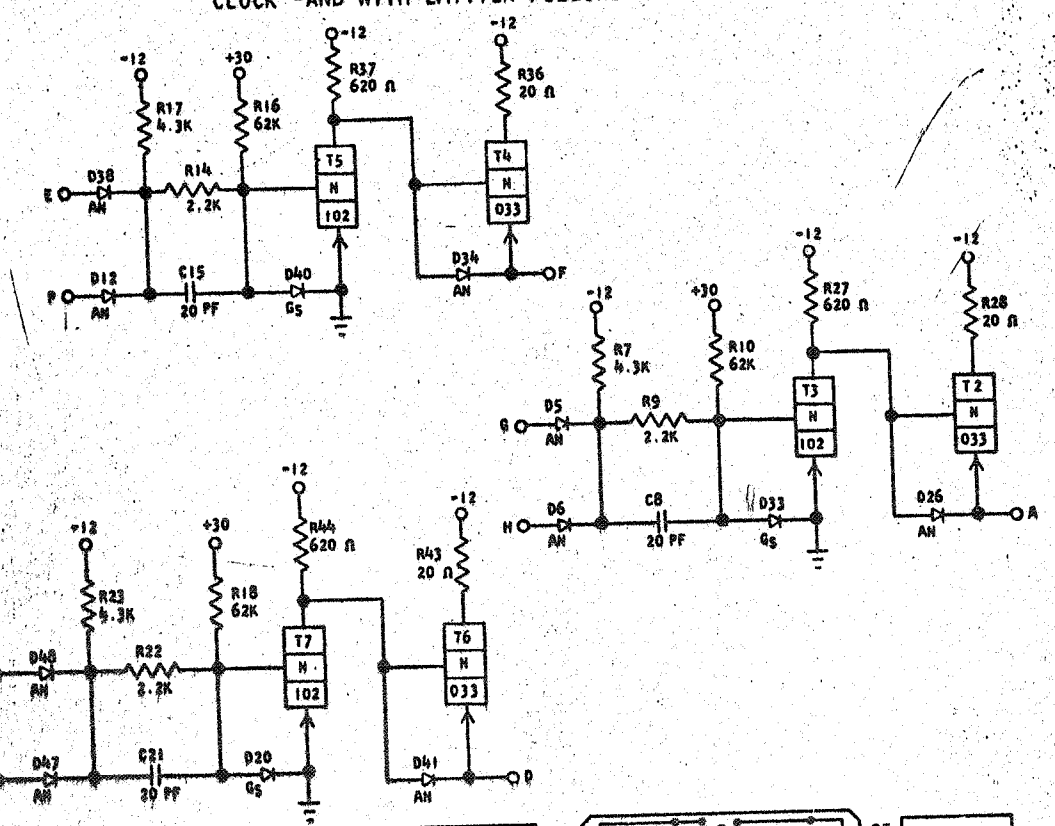
D G P -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370343

CLOCK -AND WITH EMITTER FOLLOWER DRIVER

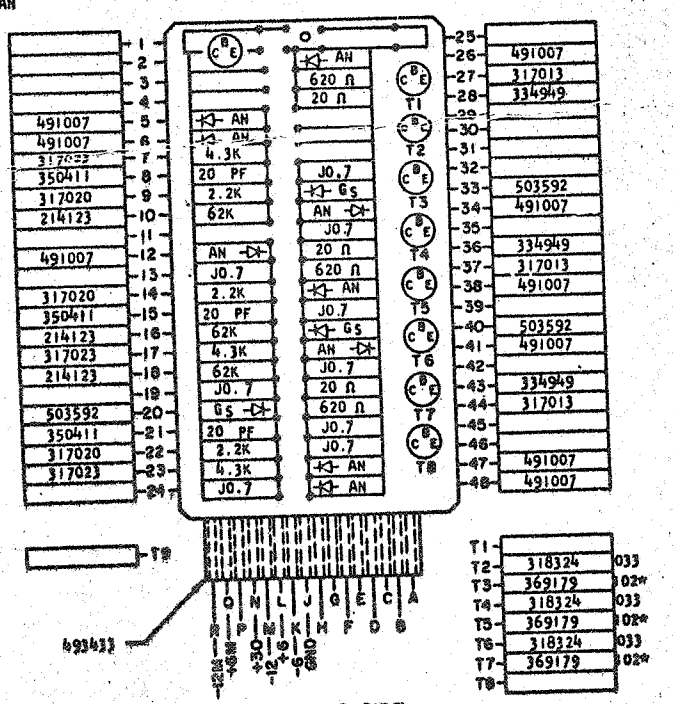




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN T5 TURNS ON, T4 OFF, OUTPUT IS UP
2. ANY INPUT UP, T5 OFF, T4 ON, OUTPUT IS DOWN
3. DELAY DRIVING CTDL LOADS
   TURN ON .28 USEC MAX
   TURN OFF .1 USEC MAX
4. DELAY DRIVING CLOCK LOAD
   TURN ON .15 USEC
   TURN OFF .15 USEC

PINS		SIGNAL R VE	WAVE SHAPE	LEVELS	MIN	MAX
E,P, C,D, B,H	T	INPUT		UP	1.44	6.24
				DOWN	-4.46	-6.24
F G A	U	OUTPUT		UP	-.89	.24
				DOWN	-7.44	-12.48



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CLOCK - AND WITH EMITTER FOLLOWER DRIVER				6-27-62	EC 115599					729856
			MODEL	SMS	30.4.63	JT 83687					
DESIGN			SCALE	NONE							
DETAIL	RQ	3-1-62	DRAW	LIS 3-17-62							
CHECK	WH	3-1-62	CHECK								
APPRO											

C

729856

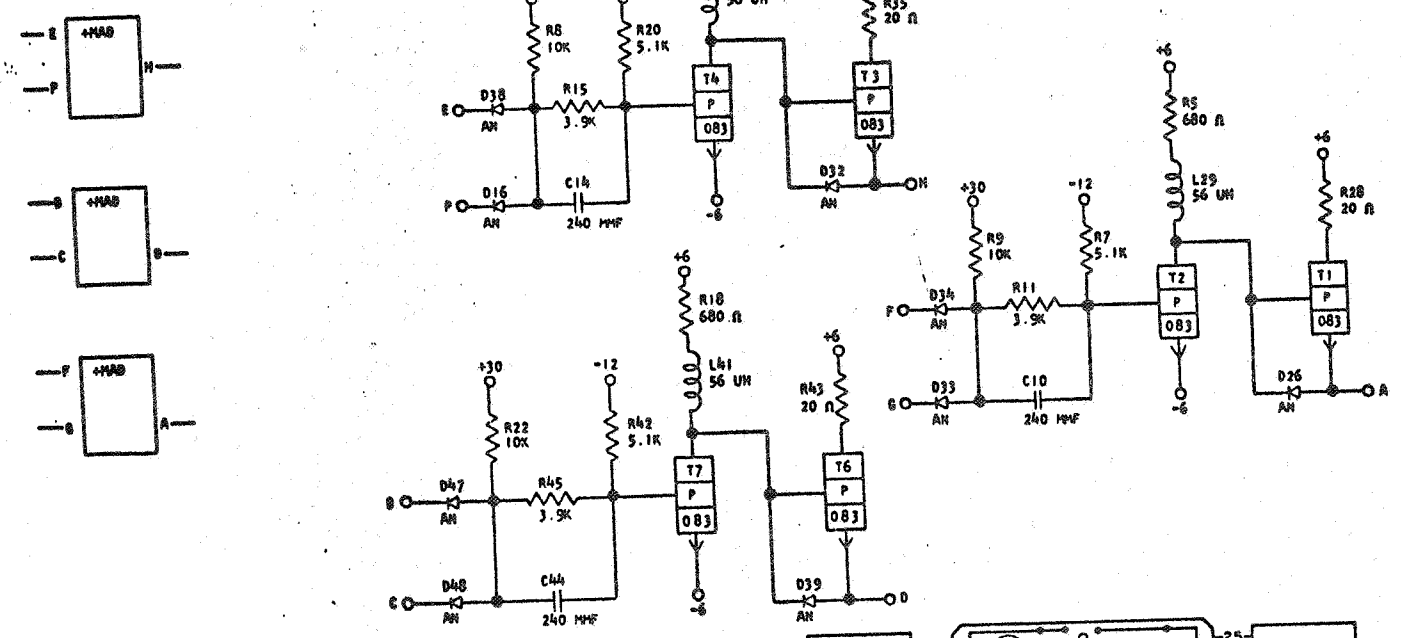
729857 STANDARDS CODE

CARD CODE 729857
D G Q -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370342

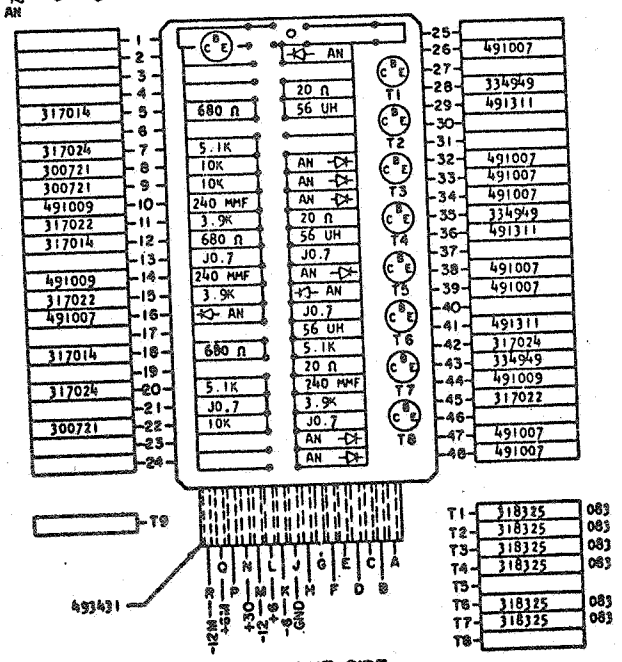
CLOCK + AND WITH EMITTER FOLLOWER DRIVER



SEQUENCE OF OPERATION

1. ALL INPUTS UP, T4 IS ON, T3 IS OFF, OUTPUT IS DOWN
2. ONE INPUT DOWN, T4 IS OFF, T3 IS ON, OUTPUT IS UP
3. DELAY WHEN DRIVING CTOL LOADS
   TURN ON .1 USEC MAX
   TURN OFF .25 USEC MAX
4. DELAY WHEN DRIVING CLOCK LOAD
   TURN ON .26 USEC MAX
   TURN OFF .12 USEC MAX

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, B	T	INPUT		UP	3.68	6.24
				DOWN	-4.46	-6.24
P,B, C	T	INPUT		UP	3.68	6.24
				DOWN	-4.46	-6.24
N,A, B	T	OUTPUT		UP	3.89	6.24
				DOWN	-4.46	-6.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CLOCK +AND WITH EMITTER FOLLOWER DRIVER				6-29-62	EC115599					
					30.4.63	TT83687					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729857

C

SHEET 9 OF 9 EC. 1138

CARD CODE 729857

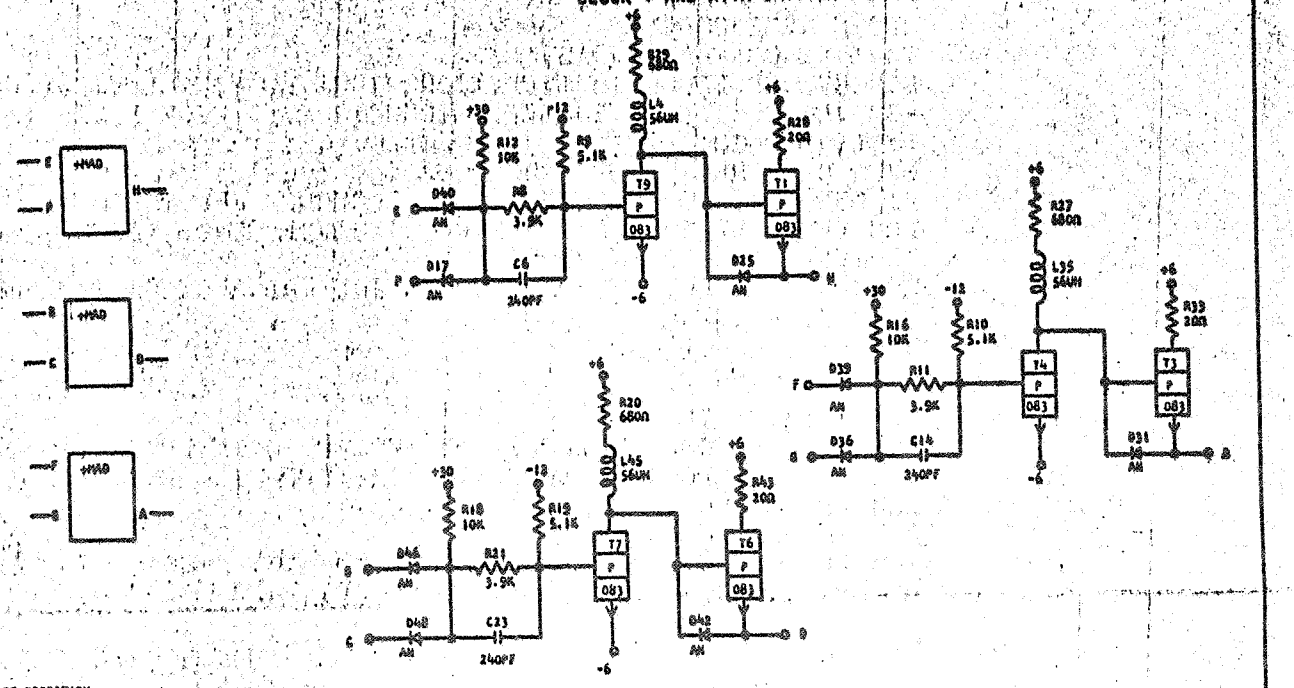
D G Q -

STANDARDS CODE 72965

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370342

CLOCK + AND WITH EMITTER FOLLOWER DRIVER



SEQUENCE OF OPERATION

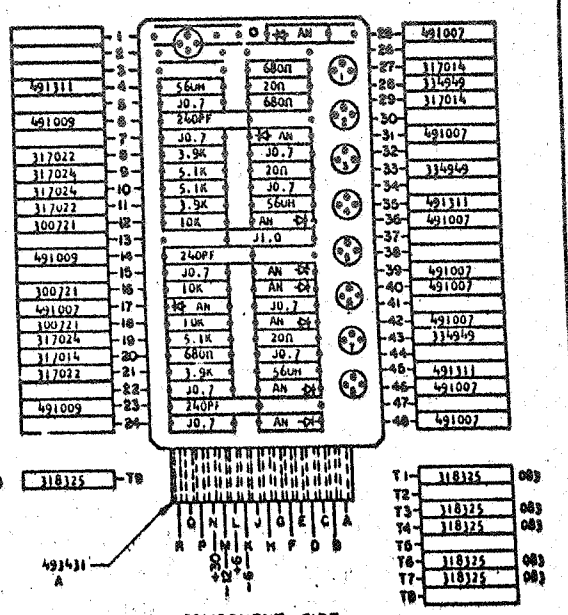
1. ALL INPUTS UP, T4 IS ON, T3 IS OFF, OUTPUT IS DOWN.
2. ONE INPUT DOWN, T4 IS OFF, T3 IS ON, OUTPUT IS UP.
3. DELAY WHEN DRIVING CTDL LOADS

   TURN ON .1 USEC MAX
   TURN OFF .25 USEC MAX

4. DELAY WHEN DRIVING CLOCK LOAD

   TURN ON .26 USEC MAX
   TURN OFF .12 USEC MAX

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, B	T	INPUT		UP	3.68	6.24
				DOWN	-4.46	-6.24
P,S, C	T	INPUT		UP	3.68	6.24
				DOWN	-4.46	-6.24
H,A, B	T	OUTPUT		UP	3.89	6.24
				DOWN	-4.46	-6.24



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-CLOCK +AND WITH EMITTER FOLLOWER DRIVER	6-29-62	115599					729857
	7-19-62	0117839					
DESIGN MODEL SMS 1401							
DETAIL RG 1-1-62 SCALE NONE							
CHECK WH 1-1-62 DRAWN [illegible] 6-14-62							

C

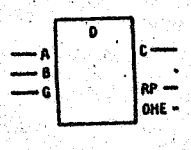
CARD CODE	729858
DKA-	

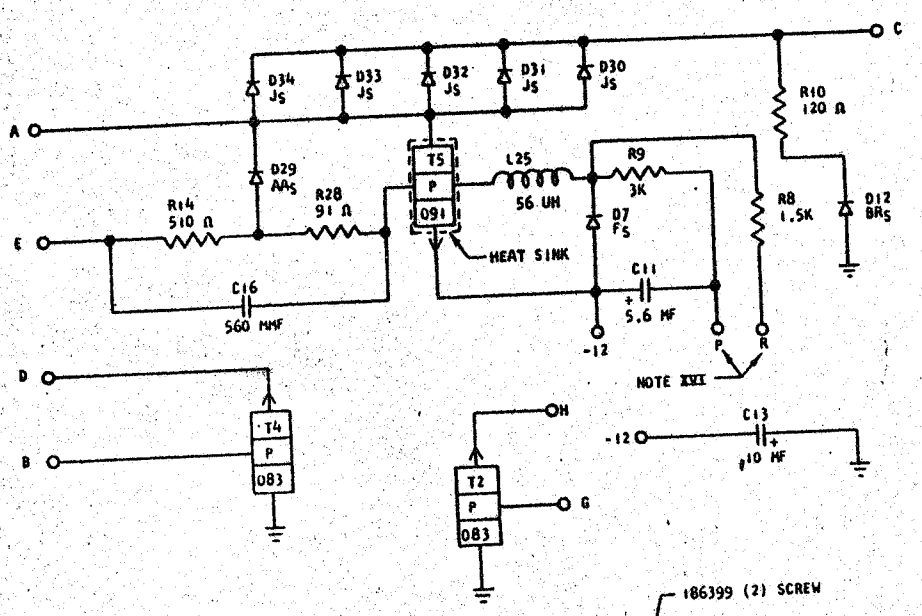
STANDARDS CODE 729858

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370443

ALLOY-DRIVER, CURRENT





SEQUENCE OF OPERATION

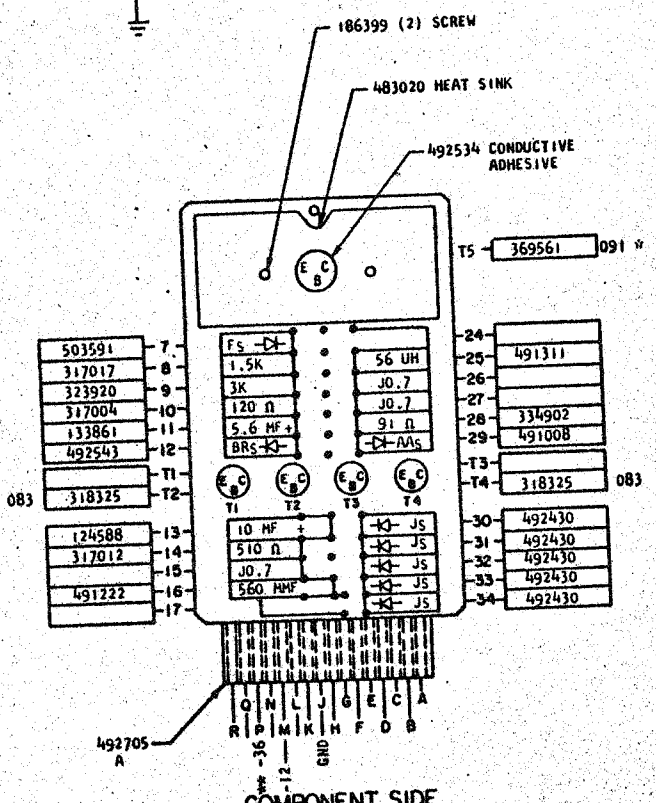
1. H, D, E TIED TOGETHER
2. DOWN OUTPUT AT B, G, T4, T2 OFF, BASE OF T5 GOES TO A MINUS LEVEL AND OFF
3. WITH T5 OFF ITS COLLECTOR IS AT PLUS LEVEL; THIS FORWARD BIAS THE DIODES D30 TO 34 ALLOWING CURRENT TO FLOW

NOTE: FOR -36V USE AS IS, FOR -20V, JUMPER BACK PANEL PINS "P" AND "R"

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B	U	ACTIVATE STORAGE		UP	-5.26	0.24
				DOWN	-7.44	-12.5
G	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
A		+34				
A		GROUND				

DELAY

1. TURN-ON DELAY SHALL BE MEASURED FROM THE 90% POINT OF THE FALL OF THE INPUT PULSE TO THE 90% POINT ON THE RISE OF THE OUTPUT PULSE AS MEASURED ACROSS R_L AND SHALL BE NOT GREATER THAN 200 NANO SECONDS.
2. TURN-OFF DELAY SHALL BE MEASURED FROM THE 10% POINT ON THE RISE OF THE INPUT PULSE TO THE 10% POINT ON THE FALL OF THE OUTPUT PULSE AS MEASURED ACROSS R_L AND SHALL BE NOT GREATER THAN 100 NANO SECONDS.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- ALLOY- CURRENT DRIVER				6-27-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729858

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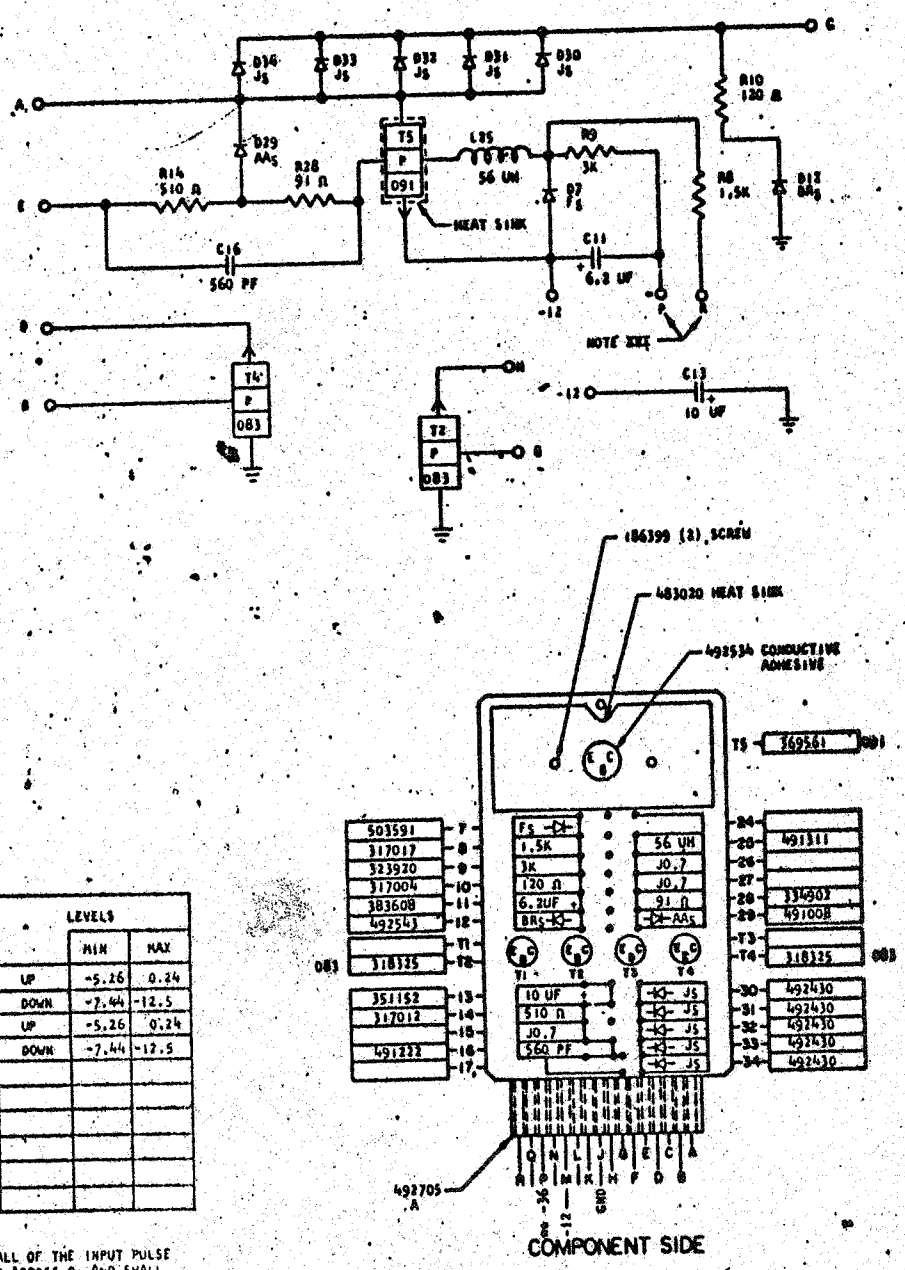
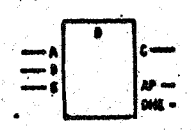
DKA-

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370443

ALLOY-DRIVER, CURRENT





SEQUENCE OF OPERATION

1. N, B, E TIED TOGETHER
2. BOTH OUTPUT AT B, C, T4, T2 OFF, BASE OF T5 GOES TO A MINUS LEVEL AND OFF
3. WITH T5 OFF ITS COLLECTOR IS AT PLUS LEVEL; THIS FORWARD BIAS THE DIODES D30 TO 34 ALLOWING CURRENT TO FLOW

NOTE: FOR -36V USE AS IS, FOR -20V, JUMPER BACK PANEL PINS "M" AND "R"

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B	U	ACTIVATE STORAGE		UP	-5.26	0.24
				DOWN	-7.44	-12.5
C	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
A		+34				
A		GROUND				

DELAY

1. TURN-ON DELAY SHALL BE MEASURED FROM THE 50% POINT OF THE FALL OF THE INPUT PULSE TO THE 90% POINT ON THE RISE OF THE OUTPUT PULSE AS MEASURED ACROSS R_L AND SHALL BE NOT GREATER THAN 200 NANO SECONDS.
2. TURN-OFF DELAY SHALL BE MEASURED FROM THE 10% POINT ON THE RISE OF THE INPUT PULSE TO THE 10% POINT ON THE FALL OF THE OUTPUT PULSE AS MEASURED ACROSS R_L AND SHALL BE NOT GREATER THAN 100 NANO SECONDS.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- ALLOY- CURRENT DRIVER				6-29-62	115599					729858
			MODEL	SMS 1	1-3-63	EC 116034					
DESIGN			SCALE	NONE	30.4.63	TF 83687					
DETAIL	RQ	3-1-62	DRAW	LJG 3-17-62							
CHECK	WH	3-1-62	CHECK								
APPRD											

C

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729859

STANDARDS CODE

CARD CODE 729859

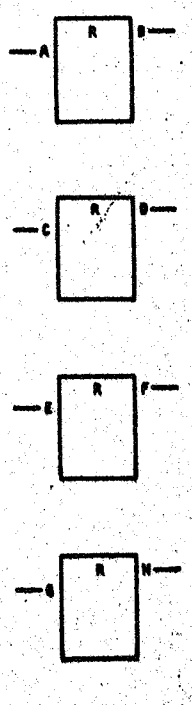
FP --

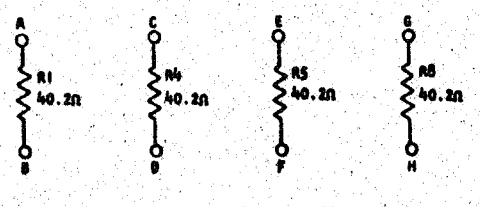
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371453

ALLOY - LOAD RESISTOR - 40.2Ω 2W

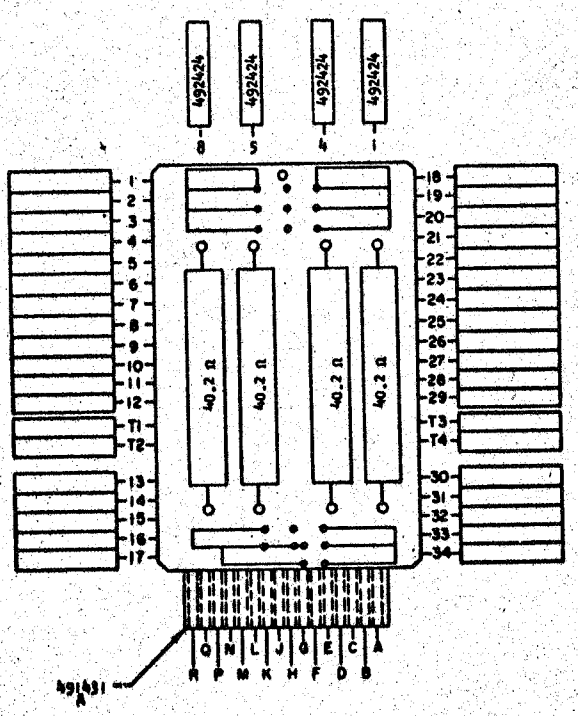
MOUNT CARD ON ONE INCH CENTERS NOTE XXX





APPLICATION

1. USED AS TERMINATING RESISTOR PRINT BUFFER ARRAY



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY LOAD RESISTOR 40.2Ω 2W					6-12-62	EC 115599					
						30-4-63	TT83687					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

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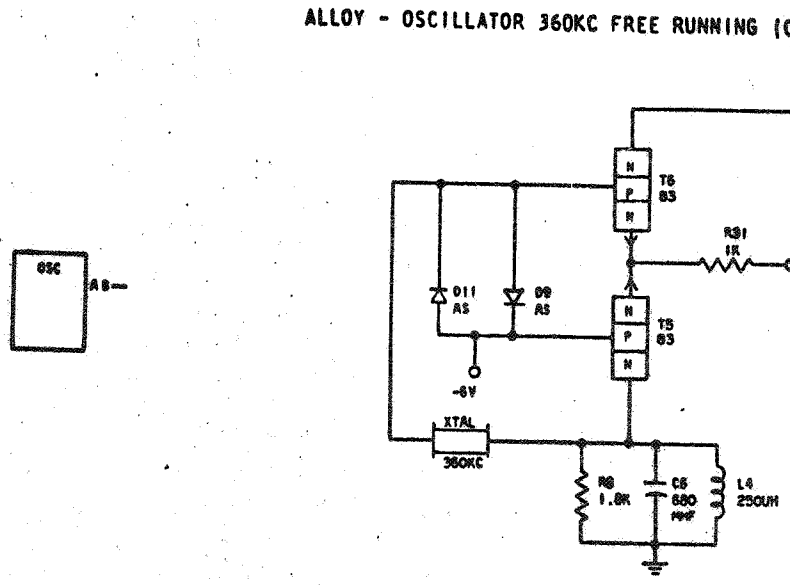
CARD CODE 729860
FT --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371405

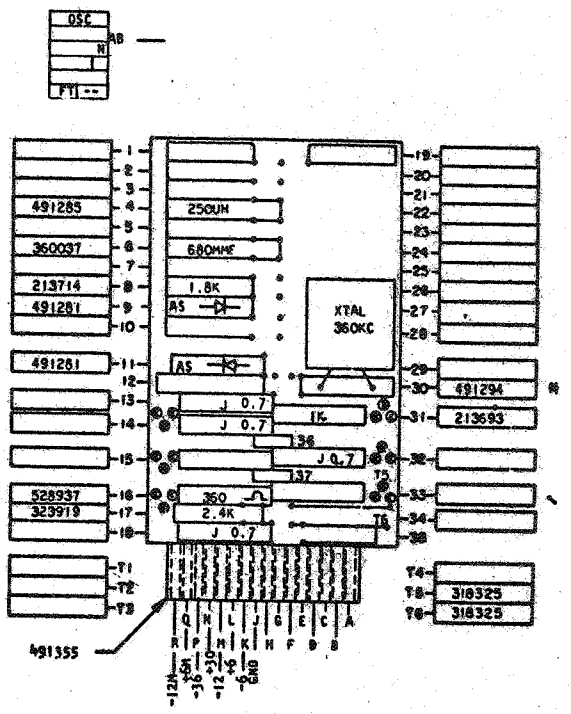
ALLOY - OSCILLATOR 360KC FREE RUNNING (CRYSTAL)



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A MUST BE TIED TO PIN B

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A	OUTPUT	360 KC	UP	.697	.86
			DOWN	-.92	-2.04



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARDS	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY				6.19.62	EC115599					
	OSC. F/R NPN 360KC (CRYSTAL)				30.4.63	7783687					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

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729860

729860

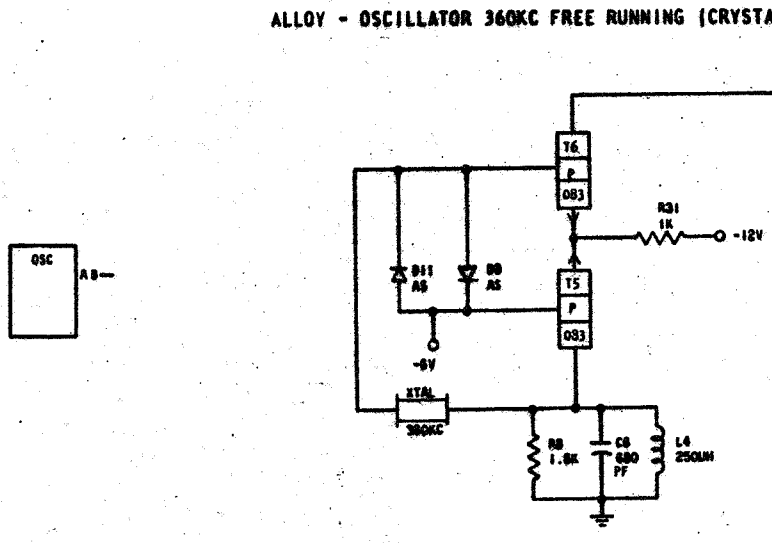
CARD CODE 729860

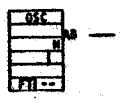
FT --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371405

ALLOY - OSCILLATOR 360KC FREE RUNNING (CRYSTAL)

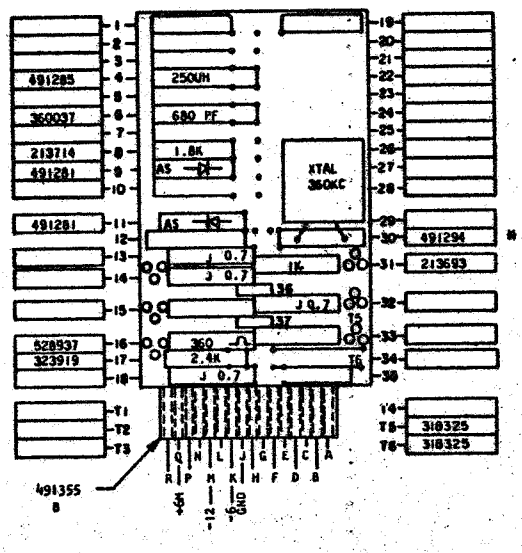




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A MUST BE TIED TO PIN B

PINS	SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
A	OUTPUT	360 KC	UP	.697	.86
			D WH	-.92	-2.04



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729860
NAME	CARD ASM TSTR - ALLOY					6-29-62	115599						
OSC. F/R NPN 360KC (CRYSTAL)						8-28-63	117802						
DESIGN			MODEL	SMS		19.2.64 TA 1841D							
DETAIL	RO	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRO			CHECK										

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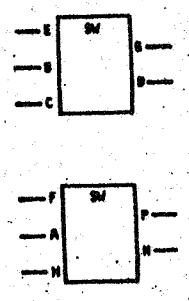
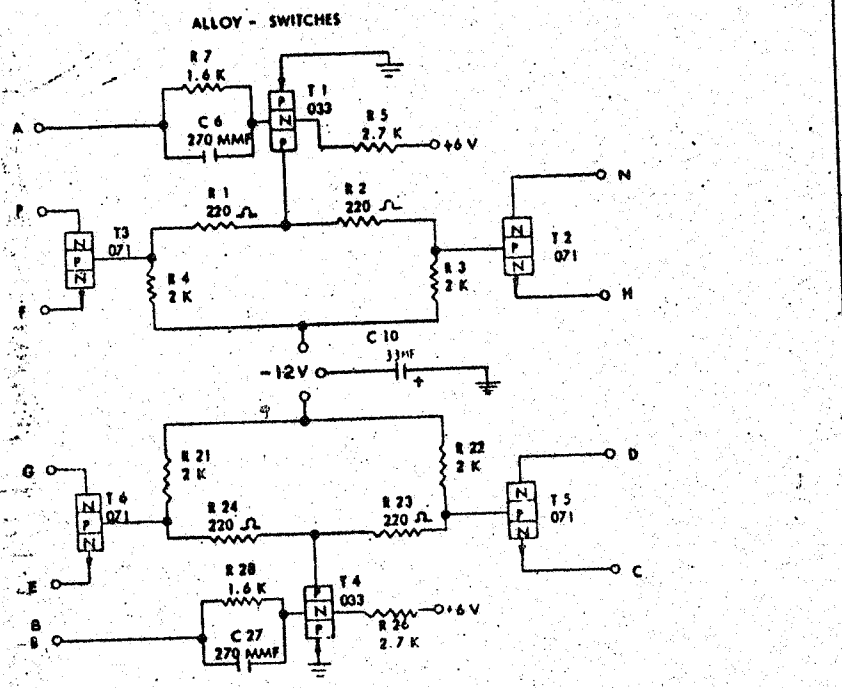
729861

CARD CODE 729861
FW --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371490



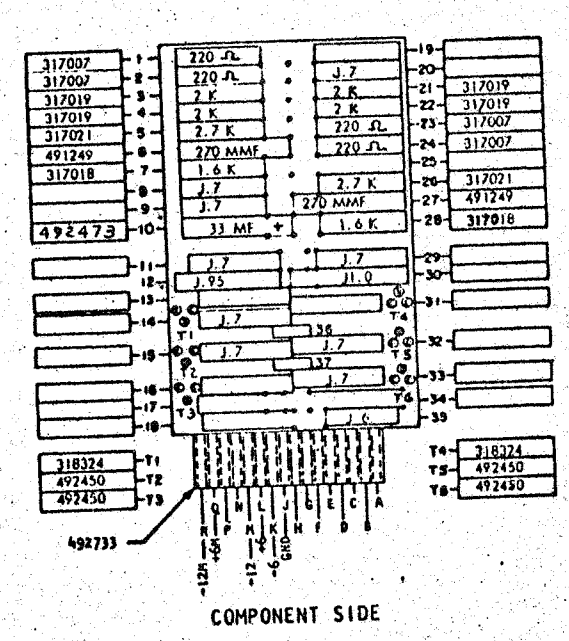


SEQUENCE OF OPERATION

1. COLLECTORS OF T3, T2, T6, T5 ARE TIED TO +6 THRU A TERMINATING RESISTOR CARD AND THEIR EMITTERS ARE TIED TO CURRENT DRIVER SOURCE CARD THRU WINDINGS IN CORE ARRAY.

2. A DOWN INPUT AT A WILL TURN T1 ON AND T3 OR T2 DEPENDING ON WHICH TRANSISTOR IS SUPPLIED EMITTER CURRENT FROM CURRENT DRIVER CARD.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,B	B	INPUT		UP	-.2	+.3
				DOWN	-5.6	-12



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY - SWITCHES				4-7-62	CL15599					729861
DESIGN			MODEL	SMS	30.4.63	JT83687					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRD			CHECK								

C

729861

729862 STANDARDS CODE

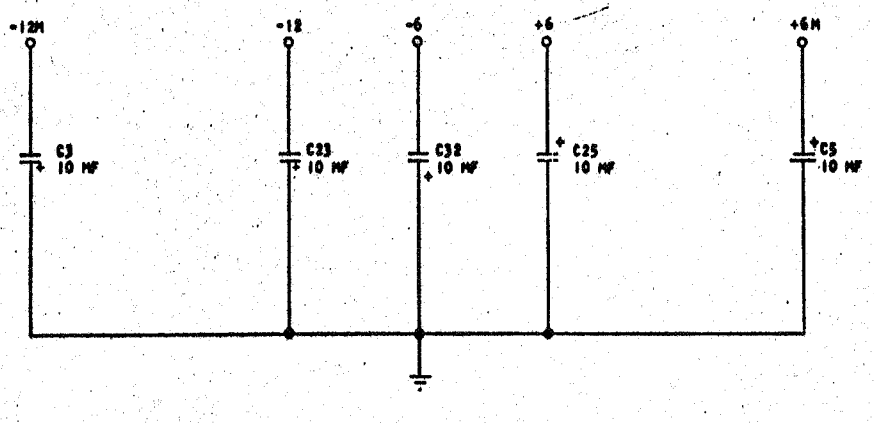
CARD CODE 729862
GJ --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371501

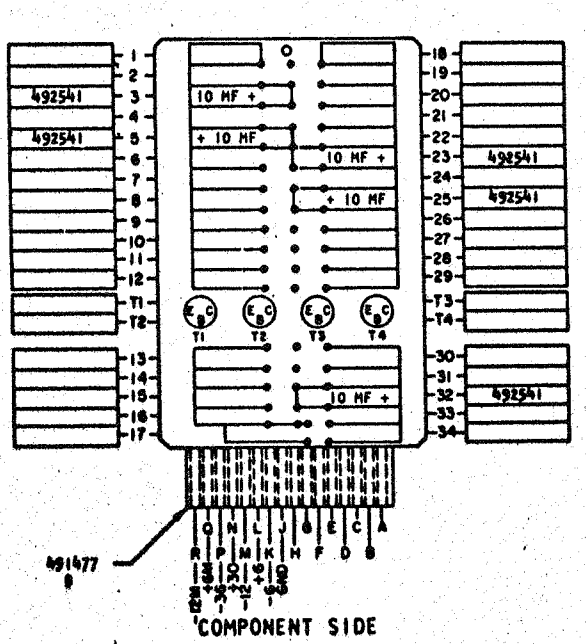
GENERAL PURPOSE FILTER CARD

FILT



APPLICATION

1. THIS CARD USED TO FILTER SUPPLY VOLTAGES TO GROUND POTENTIAL



COMPONENT SIDE

C

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR- GENERAL PURPOSE FILTER CARD				6-27-62	PC115599						729862
DESIGN			MODEL	SMS	30.4-68	7783687						
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	MH	3-1-62	DRAW	LIG 3-17-62								
APPRO			CHECK									

729862

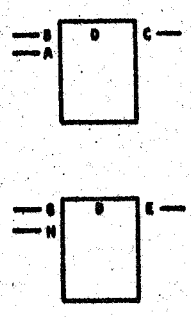
STANDARDS CODE	729863

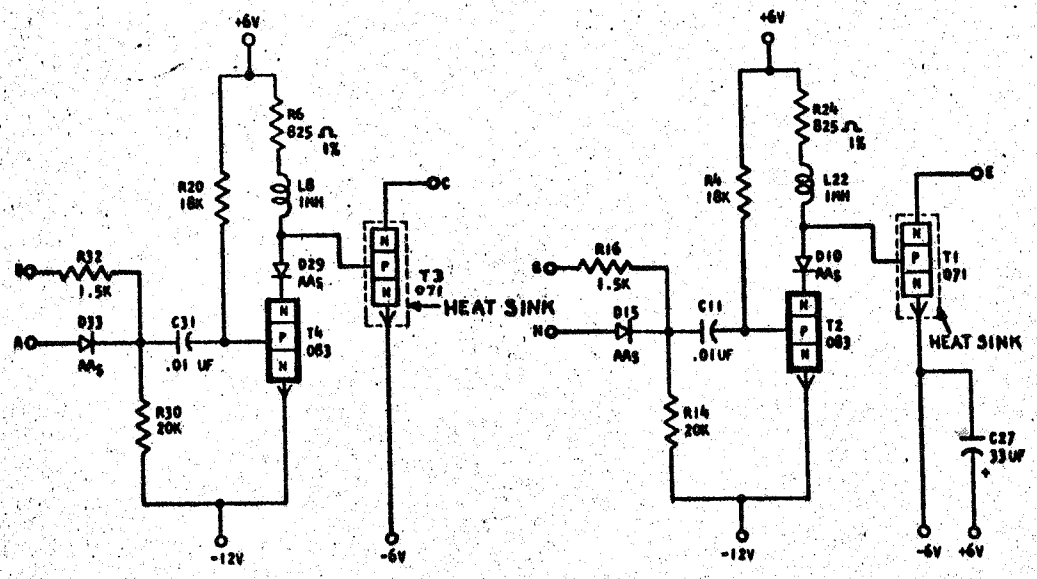
CARD CODE	729863
HN --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371463

ALLOY-DRIVERS, READ WRITE VM



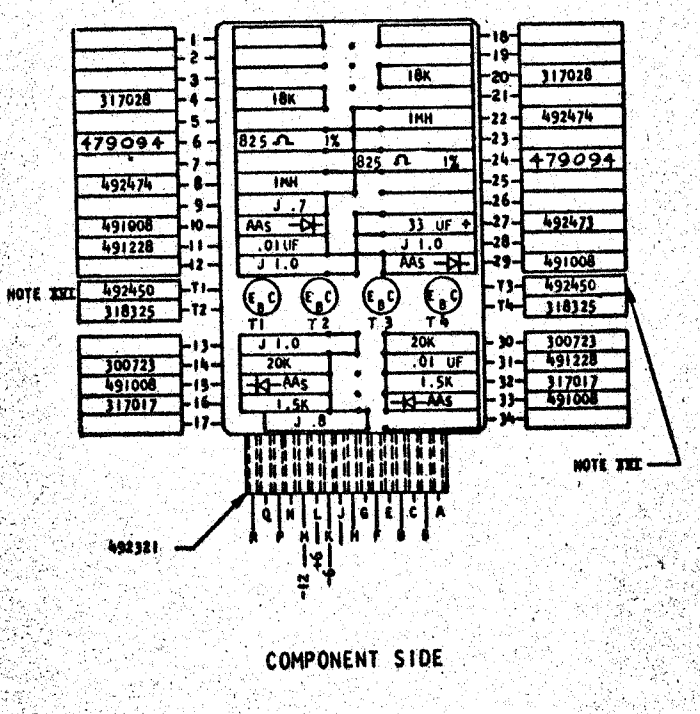


SEQUENCE OF OPERATION

1. T4, T2 ON; T3, T1 OFF
2. DOWN INPUT AT B 0.5 U SEC BEFORE DOWN INPUT AT A TURNS T4 OFF T3 ON
3. WAVE FORM AT C OR E NOT SHOWN AS THE FUNCTION OF T1 AND T3 IS CURRENT OUTPUT
4. DELAY

	MAXIMUM
TURN ON	.3 USEC
TURN OFF	.37 USEC

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,G	U	INPUT GATE		UP	-0.54	0.24
				DOWN	-7.44	-12.5
A,H	U	INPUT SET		UP	0.0	-0.1
				DOWN	-11.5	-12.5
INPUT OF	TD	BASE T1, T3		UP	-5.8	
				DOWN	-11.8	



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729863
NAME	CARD ASM TSTR - ALLOY DRIVERS - READ WRITE VM					6-27-62	EC115599						
						30-4-63	JT83687						
DESIGN			MODEL	SMS									
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WM	3-1-62	DRAW	LIG	3-17-62								
APPRO			CHECK										

C

729863

729864

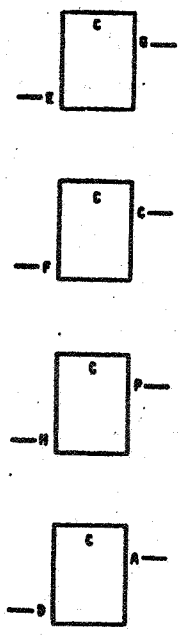
CARD CODE 729864

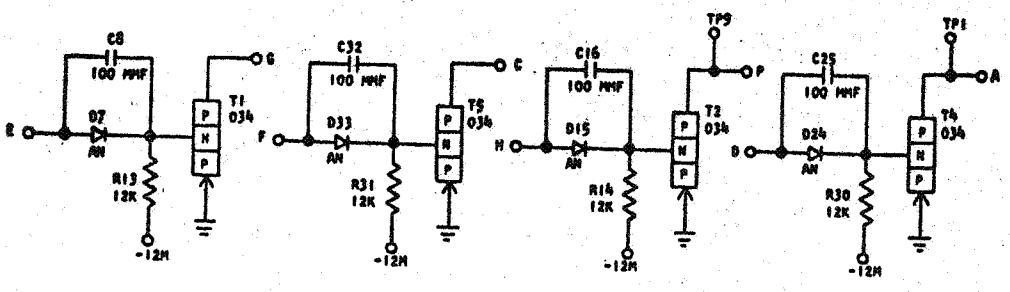
JF --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371579

CTDL - HIGH SPEED ONE WAY PNP NO LOADS





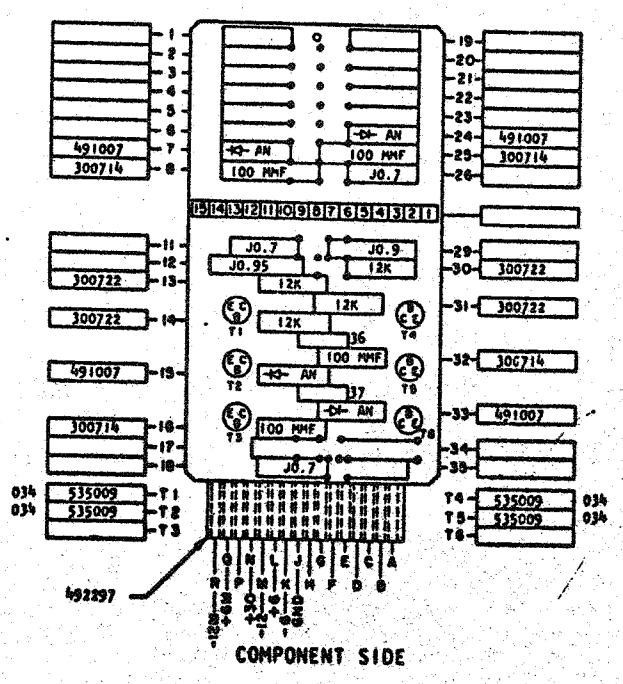
SEQUENCE OF OPERATION

1. WHEN THE INPUT IS UP, THE TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. WHEN THE INPUT IS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. ALL OUTPUTS MUST BE COLLECTOR LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E,F, H,D	I	INPUT		UP	1.44	6.24
				DOWN	-.74	-6.24
G,C, P,A	O	OUTPUT		UP	-.54	.24
				DOWN	-7.44	-12.48

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.25
TURN OFF	0.10	0.40



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-CTDL - HIGH SPEED 1 WAY PNP NO LOADS	6-27-62	P115599					729864
DESIGN MODEL SMS	30.4.63	TT83687					
DETAIL RR 3-1-62 SCALE NONE							
CHECK WH 3-1-62 DRAW LIB 3-17-62							
APPRO CHECK							

C

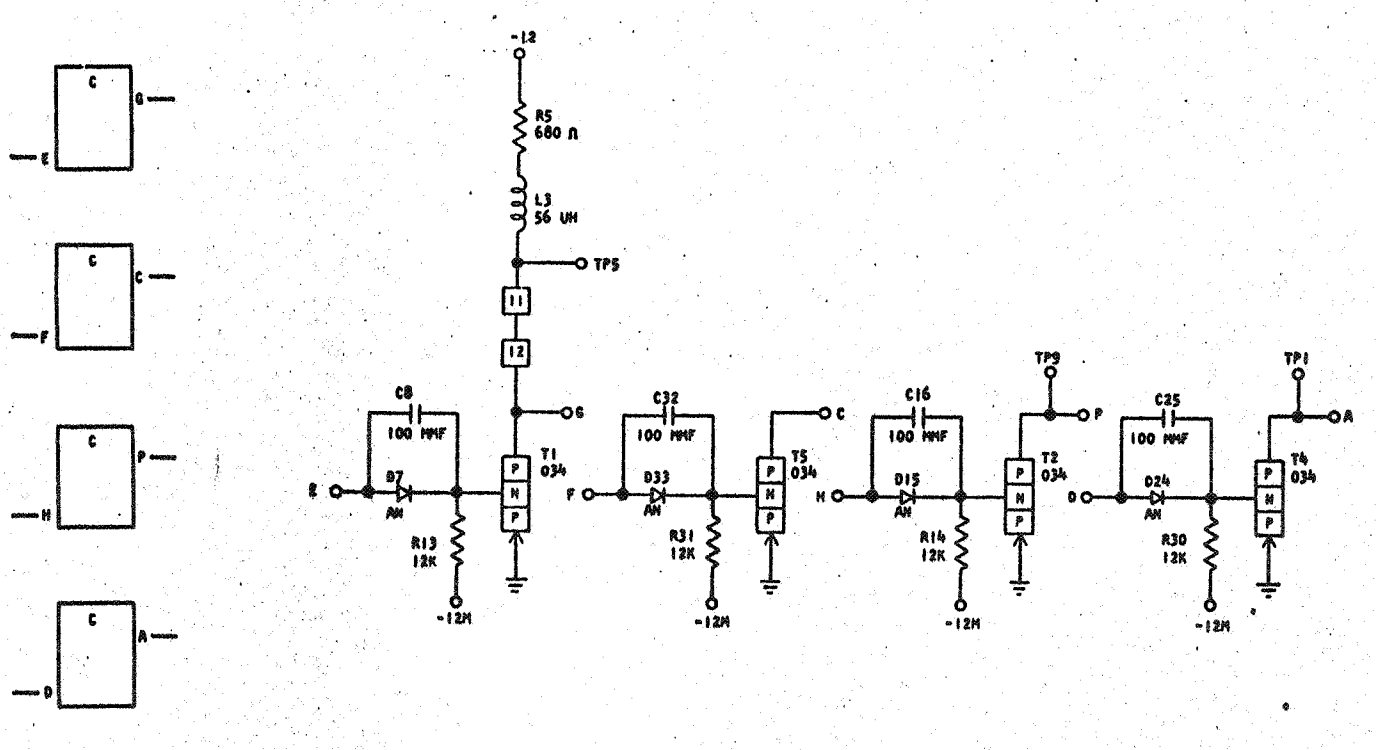
729865 STANDARDS CODE

CARD CODE	729865
JF VA	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371578

CTDL HIGH SPEED ONE WAY PNP ONE LOAD



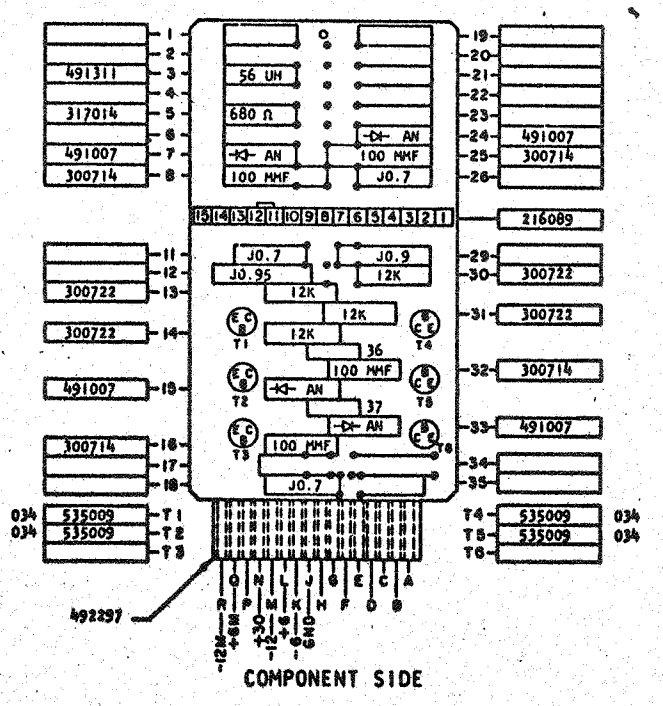
SEQUENCE OF OPERATION

1. WHEN THE INPUT IS UP, THE TRANSISTOR IS OFF, THE OUTPUT IS DOWN.
2. WHEN THE INPUT IS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP.
3. T2,T4,T5 MUST BE COLLECTOR LOADED.
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E,F H,D	T	INPUT		UP	1.44	6.24
				DOWN	-.74	-6.24
G,C P,A	U	OUTPUT		UP	-.54	.24
				DOWN	-7.44	-12.48

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.25
TURN OFF	0.19	0.40



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729865
NAME	CARD ASM TSTR-CTDL HIGH SPEED ONE WAY PNP ONE LOAD					2-27-62	EC 115599						
DESIGN			MODEL	SMS		30.4.63	JT 83687						
DETAIL	RO	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRO			CHECK										

C

729865

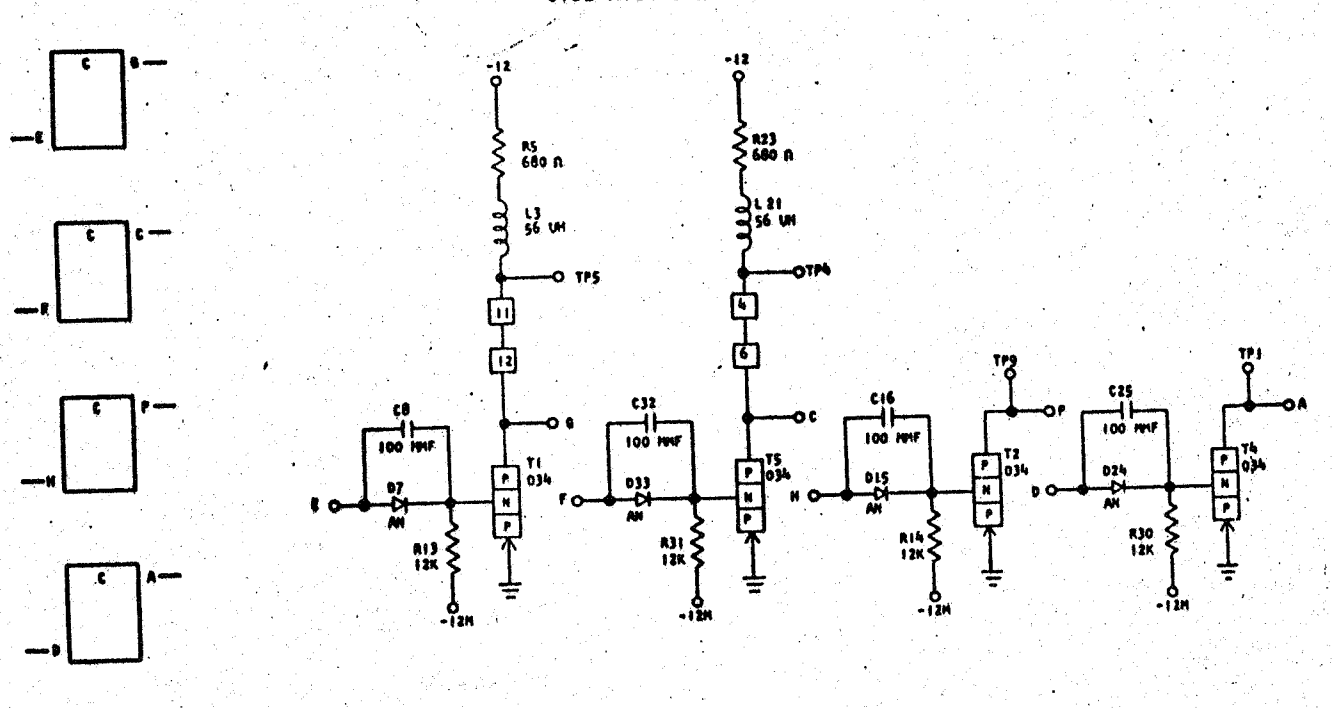
CARD CODE	729866
JF VN	

729866

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371577

CTDL HIGH SPEED ONE WAY PNP TWO LOADS



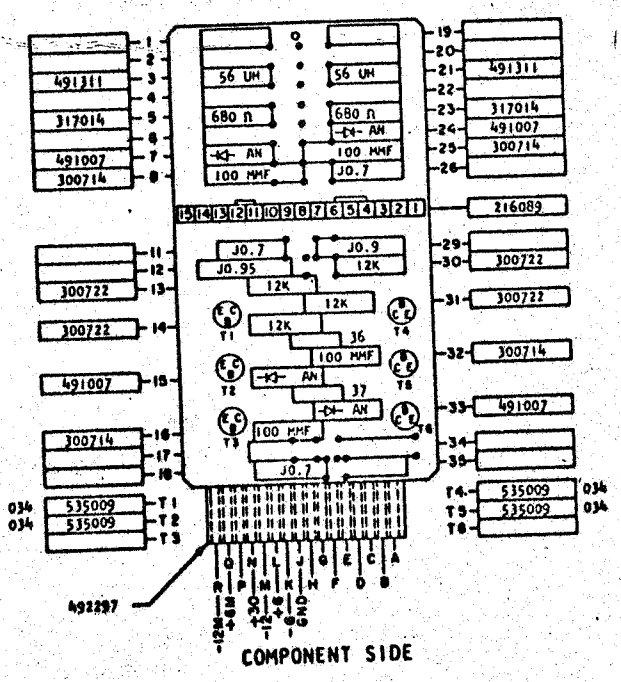
SEQUENCE OF OPERATION

1. WHEN THE INPUT IS UP, THE TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. WHEN THE INPUT IS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. T2, T4 COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, H,D	T	INPUT		UP	1.44	6.24
				DOWN	-.74	-6.24
B,C, P,A	U	OUTPUT		UP	-.54	.24
				DOWN	-7.44	-12.48

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.25
TURN OFF	0.10	0.40



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- CTDL HIGH SPEED ONE WAY PNP TWO LOADS					6-27-62	EC 115599					
DESIGN			MODEL	SMS		30-4-63	JT 83687					
DETAIL	RG	7-1-62	SCALE	NONE								
CHECK	WN	7-1-62	DRAW	LIG	7-17-62							
APPRO			CHECK									

C

729866

729867

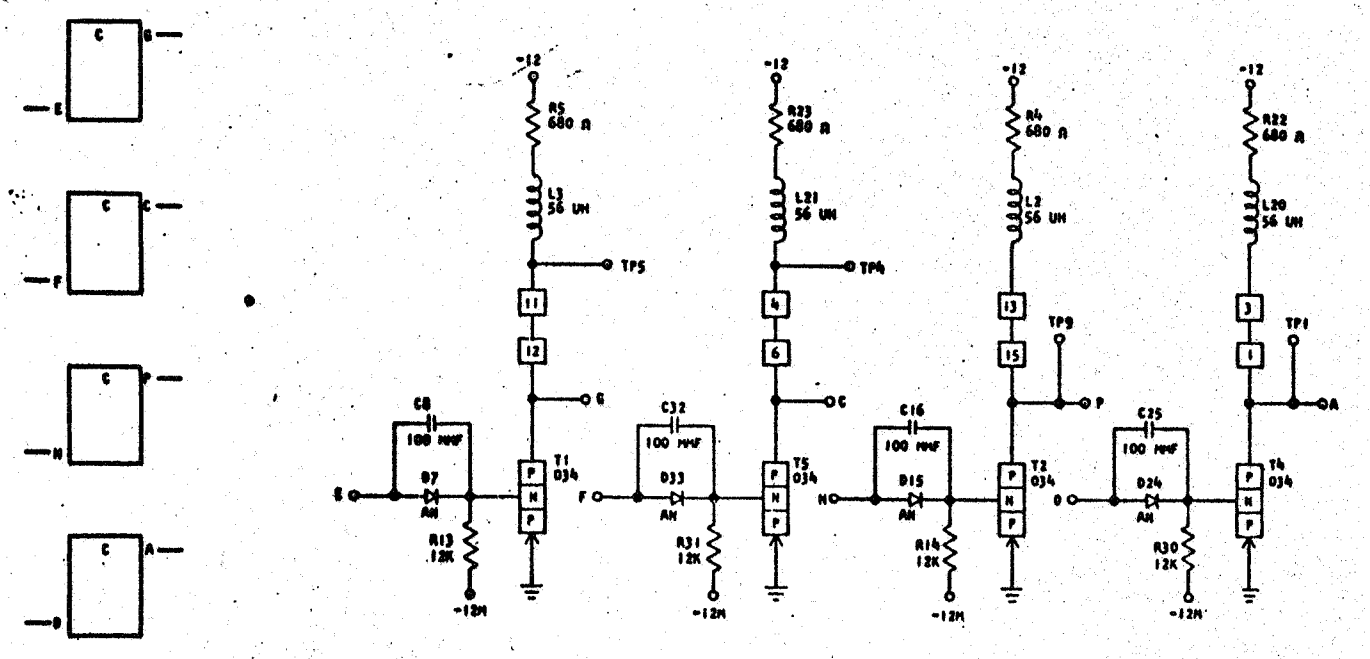
CARD CODE 729867

JF VP

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371576

CTDL HIGH SPEED ONE WAY PNP ALL LOADS



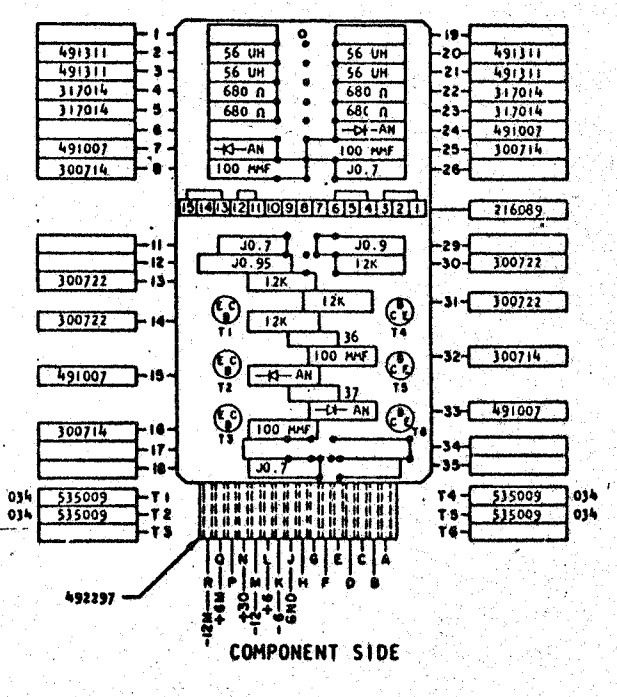
SEQUENCE OF OPERATION

1. WHEN THE INPUT IS UP, THE TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. WHEN THE INPUT IS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E,F H,D	T	INPUT		UP	1.44	6.24
				DOWN	-.74	-6.24
G,C P,A	U	OUTPUT		UP	-.54	.24
				DOWN	-7.44	-12.48

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.25
TURN OFF	0.10	0.40



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL HIGH SPEED ONE WAY PNP ALL LOADS					6-29-62	EC 115599					729867
						30-4-63	JT 83687					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

C

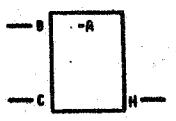
729868 STANDARDS CODE

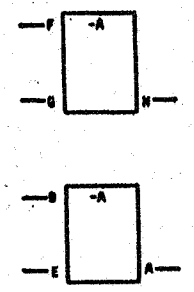
CARD CODE 729868
JG --

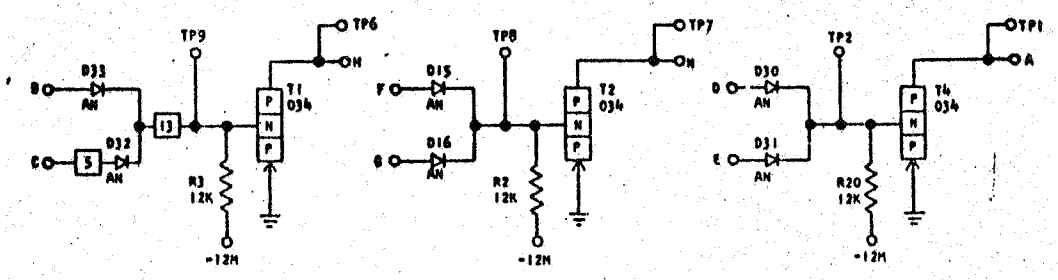
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371583

CTDL HIGH SPEED - TWO WAY "AND" PNP NO LOADS







SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. ALL OUTPUTS MUST BE COLLECTOR LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

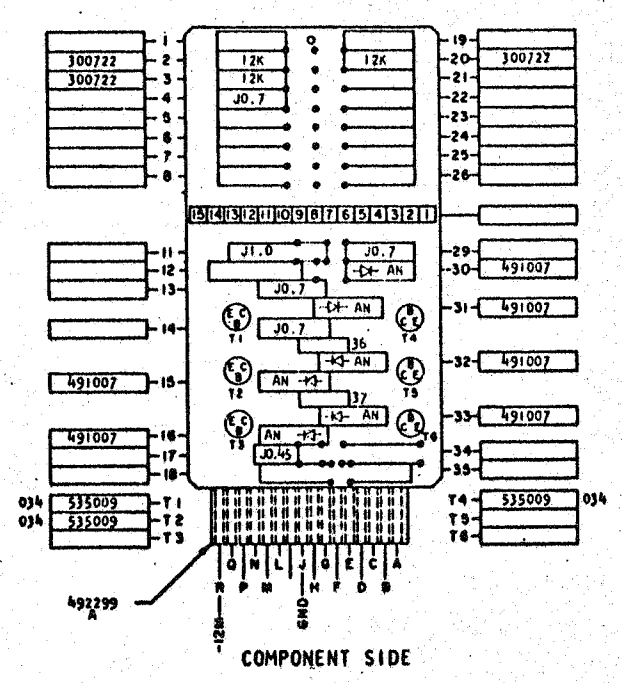
PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
B,F,D, C,G,E	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
H,N,A	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



CIRCUIT AND PACKAGING STANDARD

APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL HIGH SPEED-TWO WAY "AND" PNP NO LOADS					6-29-62	EC 115599					
DESIGN			MODEL	SMS		30.4.63	TT 83687					
DETAIL	RO	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729868

C

729868

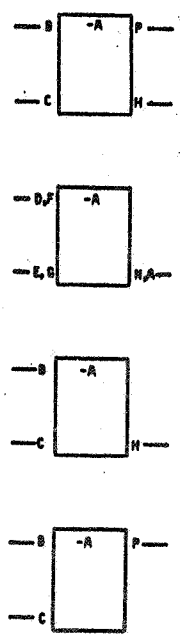
STANDARDS CODE 729869

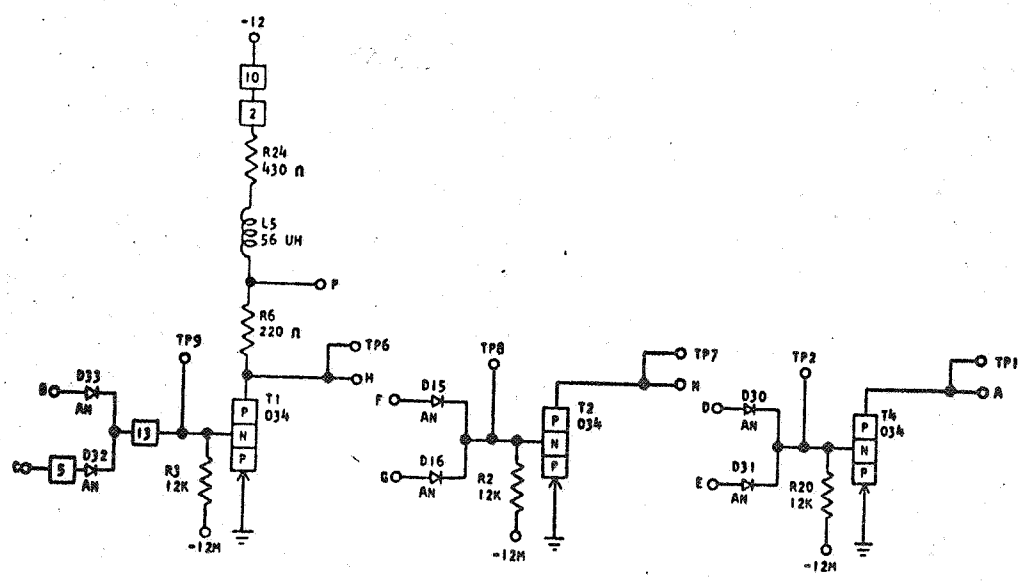
CARD CODE 729869
JG VV

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371582

CTDL HIGH SPEED-TWO WAY "AND" PNP ONE LOAD

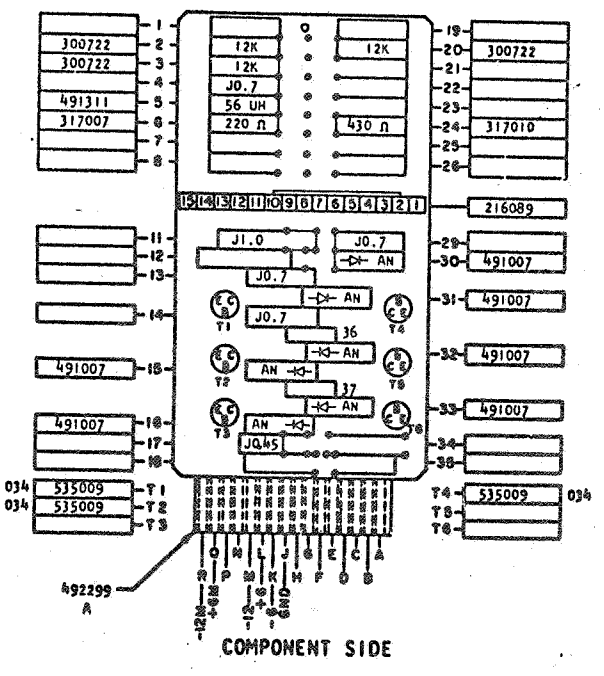




SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, THE TRANSISTOR IS ON THE OUTPUT IS UP
3. T2, T4 MUST BE COLLECTOR LOADED
4. PIN P IS CURRENT MODE OUTPUT
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,C	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
N	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
P	P	OUTPUT		UP	-4.93	-3.54
				DOWN	-8.82	-12.48
D,F, E,G	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
N,A	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48



DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS.
EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- CTDL HIGH SPEED-TWO WAY "AND" PNP ONE LOAD					6-29-62	EC115599					729869
DESIGN			MODEL	SMS		30-4-63	7783687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

C

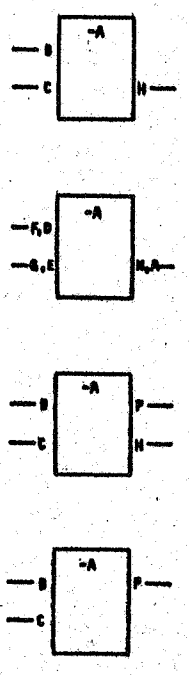
729870

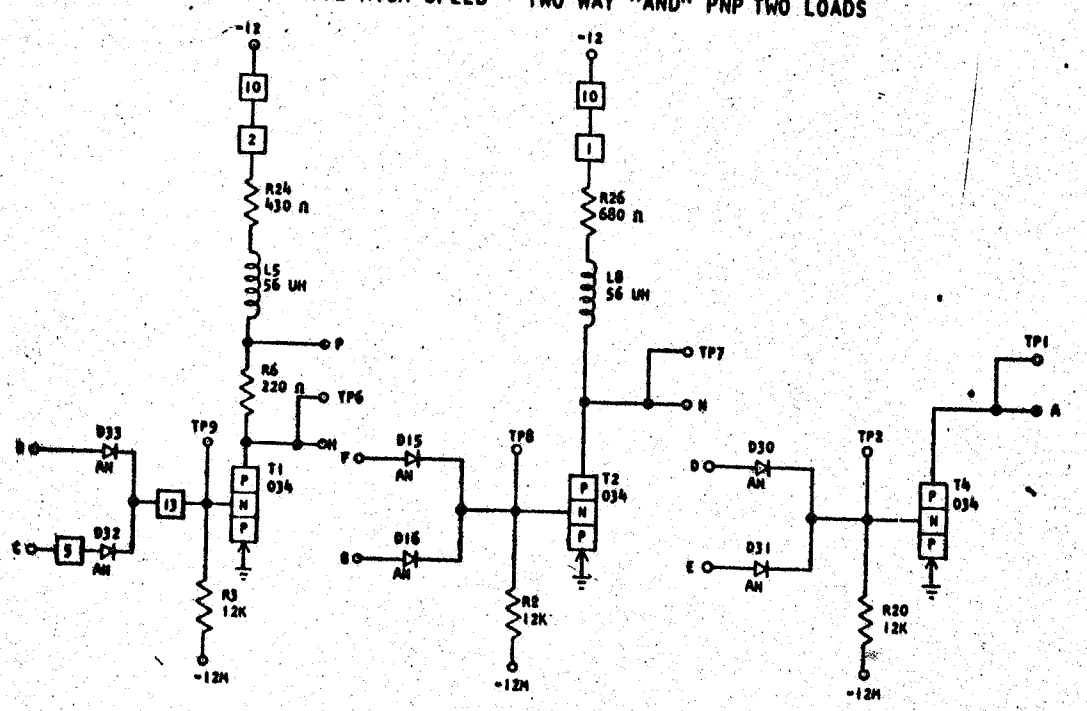
CARD CODE 729870
JG VW

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371581

CTDL HIGH SPEED - TWO WAY "AND" PNP TWO LOADS





SEQUENCE OF OPERATION

1. ANY INPUT UP, THE TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. T4 MUST BE COLLECTOR LOADED
4. PIN P IS CURRENT MODE OUTPUT
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

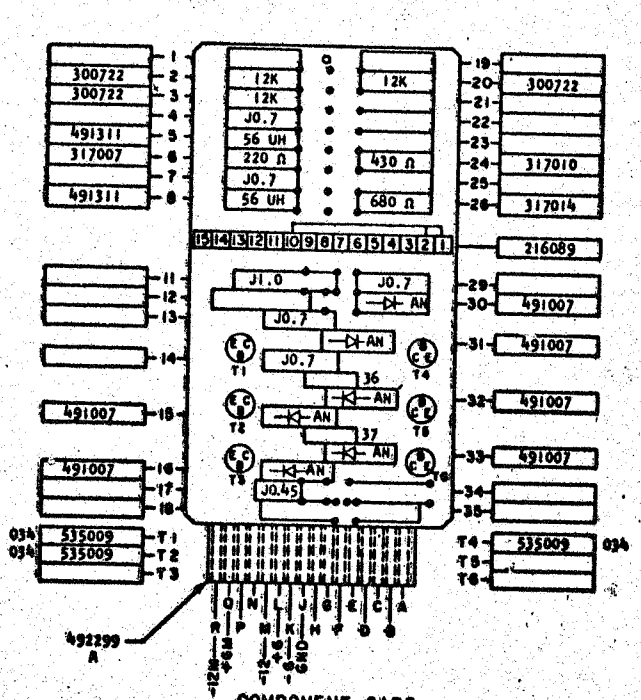
PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,C	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
H	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
P	P	OUTPUT		UP	-4.93	-3.54
				DOWN	-8.82	-11.48
F,D	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
D	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
D,E	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
A	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-CTDL HIGH SPEED-TWO WAY "AND" PNP TWO LOADS					6-27-62	EC 115599					
DESIGN			MODEL SMS		10-4-62	JT83687					
DETAIL	RQ	3-1-62	SCALE NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729870

C

729871

STANDARDS CODE

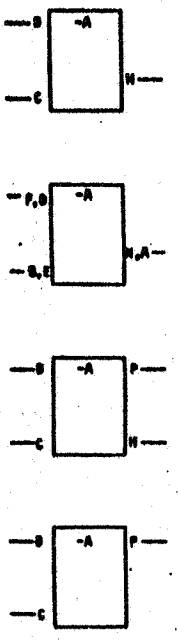
CARD CODE 729871

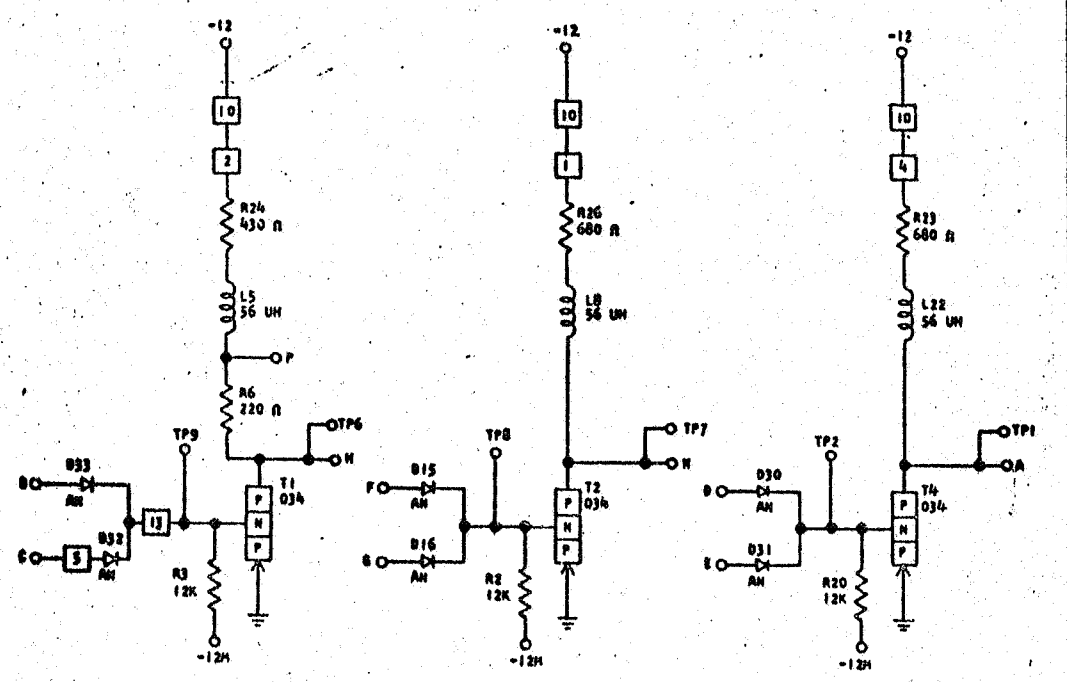
JG WW

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371580

CTDL HIGH SPEED-TWO WAY "AND" PNP ALL LOADS





SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, TRANSISTOR ON, THE OUTPUT IS UP
3. PIN P IS CURRENT MODE OUTPUT
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

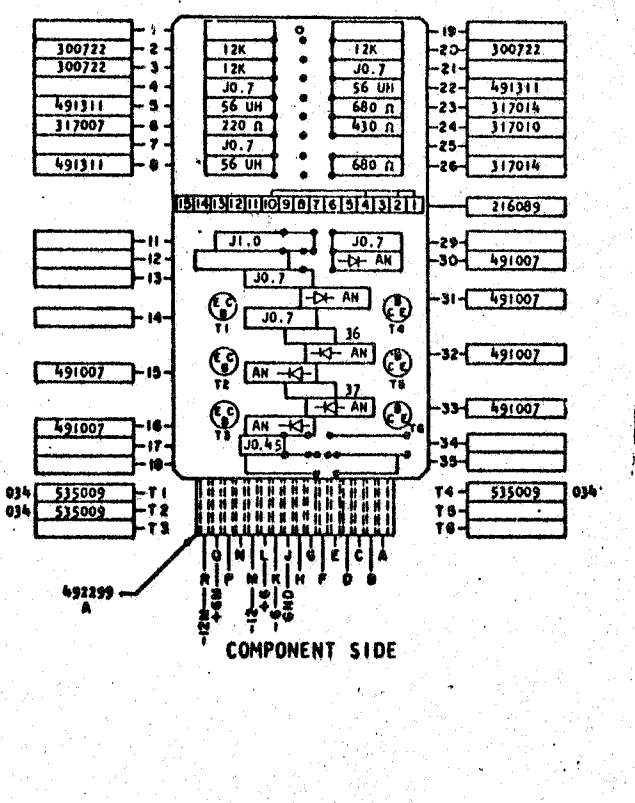
PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,C	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
H	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
P	P	OUTPUT		UP	-4.93	-3.54
				DOWN	-8.82	-12.48
F,D, G,E	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
A,H	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL HIGH SPEED-TWO WAY "AND"PNP ALL LDS					6-29-62	EC 115599					729871
DESIGN			MODEL	SMS		30-4-63	7783687					
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

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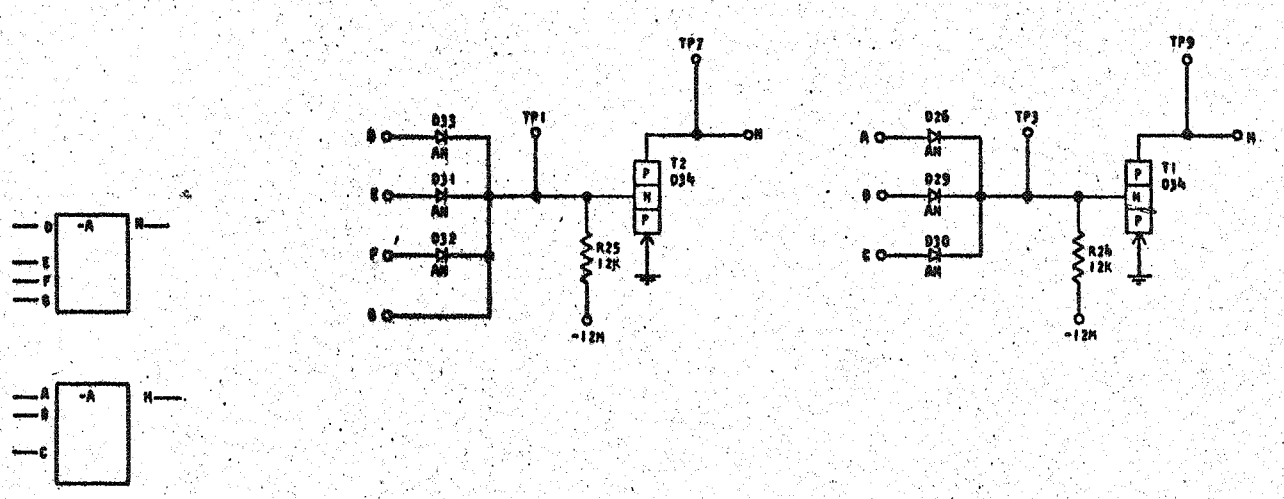
CARD CODE 729872

JH --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371586

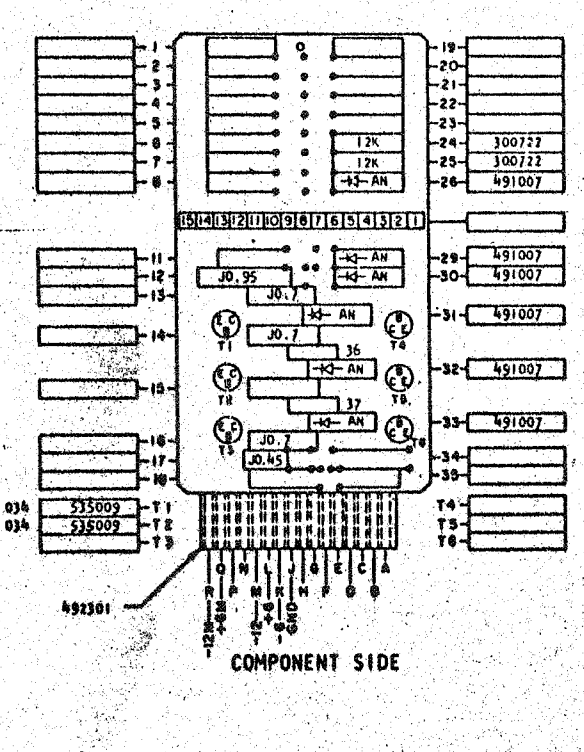
CTDL HIGH SPEED 3-WAY "AND" NO LOADS



SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, TRANSISTOR ON, THE OUTPUT IS UP
3. INPUTS ON EXTENDER INPUTS MUST BE DOWN IN COINCIDENCE WITH INPUTS ON CARD FOR UP OUTPUT
4. BOTH OUTPUTS MUST BE COLLECTOR LOADED
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D,E, F	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
N	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
				UP		
				DOWN		
A,B, C	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
N	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
G		EXTENDER INPUT		UP	+6	
				DOWN	0.0	



DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "ON".

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL HIGH SPEED 3-WAY "AND" PNP NO LOADS					2-19-62	RC115599					
DESIGN				MODEL	SMS	30.4.63	TT83697					
DRAWN	RG	8-1-62		SCALE	NONE							
CHECK	WR	8-1-62		DRAW	LIC	9-12-62						
APPRD				CHECK								

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CARD CODE 729873

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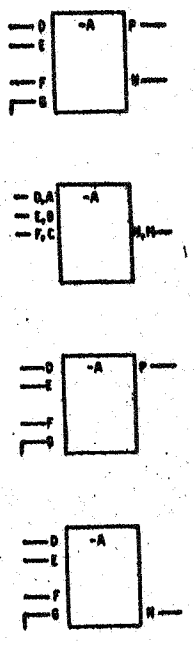
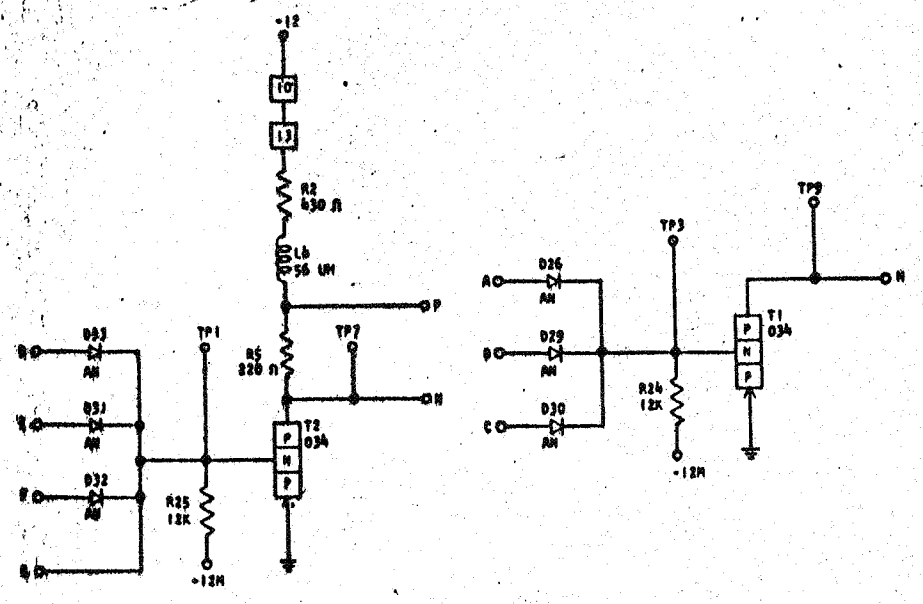
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371585

CTDL HIGH SPEED THREE WAY "AND" PNP ONE LOAD

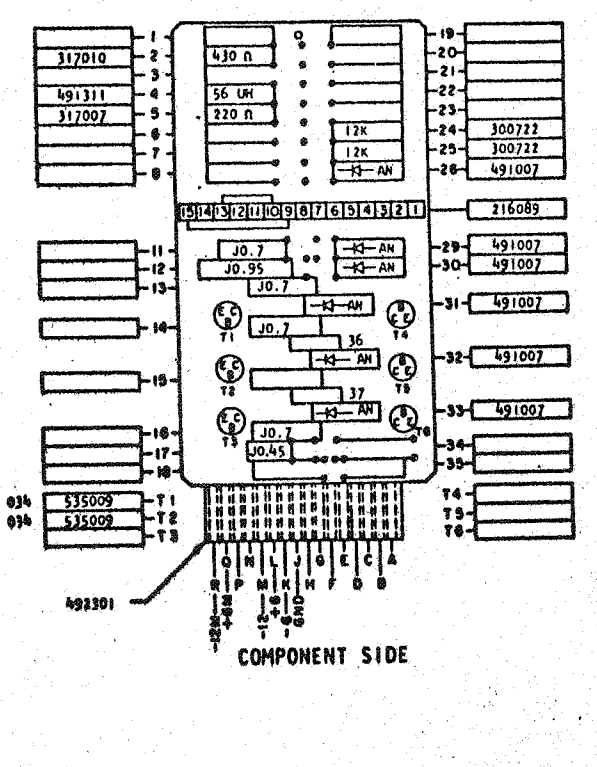




SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, TRANSISTOR ON, THE OUTPUT IS UP
3. INPUTS ON EXTENDER CARD MUST BE DOWN IN COINCIDENCE WITH INPUTS ON CARD FOR UP OUTPUT
4. T1 MUST BE COLLECTOR LOADED
5. PIN P IS CURRENT MODE OUTPUT
6. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D,E, F	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
N	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
P	U	OUTPUT		UP	-4.93	-3.54
				DOWN	-8.82	-12.48
A,B, C	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
N	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
G		EXTENDER INPUT		UP	+6	
				DOWN	0.0	



DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL HIGH SPEED THREE WAY "AND" PNP ONE LD				6-25-62	EC 115599					
					10-4-62	TT 83689					
DESIGN			MODEL	SMS							
DETAIL	BQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	L16 047-62							
APPRO			CHECK								

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CARD CODE 729874

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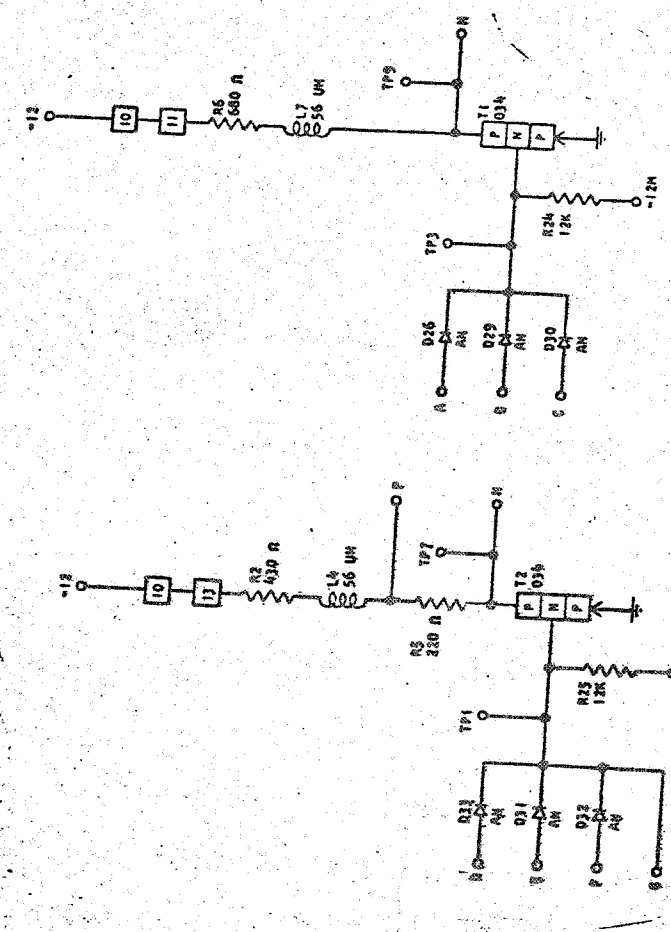
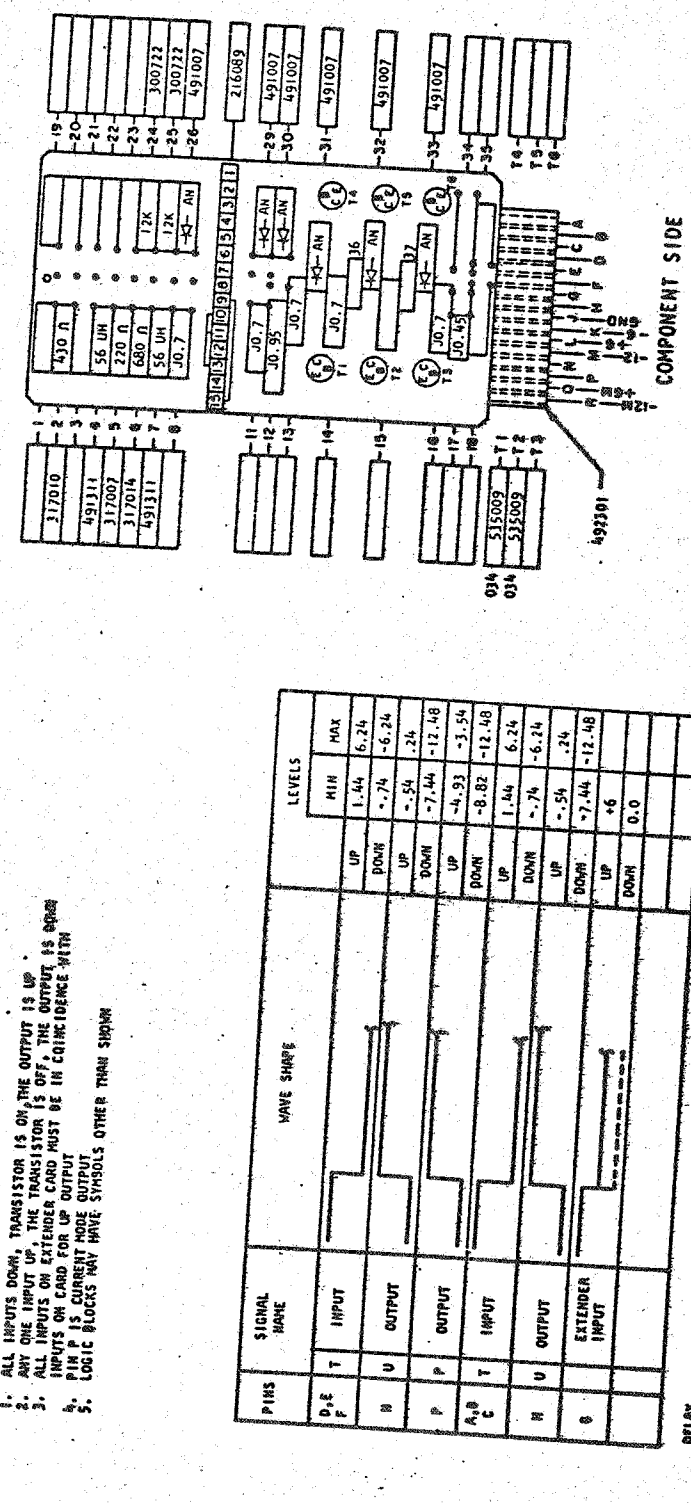
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371584

CTDL HIGH SPEED 3 - WAY "AND" PNP ALL LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN, TRANSISTOR IS ON, THE OUTPUT IS UP.
2. ANY ONE INPUT UP, THE TRANSISTOR IS OFF, THE OUTPUT IS DOWN
3. ALL INPUTS ON EXTENDER CARD MUST BE IN COINCIDENCE WITH INPUTS ON CARD FOR OUTPUT
4. PIN P IS CURRENT MODE OUTPUT
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS MIN	LEVELS MAX
D,E,F	INPUT	UP	1.44	6.24
		DOWN	-.74	-6.24
H	OUTPUT	UP	-.54	.24
		DOWN	-7.44	-12.48
P	OUTPUT	UP	-4.93	-3.54
		DOWN	-8.82	-12.48
A,B,C	INPUT	UP	1.44	6.24
		DOWN	-.74	-6.24
M	OUTPUT	UP	-.54	.24
		DOWN	-7.44	-12.48
G	EXTENDER INPUT	UP	+6	
		DOWN	0.0	

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

CHECKED AND PACKAGING STANDARDS APPROVAL	DATE	729874
ABC	4-2-62	DEVELOPMENT NO.

CHANGE NO.	APPROVAL	DATE
EC 115599		
837683687		

INTERNATIONAL BUSINESS MACHINES CORP. DATE 4-2-62

DRAWN RG 3-1-62 (SCALE) NONE

DESIGN WF 3-1-62 (DRAW) L16 P-17-66

APPROVED (CHECK)

CARD ASM TSTR-CTDL HIGH SPEED 3-WAY "AND" PNP ALL LOADS 30.4.63 837683687

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CARD CODE 729875

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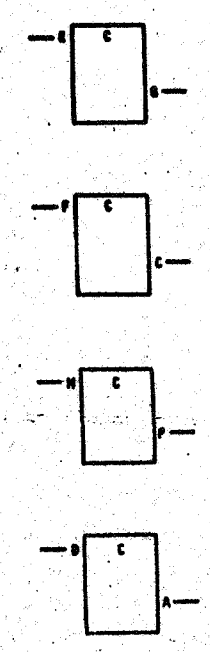
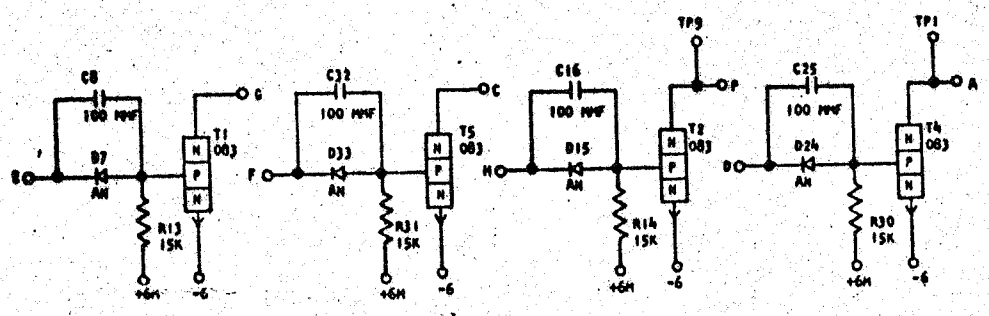
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371590

CTDL HIGH SPEED ONE WAY NPN NO LOADS





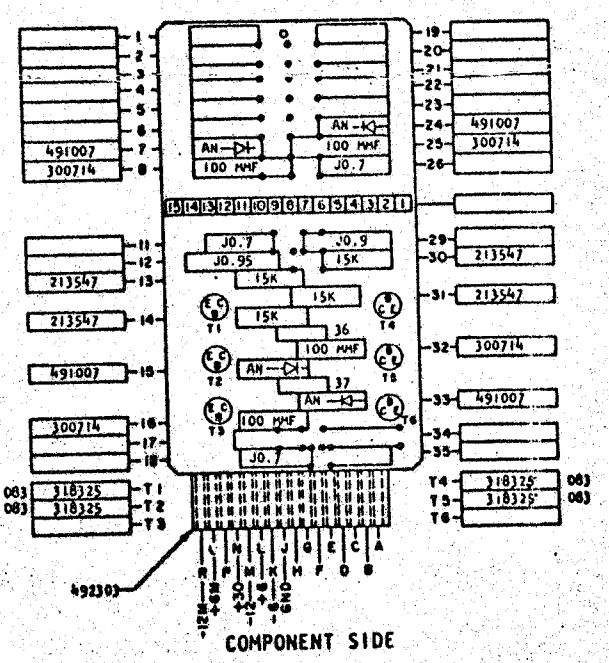
SEQUENCE OF OPERATION

1. IF THE INPUT IS UP, THE TRANSISTOR IS ON, THE OUTPUT IS DOWN
2. IF THE INPUT IS DOWN, THE TRANSISTOR IS OFF, THE OUTPUT IS UP
3. ALL TRANSISTORS MUST BE COLLECTOR LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, H,B	U	INPUTS		UP	-5.26	+.24
				DOWN	-7.44	-12.48
B,C, P,A	T	OUTPUTS		UP	+1.44	+8.24
				DOWN	-5.26	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.20
TURN OFF	0	0.30



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-CTDL HIGH SPEED ONE WAY NPN NO LOADS				4-27-62	ECI 15599						729875
DESIGN			MODEL	SMS	30.4.63	JT 83687						
DETAIL	RC	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRD			CHECK									

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CARD CODE 729876
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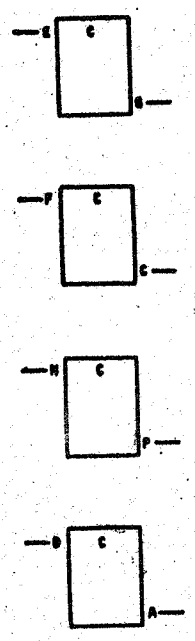
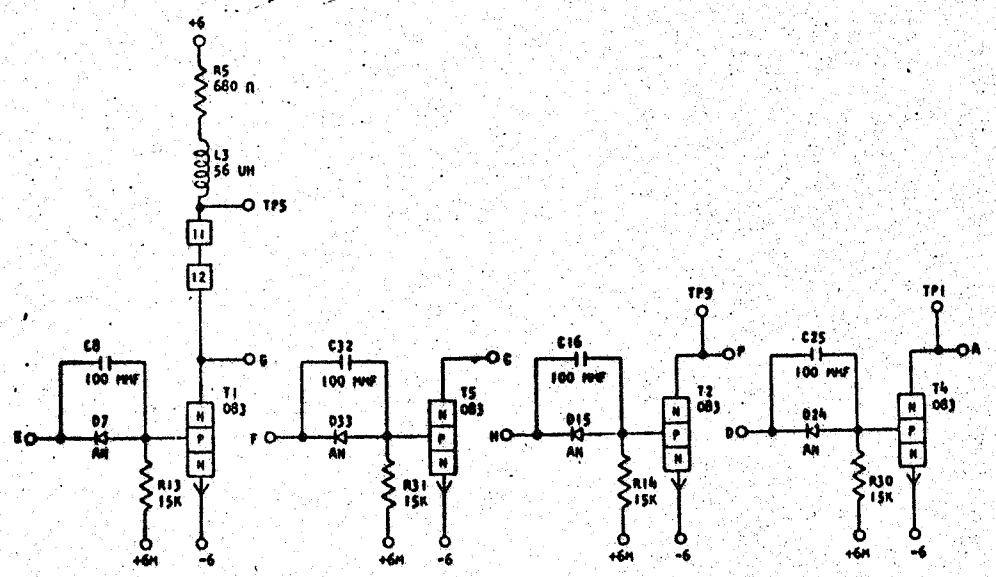
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371589

CTDL HIGH SPEED ONE WAY NPN ONE LOAD





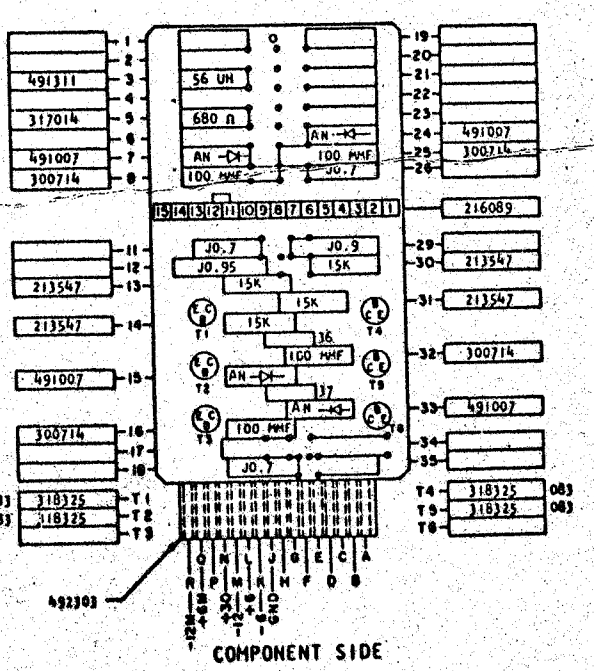
SEQUENCE OF OPERATION

1. IF THE INPUT IS UP, THE TRANSISTOR IS ON, THE OUTPUT IS DOWN
2. IF THE INPUT IS DOWN, THE TRANSISTOR IS OFF, THE OUTPUT IS UP
3. T5, T2, T4 MUST BE COLLECTOR LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, H,B	U	INPUT		UP	-5.26	+.24
				DOWN	-7.44	-12.48
G,C, P,A	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.20
TURN OFF	0	0.30



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INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL HIGH SPEED ONE WAY NPN ONE LOAD				6-27-62	EC 115599					
DESIGN			MODEL	SMS	30.4.63	TT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LTG 3-17-62							
APPRD			CHECK								

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

729876

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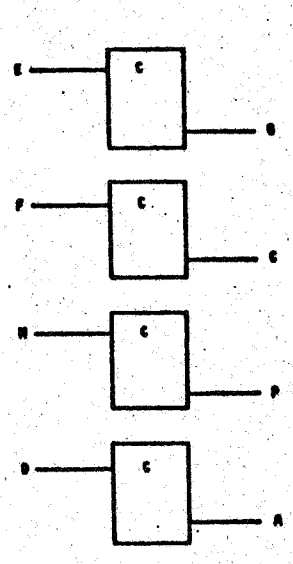
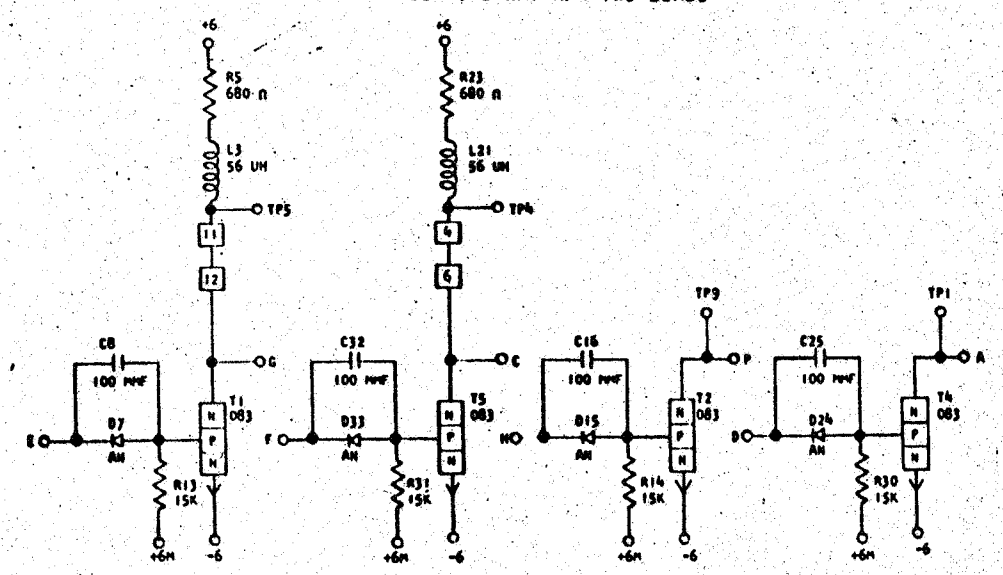
CARD CODE	729877
JJ VN	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371588

CTDL HIGH SPEED ONE WAY NPN TWO LOADS





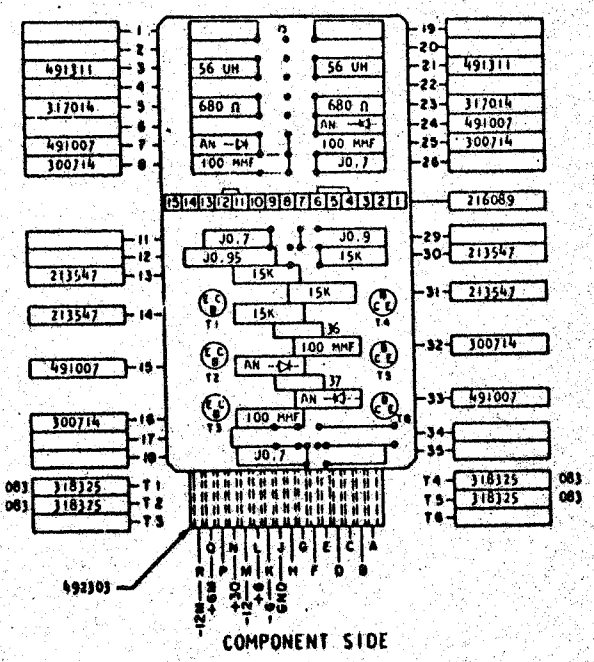
SEQUENCE OF OPERATION

1. IF THE INPUT IS UP, THE TRANSISTOR IS ON, THE OUTPUT IS DOWN
2. IF THE INPUT IS DOWN, THE TRANSISTOR IS OFF, THE OUTPUT IS UP
3. PINS P & A MUST BE TIED TO COLLECTOR LOAD
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E, F, H, D	U	INPUT		UP	-5.26	+.24
				DOWN	-7.44	-12.48
C, G, P, A	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.20
TURN OFF	0	0.30



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL HIGH SPEED ONE WAY NPN TWO LOADS				4-17-62	EC 115599					
					30-4-62	JT83687					
DESIGN			UNLESS	SMS							
DETAIL	RG	3-1-62	SCALE	NONE							
CHECK	VN	3-1-62	DRAW	CTG 3-17-62							
APPRO			CHECK								

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CARD CODE 729878

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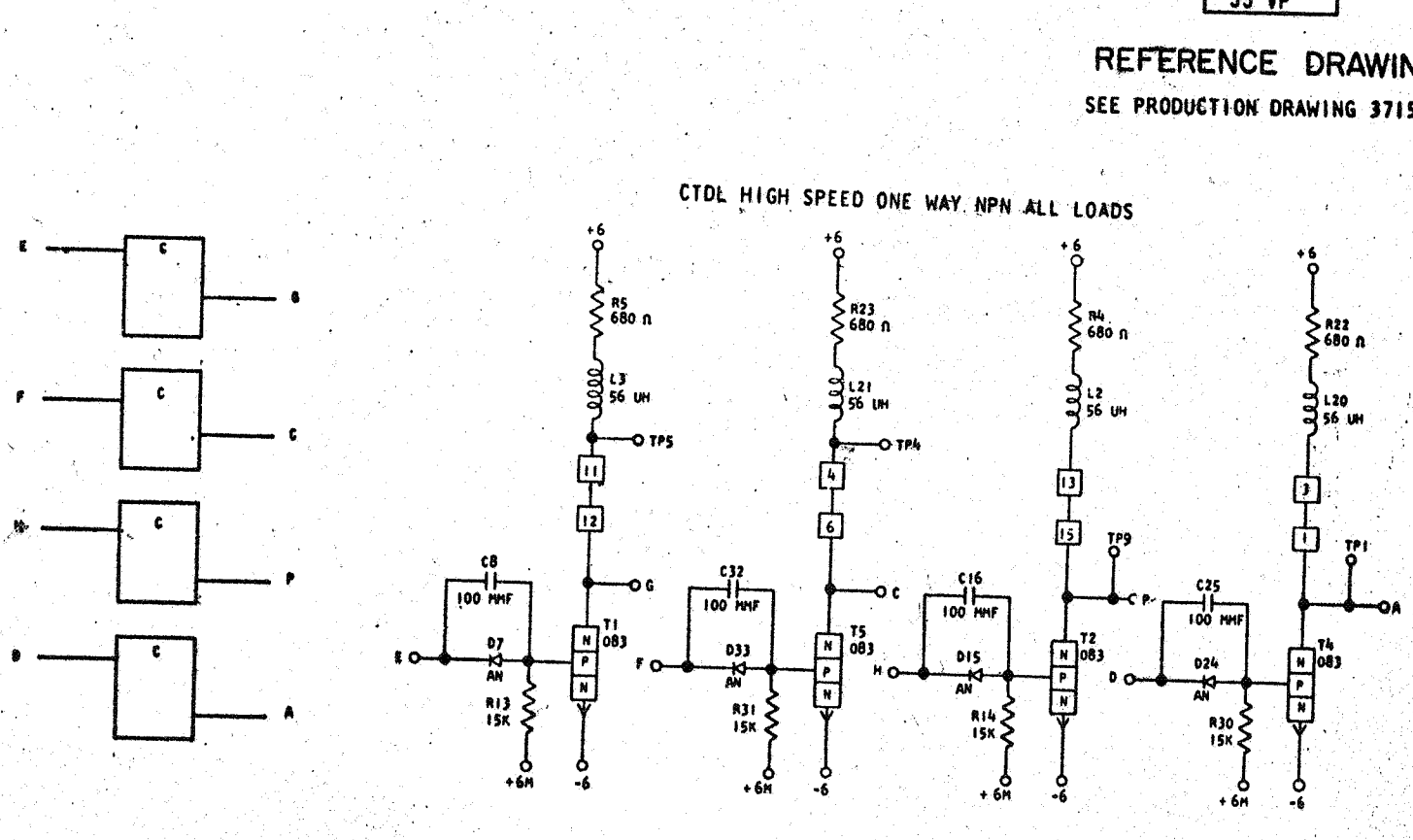
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371587

CTDL HIGH SPEED ONE WAY NPN ALL LOADS



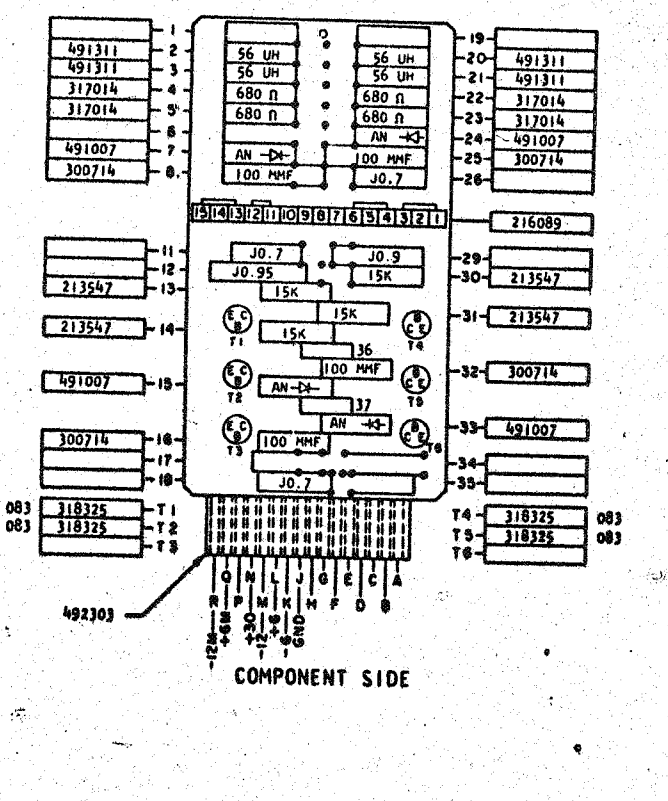
SEQUENCE OF OPERATION:

1. IF THE INPUT IS UP, THE TRANSISTOR IS ON, THE OUTPUT IS DOWN.
2. IF THE INPUT IS DOWN, THE TRANSISTOR IS OFF, THE OUTPUT IS UP.
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, H,D	U	INPUT		UP	-5.26	+.24
				DOWN	-7.44	-12.48
G,C, P,A	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
				UP		
				DOWN		

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.20
TURN OFF	0	0.30



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-CTDL HIGH SPEED ONE WAY NPN ALL LOADS					6-29-62	EC115599					
			MODEL	SMS	30-4-63	JT83687					
DESIGN											
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LTG 3-17-62							
APPRD			CHECK								

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CARD CODE	729879
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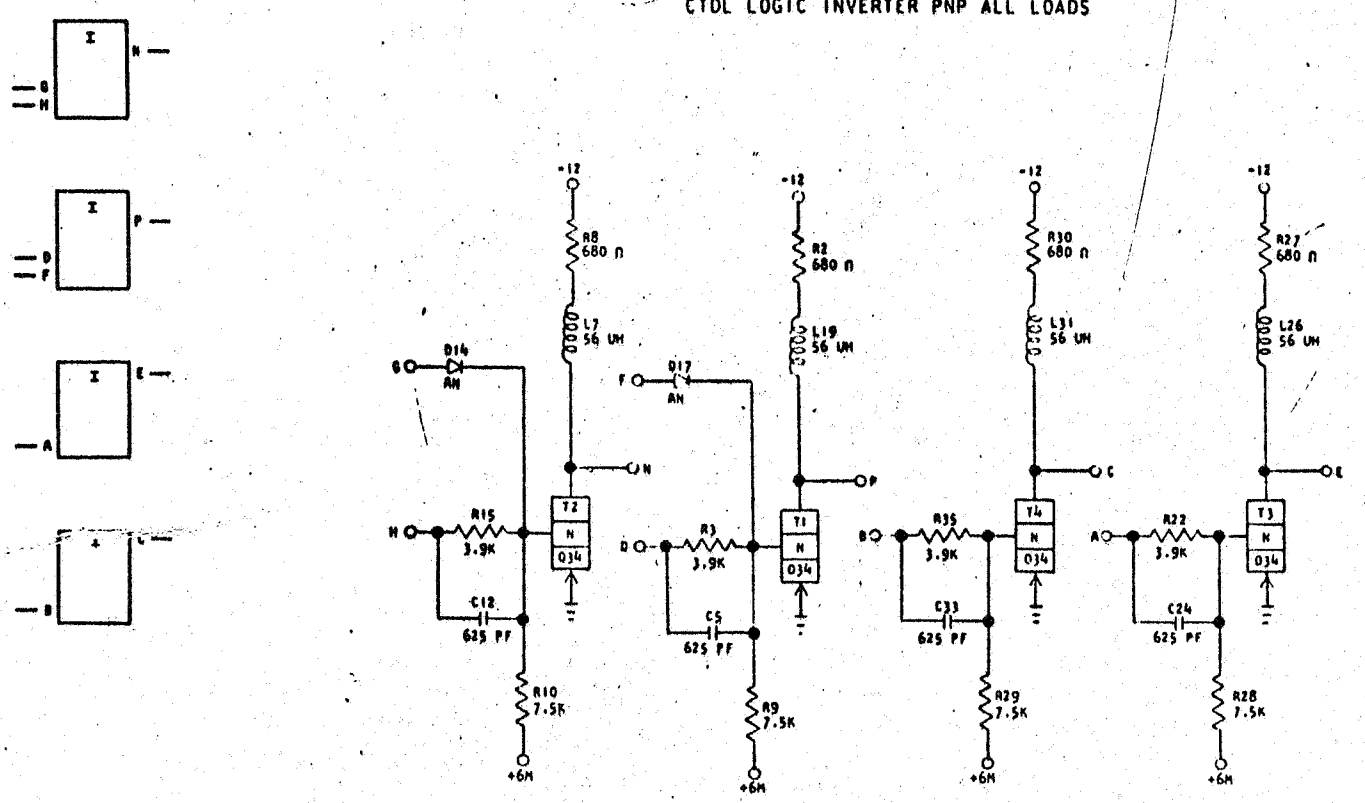
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371077

CTDL LOGIC INVERTER PNP ALL LOADS



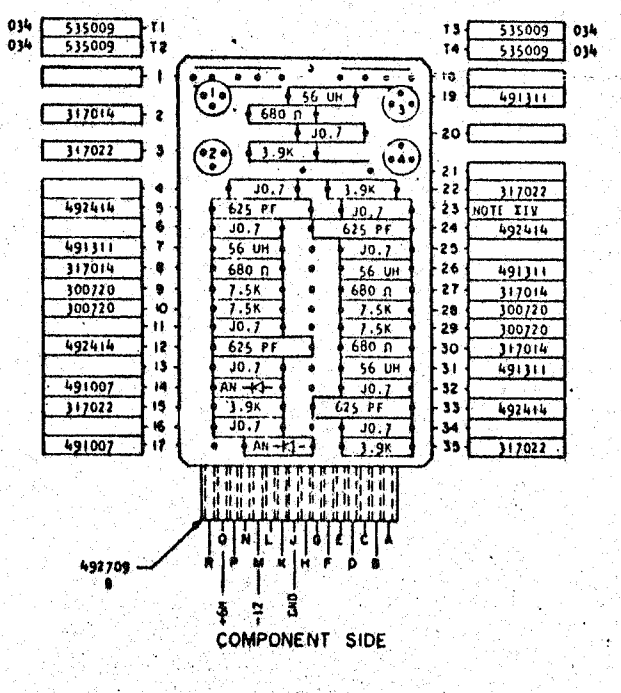
SEQUENCE OF OPERATION

1. FOR AN UP OUTPUT THE INPUT MUST BE DOWN
2. THE GATING DIODE IS PROVIDED ONLY TO RESET A LOGIC INVERTER LATCH. IT SHOULD NOT BE USED AS A SIGNAL INPUT SINCE IT IS POSSIBLE FOR THE SIGNAL INPUT TO OVERRIDE THE GATE
3. IN APPLICATIONS USING BOTH INPUTS ON CIRCUITS 1 AND 2 THE GATE (PINS G OR F) AND SIGNAL INPUTS MUST BE DOWN FOR AN UP OUTPUT
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,D	U	INPUT SIGNAL		UP	-0.54	+0.24
				DOWN	-7.44	-12.48
G,F	T	INPUT GATE		UP	+1.44	+6.24
				DOWN	-0.74	-6.24
H,P	U	OUTPUT		UP	-0.54	+0.24
				DOWN	-7.44	-12.48
A,B, H,D	U	INPUT		UP	0.54	+0.24
				DOWN	-7.44	-12.48
E,C, P,N	U	OUTPUT		UP	-0.54	+0.24
				DOWN	-7.44	-12.48

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	-0.05	-0.15
TURN OFF	+0.05	+0.55



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR - CTDL LOGIC INVERTER PNP ALL LOADS				6-29-62	EC 115599						729879
					30.4.63	TT83687						
DESIGN			MODEL	SMS								
DRAWN	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRD			CHECK									

C

729879

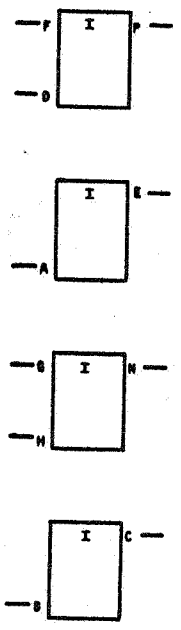
729880 STANDARDS CODE

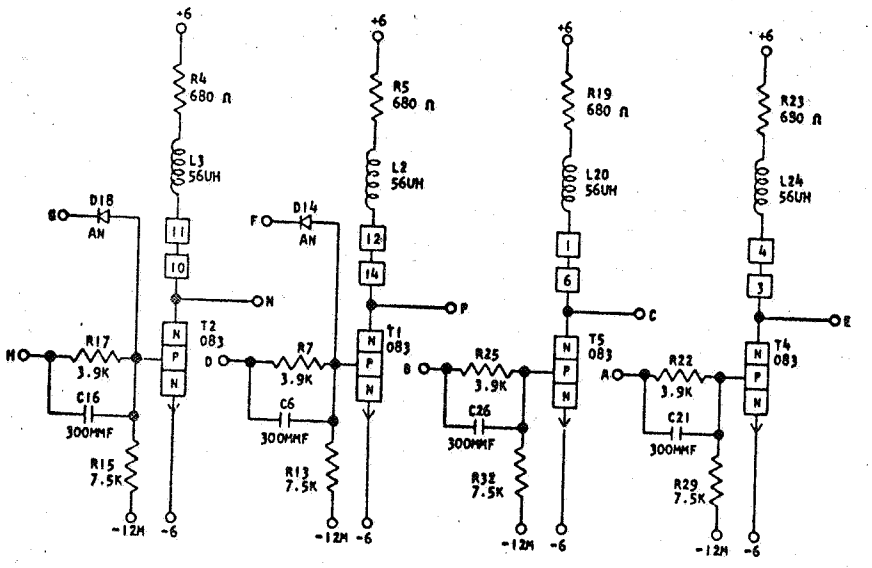
CARD CODE	729880
JM V8	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371079

CTDL LOGIC INVERTER NPN ALL LOADS





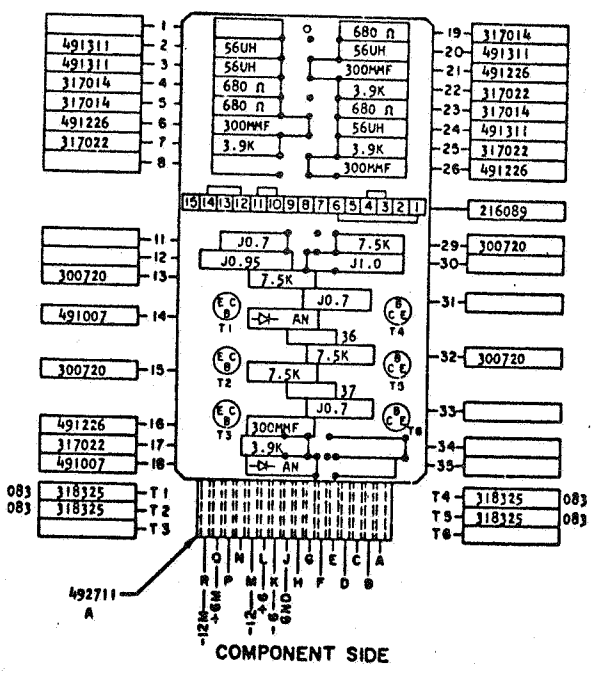
SEQUENCE OF OPERATION

1. GATE AND SIGNAL UP, TRANSISTOR ON, DOWN OUTPUT.
2. GATE OR SIGNAL DOWN, TRANSISTOR OFF, UP OUTPUT.
3. INPUT DOWN, TRANSISTOR OFF, OUTPUT UP.
4. INPUT UP, TRANSISTOR ON, OUTPUT DOWN.
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,D	T	INPUT SIGNAL		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
G,F	U	INPUT GATE		UP	-5.26	+0.24
				DOWN	-7.44	-12.48
N,P	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
B,A	T	INPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
C,E	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	-0.05	0
TURN OFF	-0.05	+0.40



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL LOGIC INVERTER NPN ALL LOADS					4-24-62	EC 115599					729880
DESIGN			MODEL	SMS		30-4-63	JT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

C

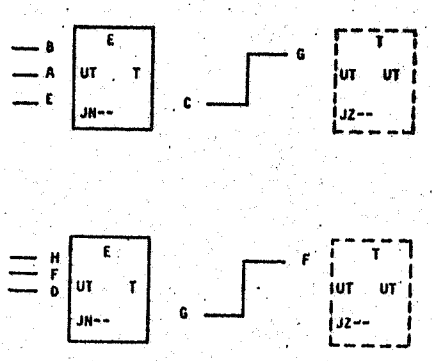
STANDARDS CODE	729881

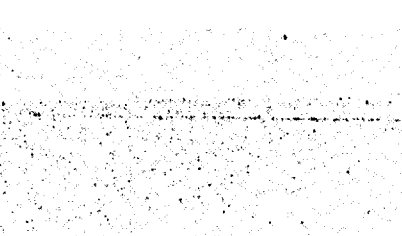
CARD CODE	729881
JN --	

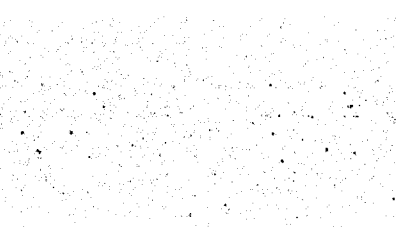
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371081

CTDL - TRIGGER GATE EXTENDER



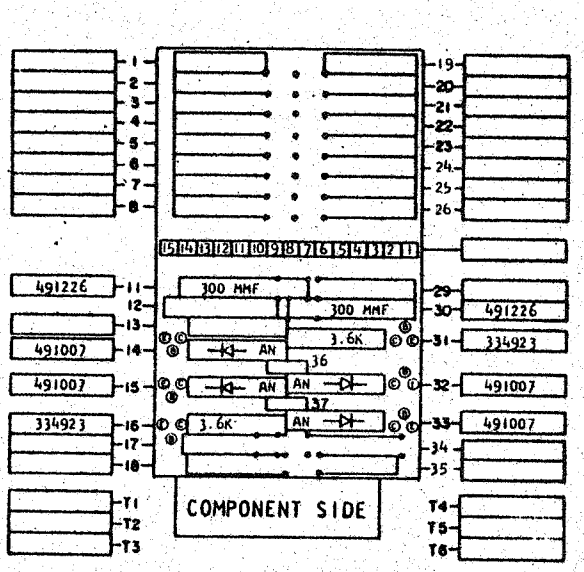




SEQUENCE OF OPERATION

1. AN UP INPUT AT PINS E, D OR AN UP INPUT AT BOTH B, H AND A, F PROVIDES A POSITIVE OUTPUT AT PIN C, G.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B, H	U	GATE INPUT		UP	-5.3	0.2
				DOWN	-7.4	-12.5
A, F	U	AC SET INPUT		UP	-5.3	0.2
				DOWN	-7.4	-12.5
E, D	T	DC SET INPUT		UP	1.44	6.2
				DOWN	-0.74	-6.2
C, G		EXTENDER OUTPUT		UP	1.44	6.2
				DOWN	-0.2	-0.2



INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL - TRIGGER GATE EXTENDER				-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

729881

C

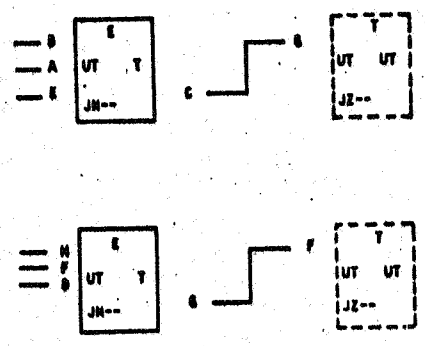
STANDARDS CODE	729881

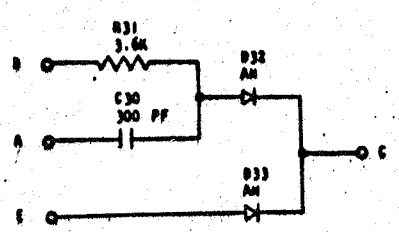
CARD CODE	729881
JN --	

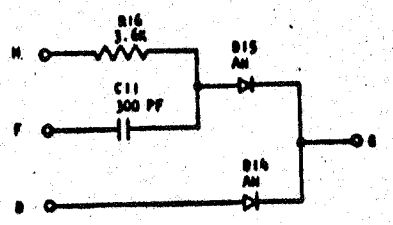
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371081

CTDL - TRIGGER GATE EXTENDER



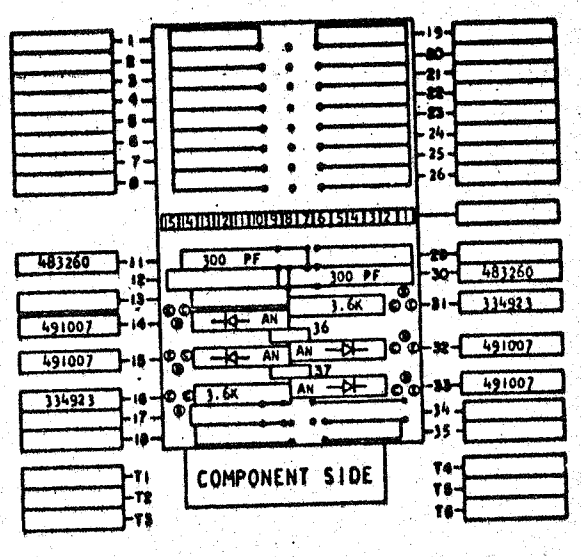




SEQUENCE OF OPERATION

1. AN UP INPUT AT PINS E, D OR AN UP INPUT AT BOTH B, H AND A, F PROVIDES A POSITIVE OUTPUT AT PIN C, G.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B, H	U	GATE INPUT		UP	-5.3	0.2
				DOWN	-7.4	-12.5
A, F	U	AC SET INPUT		UP	-5.3	0.2
				DOWN	-7.4	-12.5
E, D	T	DC SET INPUT		UP	1.44	6.2
				DOWN	-0.74	-6.2
C, G		EXTENDER OUTPUT		UP	1.44	6.2
				DOWN	-0.2	-0.2



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR - CTDL - TRIGGER GATE EXTENDER				
DESIGN			MODEL	SMS	
DETAIL	AQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	L16	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-24-62	115599					729881
1-4-63	EC 116066					
30-4-63	JT 83687					

C

729882

STANDARDS CODE

CARD CODE JZ --

729882

REFERENCE DRAWING

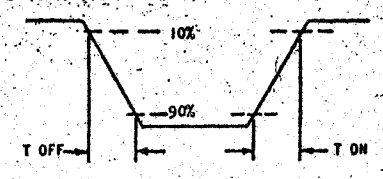
SEE PRODUCTION DRAWING 371082

A,D — T — E,H
B,C
G,F — JZ — N,P

CTDL TRIGGER NO 2

DELAY - USEC

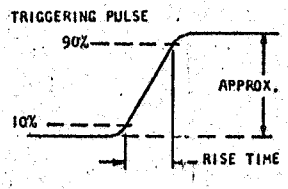
TYPICAL INVERTER AND EF OUTPUT WAVEFORM



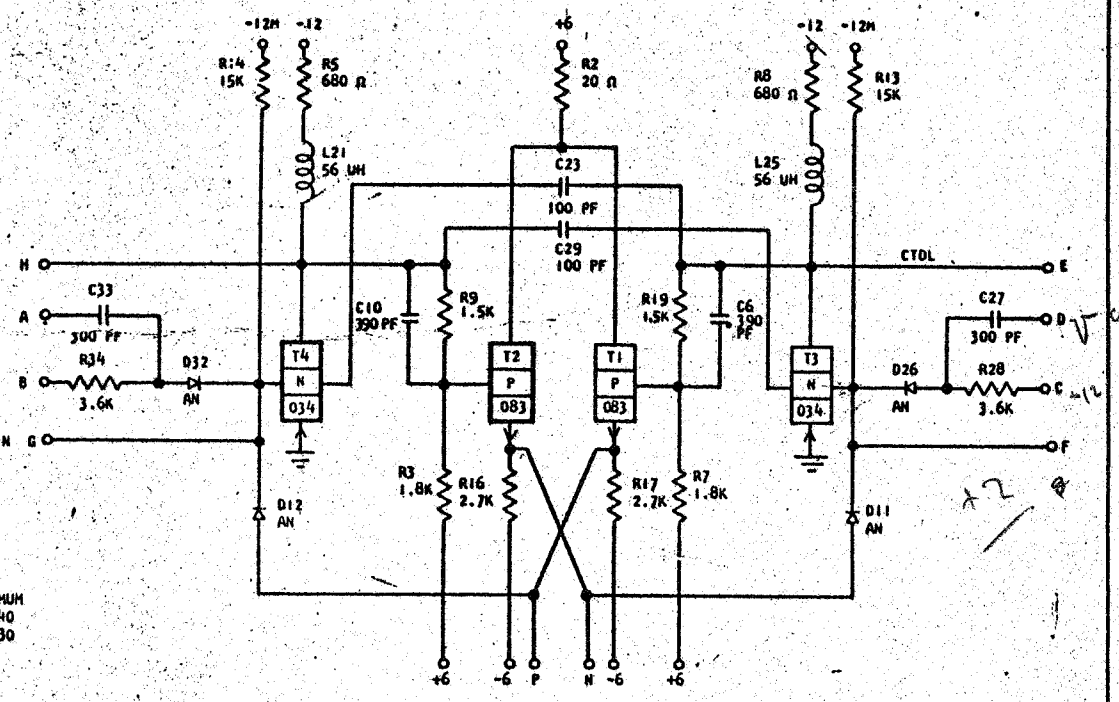
INVERTER DELAY	MINIMUM	MAXIMUM
T OFF	0.15	0.8
T ON	0.10	0.3
EF DELAY	**MINIMUM**	**MAXIMUM**
T OFF	0.05	0.1
T ON	0.10	0.4

THE FOLLOWING DELAY INFORMATION APPLIES WHEN THE AC TRIGGERING INPUT PULSE HAS A RISE TIME OF 0.45 USEC. (SEE FOLLOWING FIGURE)

TRIGGERING PULSE



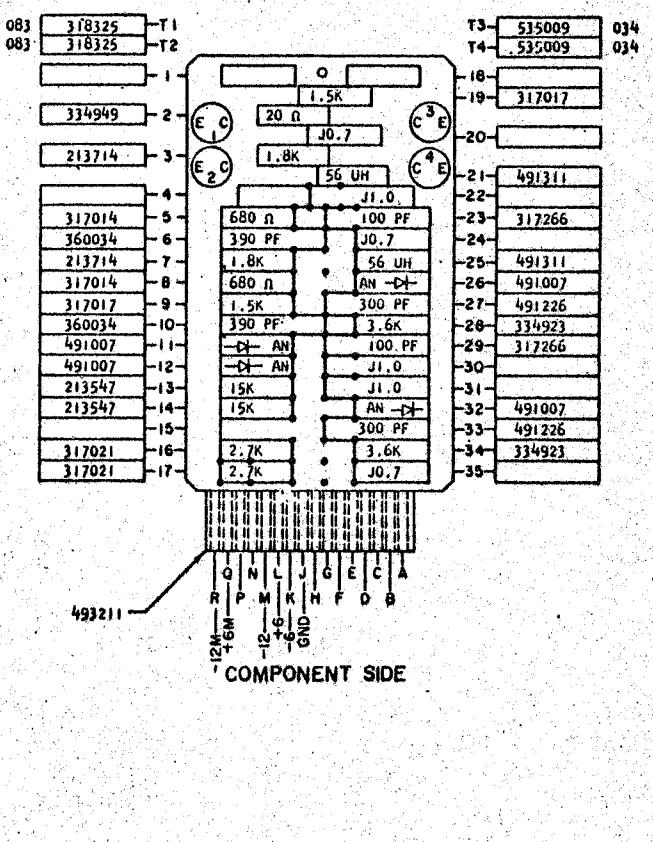
	MINIMUM	MAXIMUM
FROM AC SET TO INVERTER OUTPUTS	0.10	0.40
FROM AC SET TO EF OUTPUTS	0.10	0.30



SEQUENCE OF OPERATION

1. T2 & T4 ON, T1 & T3 OFF
2. PIN B MUST BE CONDITIONED TO AN UP LEVEL 3.75 U SEC BEFORE A POSTIVE SHIFT IS APPLIED TO PIN A TO GIVE AN UP OUTPUT AT PINS E & P AND A DOWN OUTPUT AT PINS H & N. T2 &T4 ARE NOW OFF AND T1 & T3 ON.
3. TO FLIP THE TRIGGER TO ORIGINAL STATE PIN C & D MUST BE CONDITIONED AS WERE PINS A & B ABOVE.
4. COLLECTIVE PULLOVER CAN BE USED ON PINS E & H TO GIVE AN UP OUTPUT.
5. A (JN --) EXTENDER CARD PERMITS ADDITIONAL INPUTS AT PINS G & F TO CONTROL THE TRIGGER.
6. IF SET OR RESET IS ACCOMPLISHED THROUGH PINS G OR F, THE MINIMUM PULSE WIDTH IS 0.5 USEC.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D	T	A.C. SET		UP	-0.5	0.2
				DOWN	-7.4	-12.4
B	U	GATE		UP	-0.5	0.2
				DOWN	-7.4	-12.4
C	U	GATE		UP	-0.5	0.2
				DOWN	-7.4	-12.4
E	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
H	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
N	T	OUTPUT		UP	1.4	3.1
				DOWN	0.7	-5.2
P	T	OUTPUT		UP	1.4	3.1
				DOWN	0.7	-5.2



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTK - CTDL TRIGGER NO 2					2-7-62	115599					
DESIGN				MODEL	SMS							
DETAIL	RG	3-1-62		SCALE	NONE							
CHECK	WH	3-1-62		DRAW	LIG 3-17-62							
APPRO				CHECK								

729882

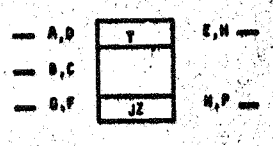
729882

STANDARDS CODE	729882

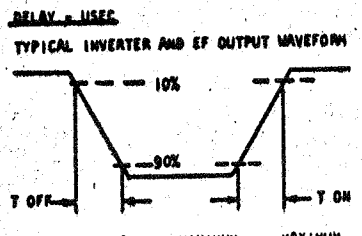
CARD CODE	729882
JZ --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371082

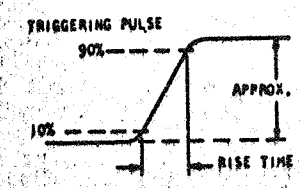


CTDL TRIGGER, NO 2

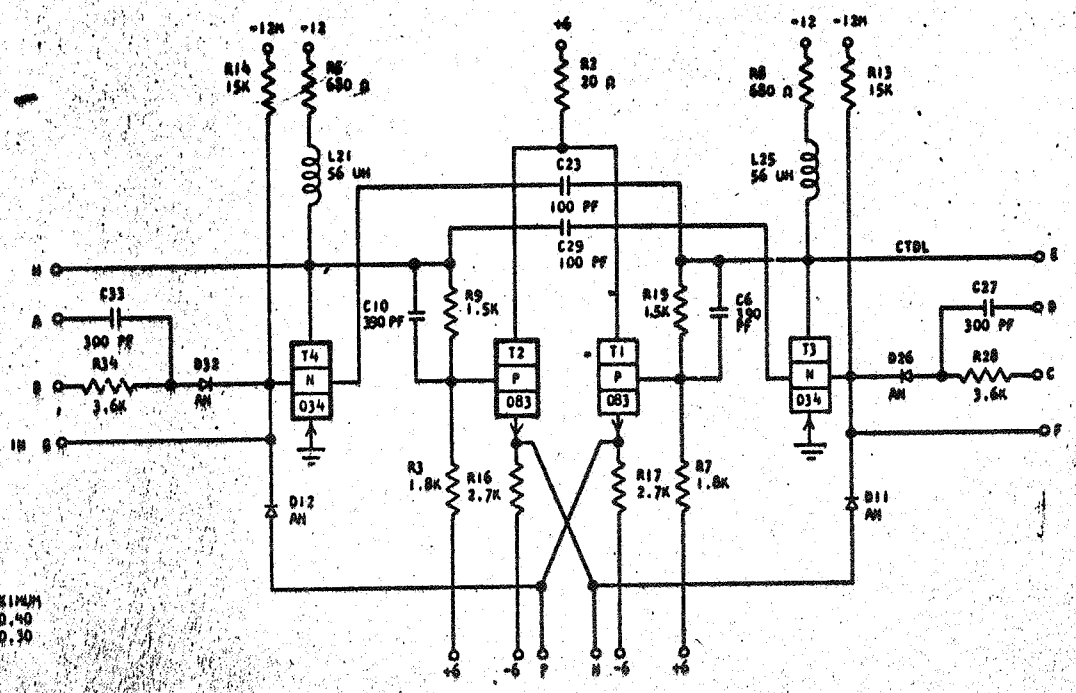


INVERTER DELAY	MINIMUM	MAXIMUM
T OFF	0.15	0.8
T ON	0.10	0.3
EF DELAY	**MINIMUM**	**MAXIMUM**
T OFF	0.05	0.1
T ON	0.10	0.4

THE FOLLOWING DELAY INFORMATION APPLIES WHEN THE AC TRIGGERING INPUT PULSE HAS A RISE TIME OF 0.45 USEC. (SEE FOLLOWING FIGURE)



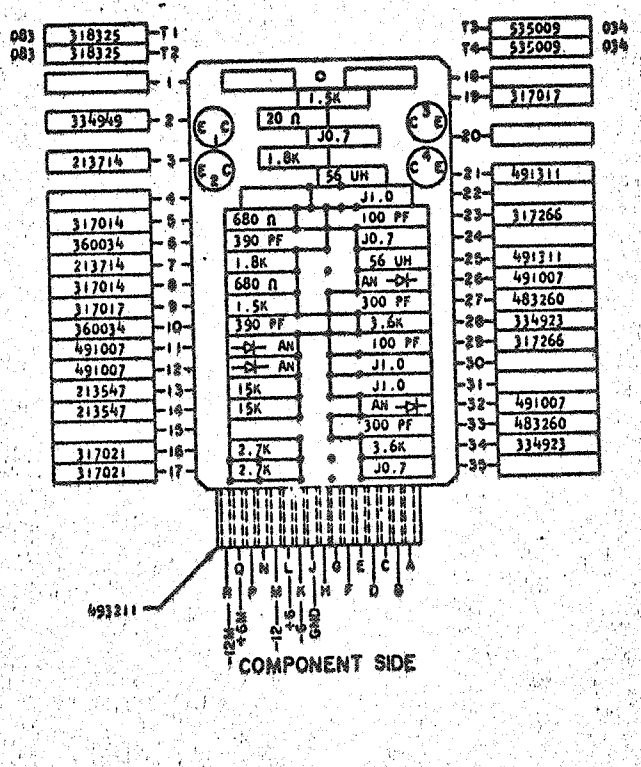
	MINIMUM	MAXIMUM
FROM AC SET TO INVERTER OUTPUTS	0.10	0.40
FROM AC SET TO EF OUTPUTS	0.10	0.30



SEQUENCE OF OPERATION

1. T2 & T4 ON, T1 & T3 OFF
2. PIN B MUST BE CONDITIONED TO AN UP LEVEL 3.75 μ SEC BEFORE A POSTIVE SHIFT IS APPLIED TO PIN A TO GIVE AN UP OUTPUT AT PINS E & P AND A DOWN OUTPUT AT PINS H & N. T2 &T4 ARE NOW OFF AND T1 & T3 ON.
3. TO FLIP THE TRIGGER TO ORIGINAL STATE PIN C & B MUST BE CONDITIONED AS WERE PINS A & B ABOVE.
4. COLLECTIVE PULLOVER CAN BE USED ON PINS E & N TO GIVE AN UP OUTPUT.
5. A (JN --) EXTENDER CARD PERMITS ADDITIONAL INPUTS AT PINS B & F TO CONTROL THE TRIGGER.
6. IF SET OR RESET IS ACCOMPLISHED THROUGH PINS G OR F, THE MINIMUM PULSE WIDTH IS 0.5 USEC.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,B	T	A.C. SET		UP	-0.5	0.2
				DOWN	-7.4	-12.4
B	U	GATE		UP	-0.5	0.2
				DOWN	-7.4	-12.4
C	U	GATE		UP	-0.5	0.2
				DOWN	-7.4	-12.4
E	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
H	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
N	T	OUTPUT		UP	1.4	3.1
				DOWN	0.7	-5.2
P	T	OUTPUT		UP	1.4	3.1
				DOWN	0.7	-5.2



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL TRIGGER NO 2				6-29-62	115599					729882
DESIGN			MODEL	SMS	1-4-63	EC 116066					
DETAIL	RO	3-1-62	SCALE	NONE	30-4-63	JT 83687					
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

729883 | STANDARDS CODE

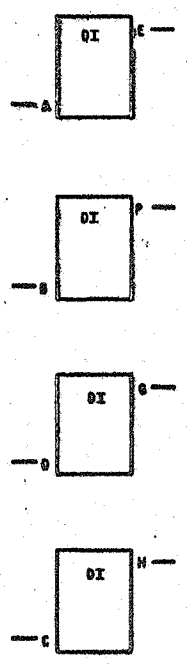
CARD CODE: KA --

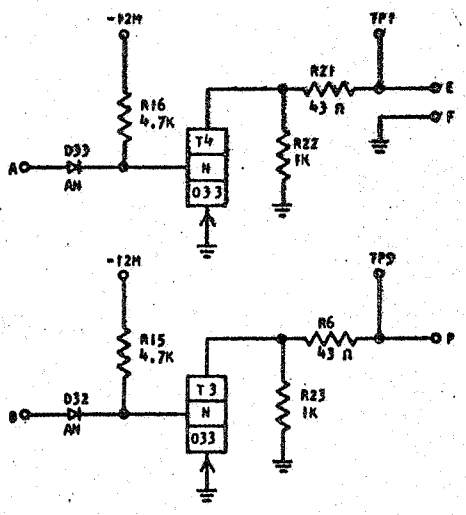
729883

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371546

ALLOY - INDICATOR DRIVER 40 MA

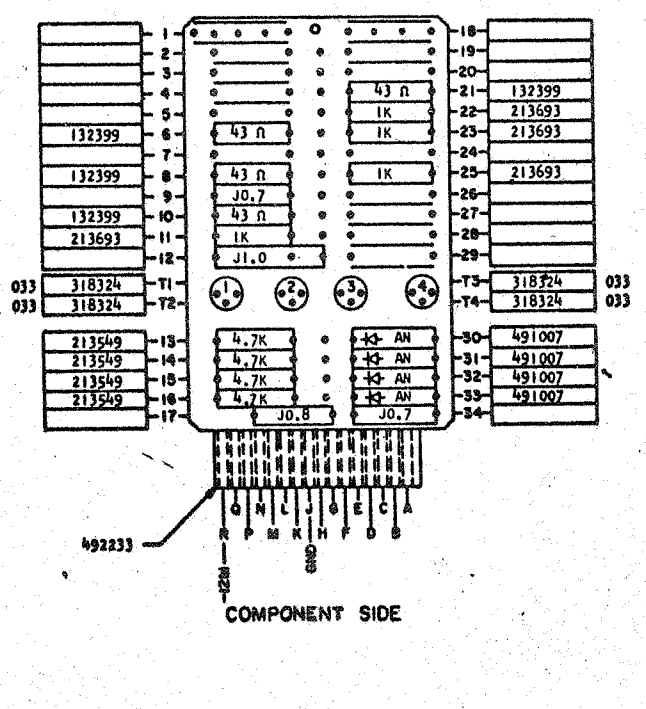




SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
A,D, B,C	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
E,G, P,H	U	OUTPUT		UP	-0.54	0.24
				DOWN		-10



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729883
NAME	CARD ASM TSTR- ALLOY- INDICATOR DRIVER (40 MA)					6-17-62	EC 115599						
DESIGN				MODEL	SMS	30.4.63	TT 83687						
DETAIL	RQ	3-1-62		SCALE	NONE								
CHECK	WH	3-1-62		DRAW	LIG	3-17-62							
APPRO				CHECK									

C

729883

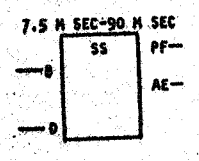
STANDARDS CODE	729884

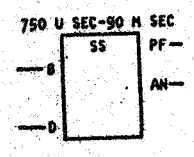
CARD CODE	729884
NB --	

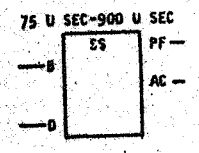
REFERENCE DRAWING

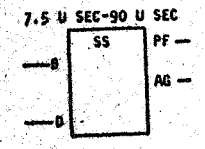
SEE PRODUCTION DRAWING 371591

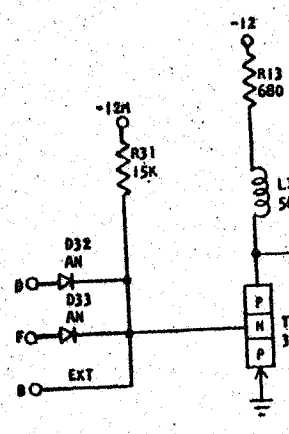
CTDL SINGLE SHOT "T" INPUT

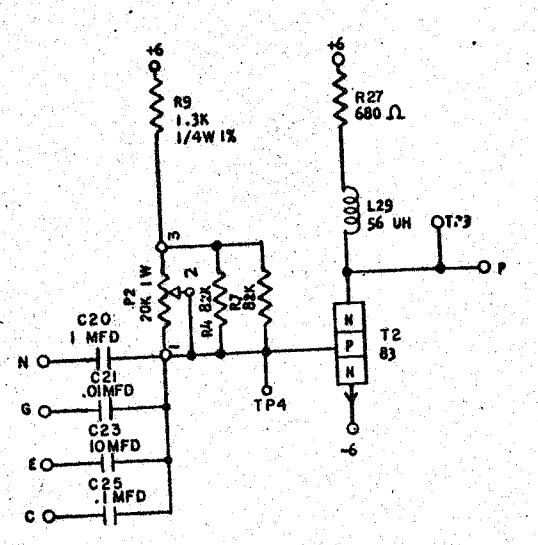








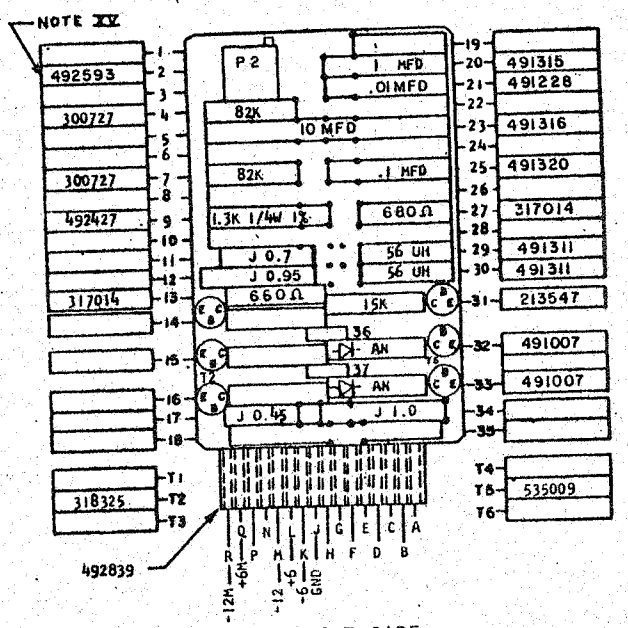




SEQUENCE OF OPERATION

1. T2, T3 ON; P TIED TO F FOR LATCH BACK AND A TO EITHER N,G, E OR C
2. POSITIVE GOING INPUT TO D, T2, T5 OFF
3. R.C. NETWORK DETERMINES LENGTH OF TIME T2 OFF
4. UP INPUT ON EXTENDER CARD WILL GIVE SAME SEQUENCE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D	T	INPUT		UP	1.4	6.2
				DOWN	-0.7	-6.2
B		EXTENDER INPUT		UP	-6	
				DOWN	-12	
F	T	INPUT		UP	1.4	6.2
				DOWN	-0.7	-6.2
P	T	OUTPUT		UP	1.4	6.2
				DOWN	-5.46	-6.2
A	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5
T2 BASE		SWITCH LEVEL		-5.8		
				-6		



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR - CTDL SINGLE SHOT "T" INPUT					6-22-62	115599					729884
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

C

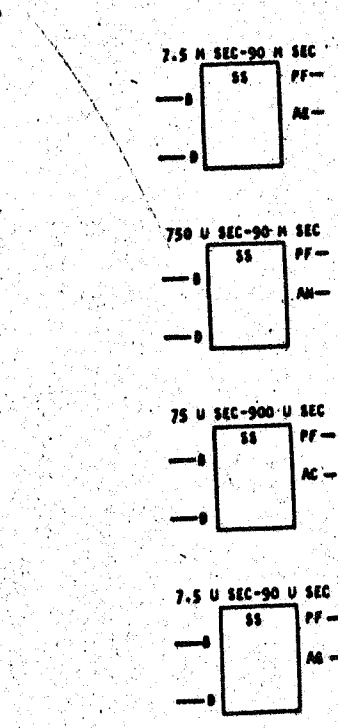
CARD CODE	729884
NB --	

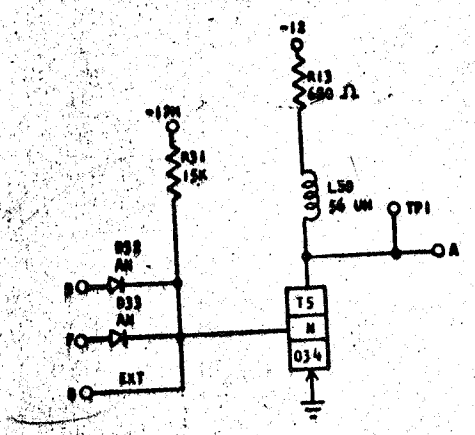
729884

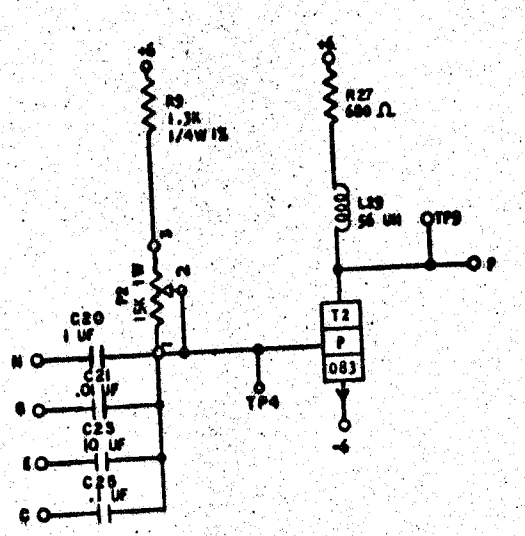
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371591

CTDL SINGLE SHOT "T" INPUT



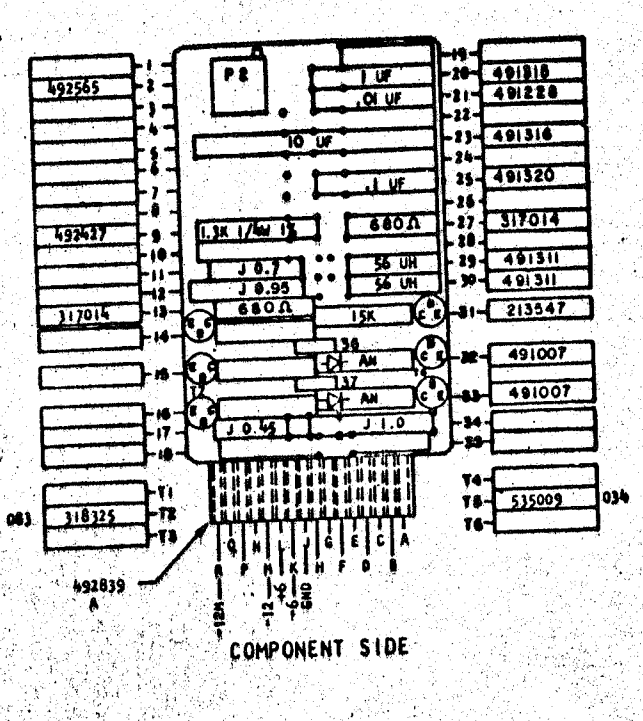




SEQUENCE OF OPERATION

1. T3, T2 ON; P TIED TO F FOR LATCH BACK AND A TO EITHER N,G, E OR C
2. POSITIVE GOING INPUT TO D, T2, T5 OFF
3. R.C. NETWORK DETERMINES LENGTH OF TIME T2 OFF
4. UP INPUT ON EXTENDER CARD WILL GIVE SAME SEQUENCE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D	T	INPUT		UP	1.4	6.2
				DOWN	-0.7	-6.2
D		EXTENDER INPUT		UP	-6	
				DOWN	-12	
F	T	INPUT		UP	1.4	6.2
				DOWN	-0.7	-6.2
P	T	OUTPUT		UP	1.4	6.2
				DOWN	-5.46	-6.2
A	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5
T2 BASE		SWITCH LEVEL →		-6	-5.8	



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729884
NAME	CARD ASSEMBLY TSTR - CTDL SINGLE SHOT "T" INPUT				6-29-62	115599						
					1-11-63	EC 416038						
DESIGN			MODEL	SMS	5a.4.63	JT 83687						
DRAFT	RQ	3-1-62	SCALE	NONE								
CHECK	WM	3-1-62	DRAW.	LIG 3-17-62								
APPRO			CHECK									

C

SHEET 20 OF 20 EC. 113594

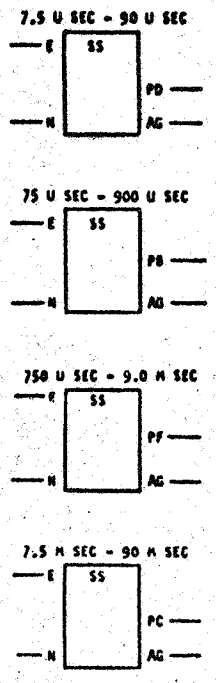
729885 STANDARD CODE

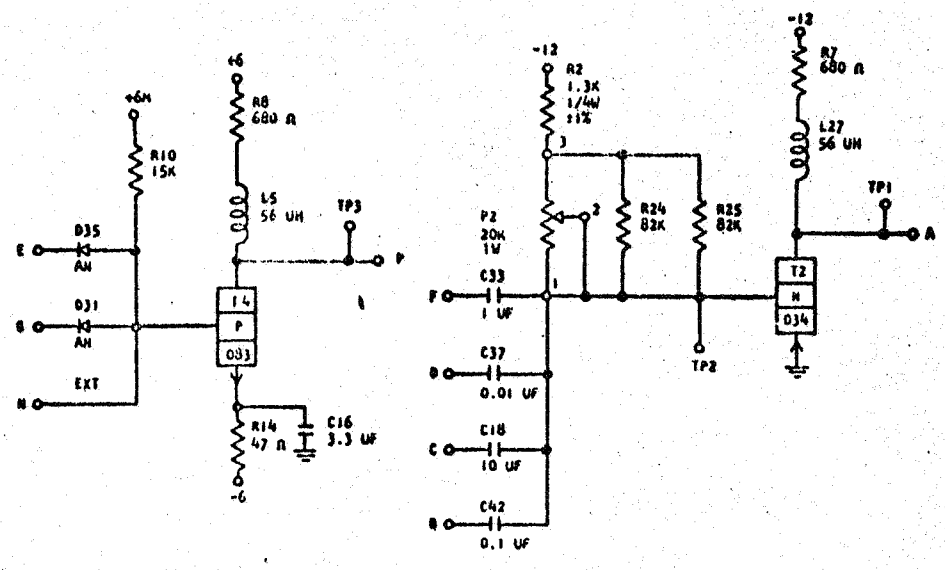
NC-- 729885

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371592

CTDL SINGLE SHOT "U" INPUT

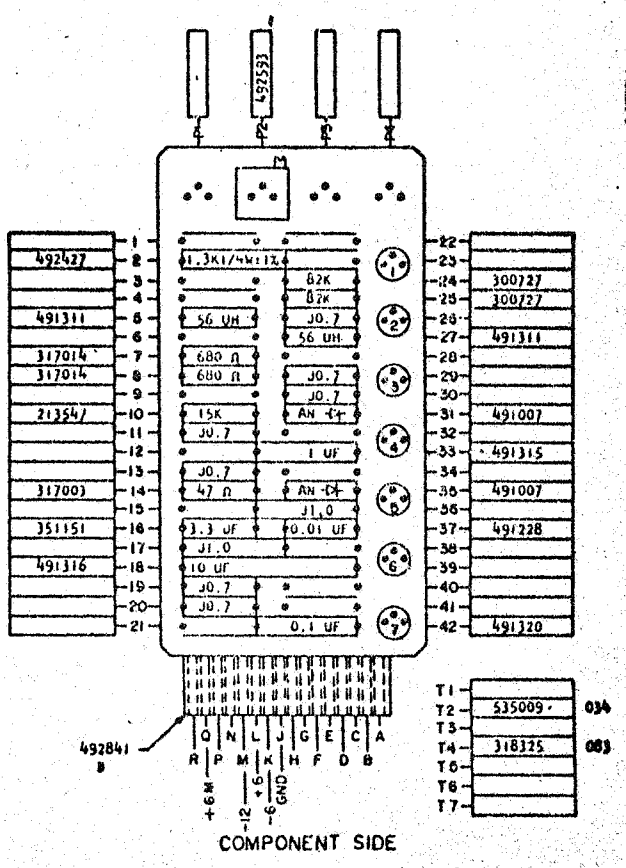




SEQUENCE OF OPERATION

1. T2, T5 ON; A TIED TO G FOR LATCH BACK AND P TO EITHER D, B, F OR C
2. MINUS GOING INPUT TO E, T2, T5 OFF
3. R.C. NETWORK DETERMINES LENGTH OF TIME T5 OFF
4. DOWN INPUT ON EXTENDER CARD WILL GIVE SAME SEQUENCE

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
E	U	INPUT		UP	-0.5	0.2
				DOWN	-7.4	-12.5
N		EXTENDER INPUT		UP	-6	
				DOWN	-12	
G	U	INPUT		UP	-0.5	0.2
				DOWN	-7.4	-12.5
A	U	OUTPUT		UP	-0.5	0.2
				DOWN	-7.44	-12.5
P	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
TS BASE		SWITCH LEVEL				



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TEST-- CTDL SINGLE SHOT "U" INPUT				6-29-62	115599					729885
DESIGN			MODEL	SMS	9-5-62	113594					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW CHECK	JAB	3-21-62						
APPRD											

C

729885 | STANDARDS CODE

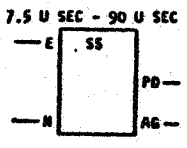
CARD CODE 729885
NC --

REFERENCE DRAWING

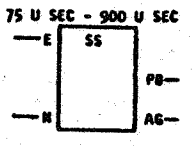
SEE PRODUCTION DRAWING 371592

CTDL SINGLE SHOT "U" INPUT

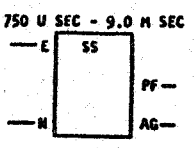
7.5 U SEC - 90 U SEC



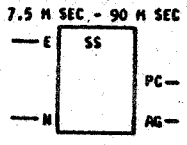
75 U SEC - 900 U SEC

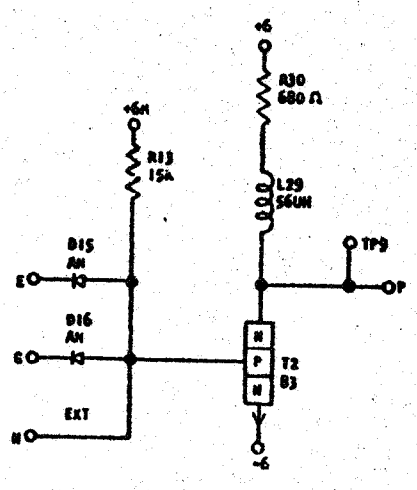


750 U SEC - 9.0 M SEC



7.5 M SEC - 90 M SEC

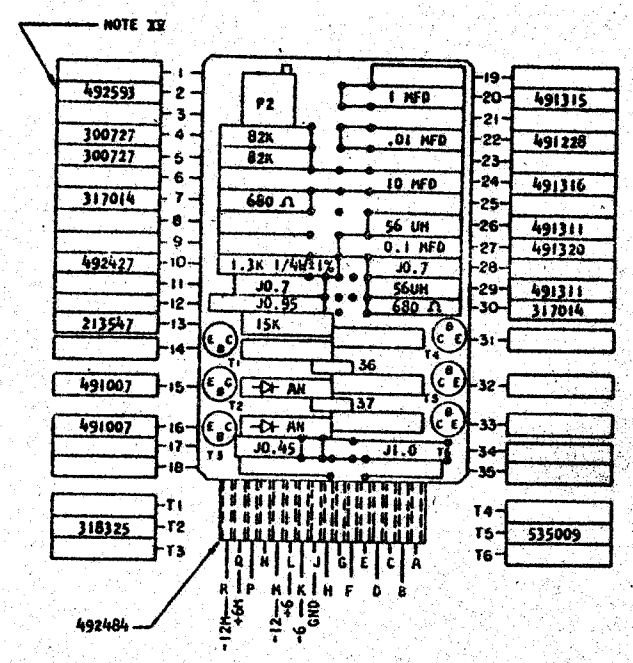




SEQUENCE OF OPERATION

1. T2, T5 ON; A TIED TO G FOR LATCH BACK AND P TO EITHER D, B, F OR C
2. MINUS GOING INPUT TO E, T2, T5 OFF
3. R.C. NETWORK DETERMINES LENGTH OF TIME T5 OFF
4. DOWN INPUT ON EXTENDER CARD WILL GIVE SAME SEQUENCE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E	U	INPUT		UP	-0.5	0.2
				DOWN	-7.4	-12.5
N		EXTENDER INPUT		UP	-6	
				DOWN	-12	
G	U	INPUT		UP	-0.5	0.2
				DOWN	-7.4	-12.5
A	U	OUTPUT		UP	-0.5	0.2
				DOWN	-7.44	-12.5
P	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
T5 BASE		SWITCH LEVEL →				



CONPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR - CTDL SINGLE SHOT "U" INPUT				6-27-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRD			CHECK								

729885

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STANDARDS CODE

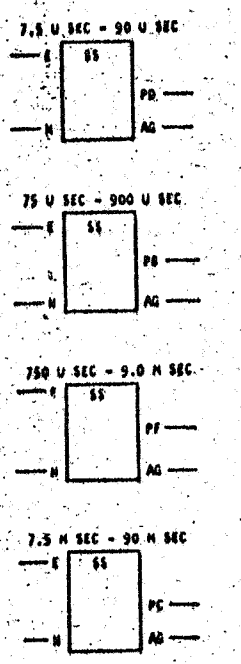
CARD CODE 729885

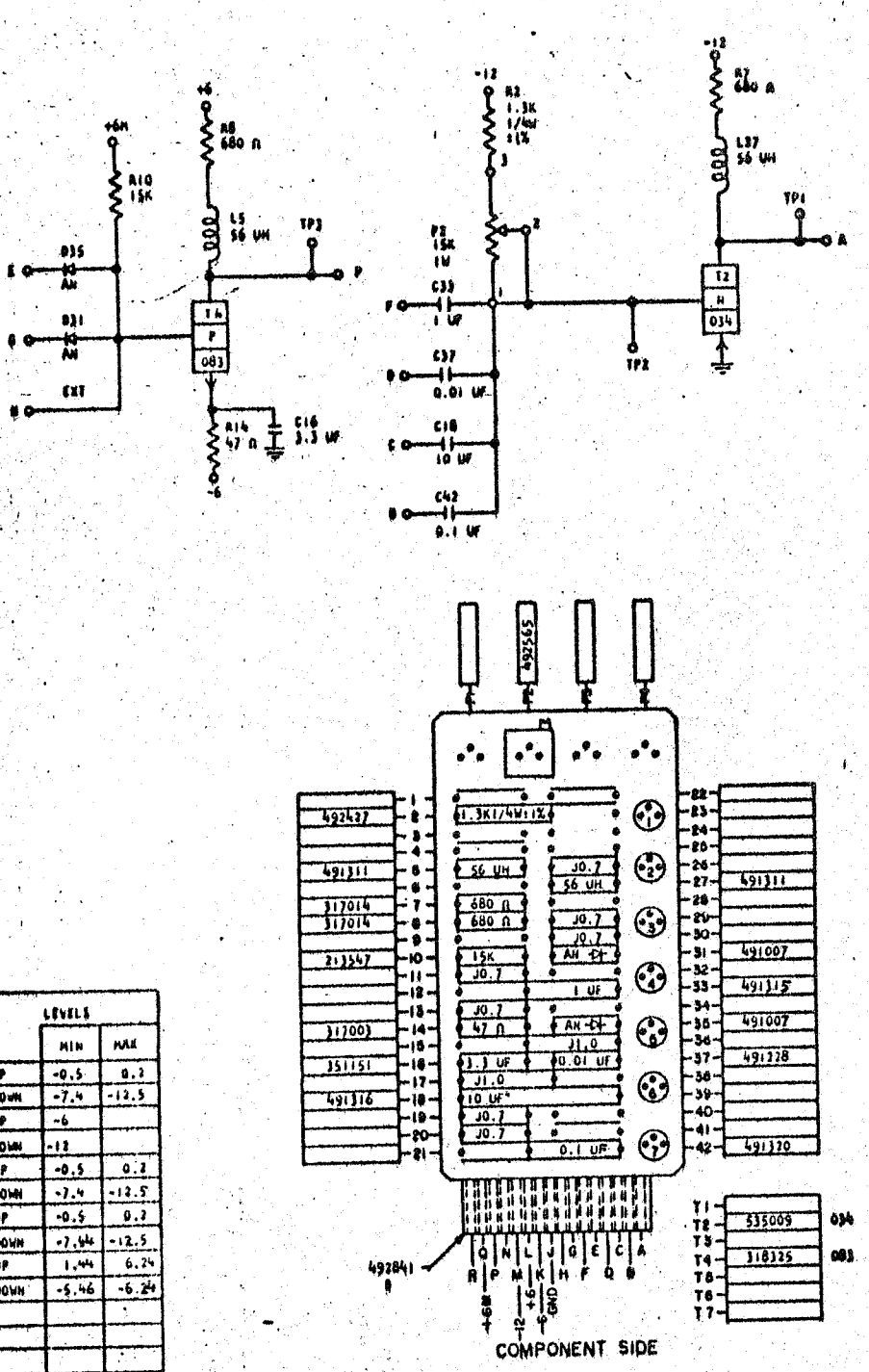
NC--

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371592

CTDL SINGLE SHOT "U" INPUT





SEQUENCE OF OPERATION

1. T2, T5 ON; A TIED TO B FOR LATCH BACK AND P TO EITHER B, B, F OR C
2. MINUS GOING INPUT TO E, T2, T5 OFF
3. R.C. NETWORK DETERMINES LENGTH OF TIME T5 OFF
4. DOWN INPUT ON EXTENDER CARD WILL GIVE SAME SEQUENCE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E	U	INPUT		UP	-0.5	0.2
				DOWN	-7.4	-12.5
N		EXTENDER INPUT		UP	-6	
				DOWN	-12	
B	U	INPUT		UP	-0.5	0.2
				DOWN	-7.4	-12.5
A	U	OUTPUT		UP	-0.5	0.2
				DOWN	-7.44	-12.5
P	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
T5 BASE		SWITCH LEVEL				

CIRCUIT AND PACKAGING STANDARD

APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TST#--- CTDL SINGLE SHOT "U" INPUT					6-29-62	115598					
DESIGN			MODEL	SMS		9-5-62	115594					
DETAIL	PQ	3-1-62	SCALE	NONE		1-11-63	EC 116038					
CHECK	WH	3-1-62	DRAW	JAU	11-21-62	30-4-63	JT 83687					
APPRO			CHECK									

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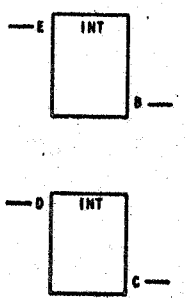
729886 STANDARDS CODE

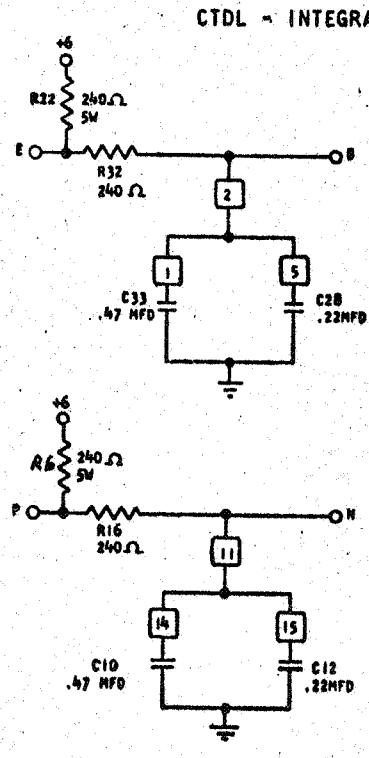
CARD CODE	729886
NG TF	

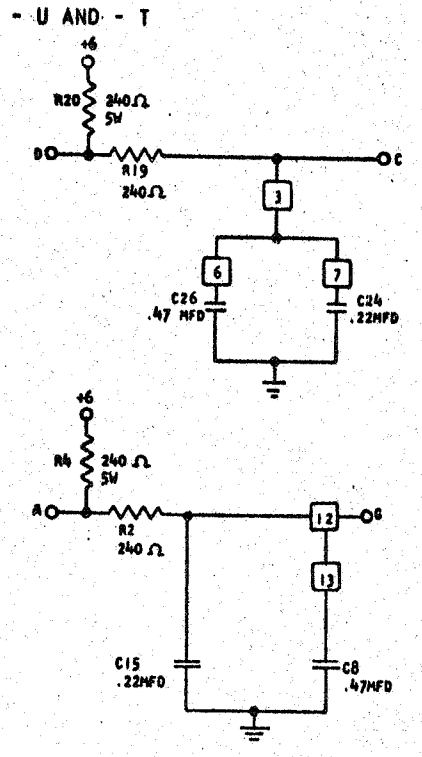
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371635

CTDL - INTEGRATOR - U AND - T







APPLICATION

1. USED TO PROVIDE AN OUTPUT THAT IS FREE OF INTERMITTENT FLUCTUATIONS RESULTING FROM BOUNCING OF MECHANICAL OPERATED CONTACTS

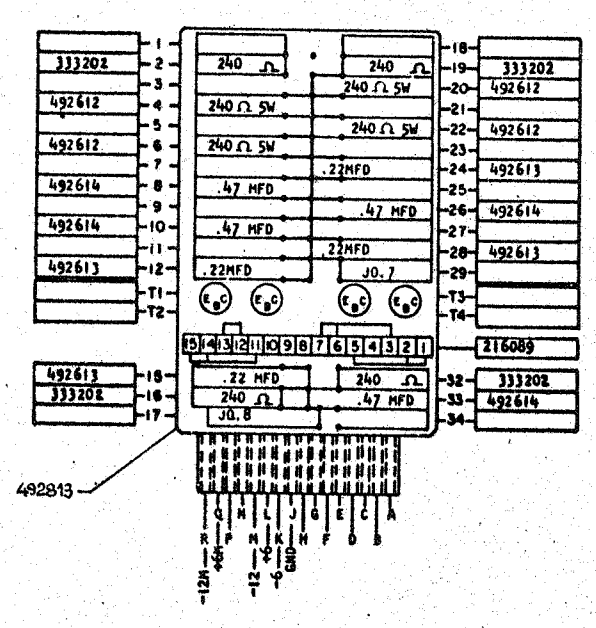
2. B, C, N, G ARE AT +6 LEVEL IF CONTACT IS OPEN AND -6 LEVEL IF CLOSED

3. WHEN THE INPUT IS MADE THROUGH A CAM TO 130 OHMS TIED TO -12 VOLTS, THE OUTPUT IS A-T LINE. DELAY IS AS FOLLOWS: RTH=325 OHMS, 3T=3RTH C.

	MINIMUM	MAXIMUM	CAPACITANCE
TURN ON	3T=510 USEC	3T=845 USEC	.69UF
TURN ON	348	580	.47UF
TURN ON	162	268	.22UF
RTH=480 OHMS			
TURN OFF	3T=755	1250	.69UF
TURN OFF	514	852	.47UF
TURN OFF	240	400	.22UF

4. WHEN THE INPUT IS MADE THROUGH A CAM TO -12 VOLTS, THE OUTPUT IS A-U LINE. DELAY IS AS FOLLOWS: RTH=240 OHMS

	MINIMUM	MAXIMUM	CAPACITANCE
TURN ON	3T=377 USEC	626 USEC	.69UF
TURN ON	257	426	.47UF
TURN ON	120	200	.22UF
RTH=480 OHMS			
TURN OFF	3T=754 USEC	1254 USEC	.69UF
TURN OFF	514	852	.47UF
TURN OFF	240	400	.22UF



INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-CTOL- INTEGRATOR - U AND T				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-29-62	EC 115599					
30-4-63	JT 83687					

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

729886

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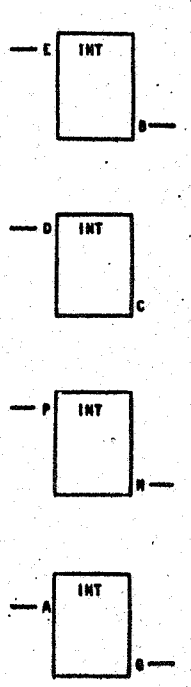
729887 | STANDARDS CODE

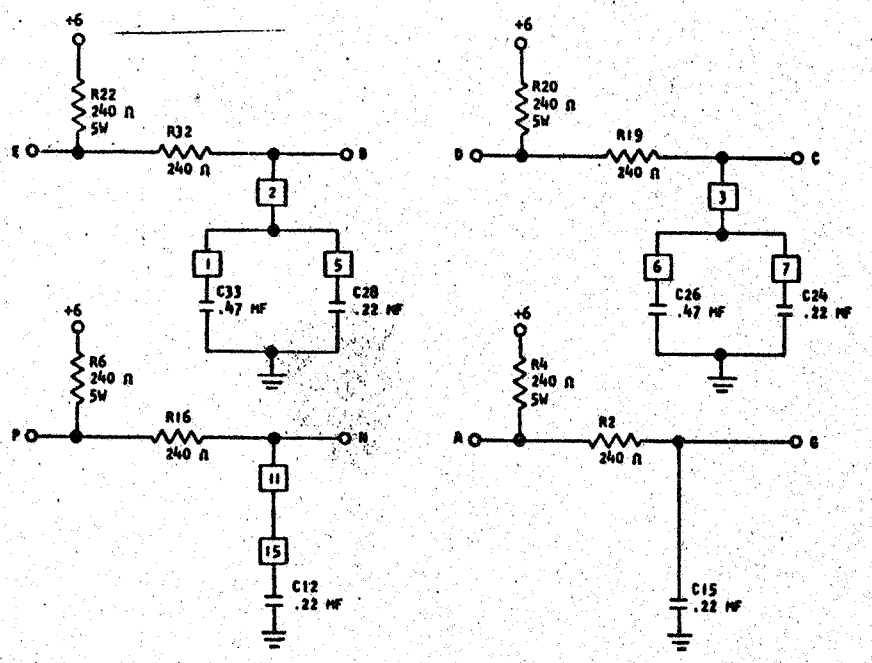
CARD CODE: NG XX | 729887

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371996

CTDL - INTEGRATOR - U AND - T





APPLICATION

1. USED TO PROVIDE AN OUTPUT THAT IS FREE OF INTERMITTENT FLUCTUATIONS RESULTING FROM BOUNCING OF MECHANICAL OPERATED CONTACTS

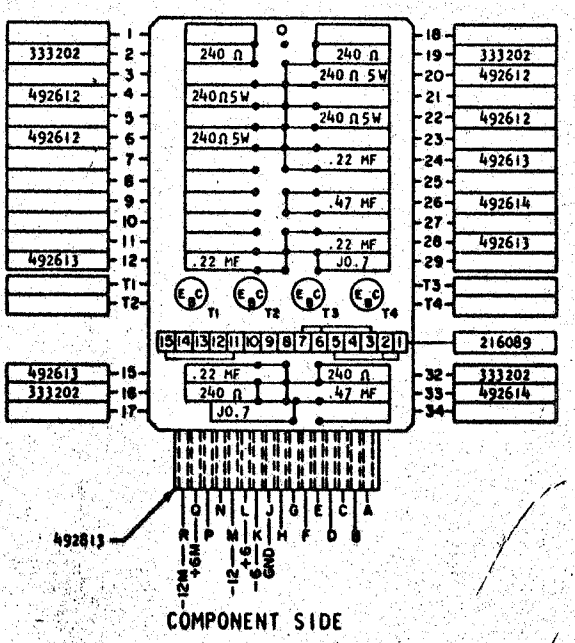
2. B, C, N, G ARE AT +6 LEVEL IF CONTACT IS OPEN AND -6 LEVEL IF CLOSED

3. WHEN THE INPUT IS MADE THROUGH A CAM TO 130 OHMS TIED TO -12 VOLTS, THE OUTPUT IS A-T LINE. DELAY IS AS FOLLOWS. RTH=325 OHMS. 3T=3RTH C.

	MINIMUM	MAXIMUM	CAPACITANCE
TURN ON	3T=510 USEC	3T=845 USEC	.69UF
TURN ON	348	580	.47UF
TURN ON	162	268	.22UF
	RTH=480 OHMS		
TURN OFF	3T=755	1250	.69UF
TURN OFF	514	852	.47UF
TURN OFF	240	400	.22UF

4. WHEN THE INPUT IS MADE THROUGH A CAM TO -12 VOLTS, THE OUTPUT IS A-U LINE. DELAY IS AS FOLLOWS: RTH=240 OHMS

	MINIMUM	MAXIMUM	CAPACITANCE
TURN ON	3T=377 USEC	626 USEC	.69UF
TURN ON	257	426	.47UF
TURN ON	130	200	.22UF
	RTH=480 OHMS		
TURN OFF	3T=754 USEC	1254 USEC	.69UF
TURN OFF	514	852	.47UF
TURN OFF	240	400	.22UF



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD

APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL- INTEGRATOR - U AND - T					6-26-62	EC 115599					
						30-4-63	JT 83687					
DESIGN				MODEL	SMS							
DETAIL	RQ	3-1-62		SCALE	NONE							
CHECK	WH	3-1-62		DRAW	LIG 3-17-62							
APPRO				CHECK								

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CARD CODE 729888

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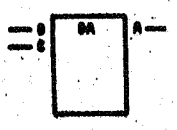
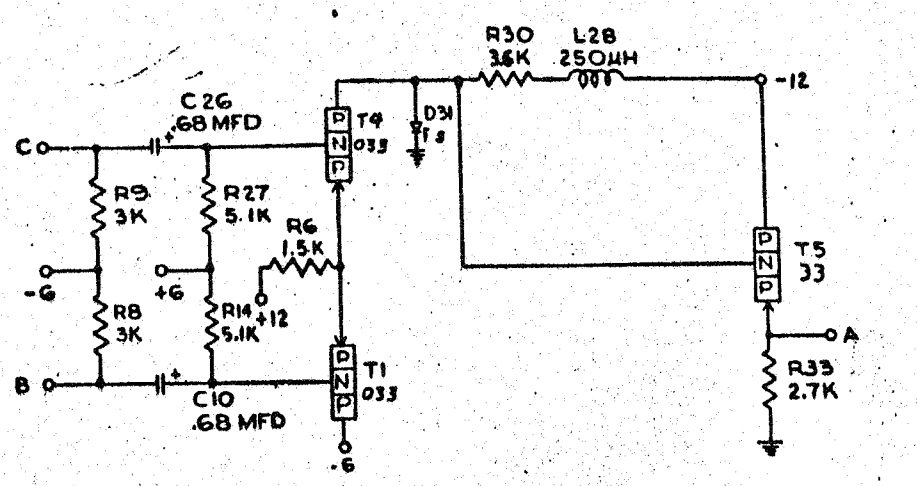
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371671

ALLOY DIFFERENCE AMPLIFIER

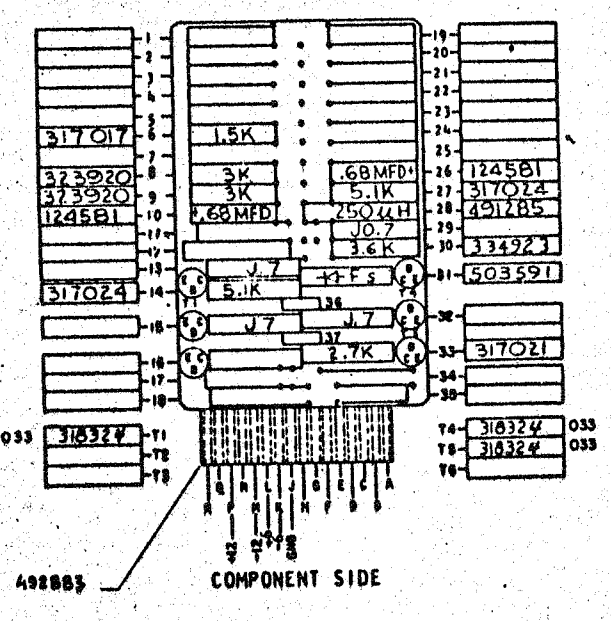




SEQUENCE OF OPERATION

1. 50 TO 100 MV P-P INPUT SIGNAL REQUIRED
2. OUTPUT WILL FOLLOW B INPUT

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C		INPUT		UP		
				DOWN		
B		INPUT		UP		
				DOWN		
A	U	OUTPUT		UP		0.0
				DOWN		-5.0



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR - ALLOY DIFFERENCE AMPLIFIER					6-26-62	EC115599					
				MODEL	SMS	30.4.62	7783687					
DESIGN												
DETAIL	AQ	5-1-62	SCALE	NONE								
CHECK	WH	5-1-62	DRAW	LIG	5-17-62							
APPRD			CHECK									

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STANDARDS CODE

CARD CODE	729889
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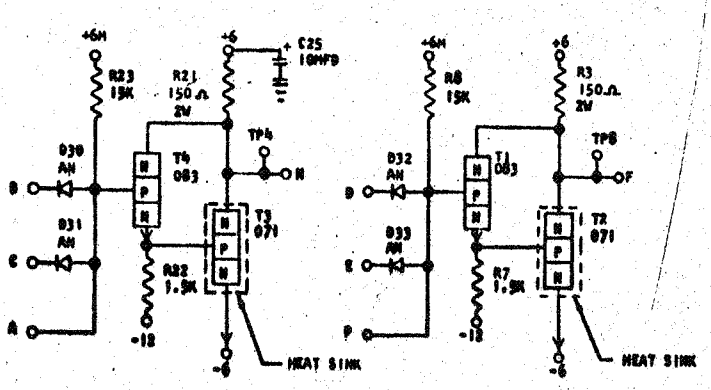
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371676

CTDL POWER INVERTER "P" TYPE



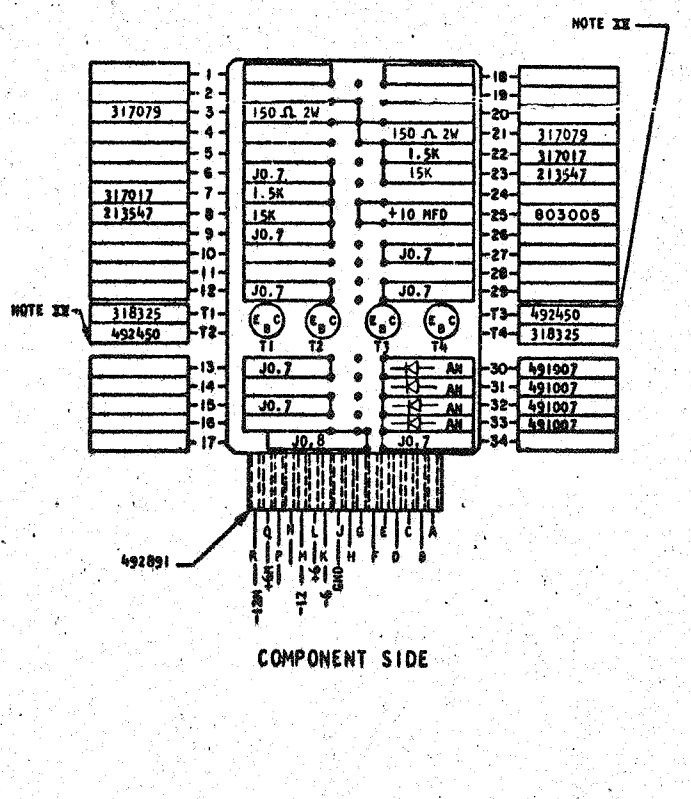
SEQUENCE OF OPERATION

1. ALL INPUTS UP TRANSISTORS ON OUTPUT DOWN.
2. ANY INPUT DOWN TRANSISTORS OFF OUTPUT UP.
3. INPUTS TO EXTENDER CARD MUST BE UP IN COINCIDENCE WITH INPUTS TO CARD FOR DOWN OUTPUT.
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
B,D	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
C,E	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
A,P		EXTENDER INPUT		UP	-6	
				DOWN	-12	
N,F	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.40
TURN OFF	0.10	0.15



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR-CTDL				6-26-62	EC115599					
	POWER INVERTER P TYPE				30.4.63	JT83687					
DESIGN			MODEL	SMS							
DETAIL	RG	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 6-17-62							
APPRO			CHECK								

C

729889

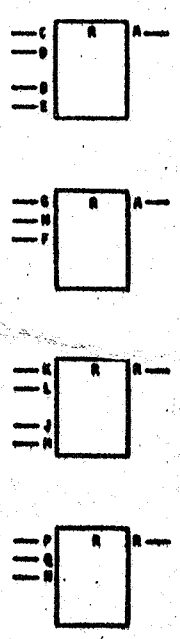
729890

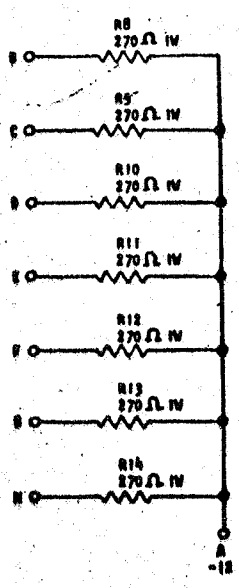
CARD CODE 729890
NW --

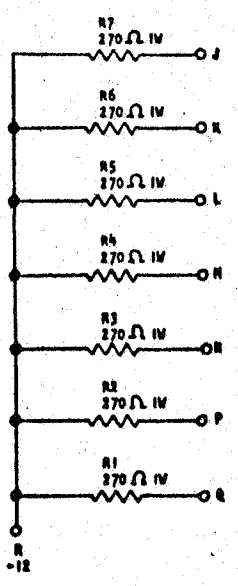
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371598

270Ω RESISTOR CARD

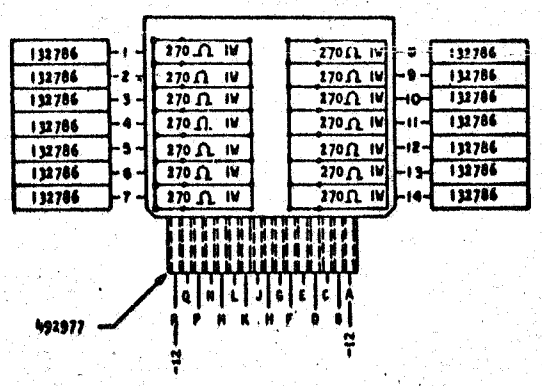






APPLICATION

1. ALLOWS MECHANICAL SWITCH INPUT TO CTRL BLOCK
2. SWITCH OPEN OUTPUT -12V, SWITCH CLOSED OUTPUT GROUND LEVEL
3. EACH RESISTOR IS USED INDIVIDUALLY



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM RESISTOR -270Ω				6-26-62	EC 115599					729890
					30-4-63	TT83687					
DESIGN			MODEL	SMS							
DETAIL	AQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIB 3-17-63							
APPROV			CHECK								

C

729890

729891 STANDARDS CODE

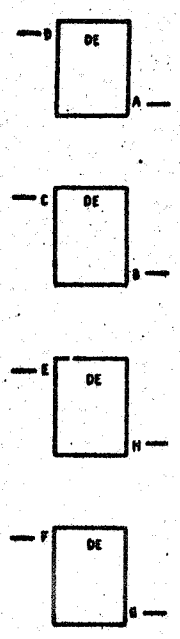
CARD CODE 729891

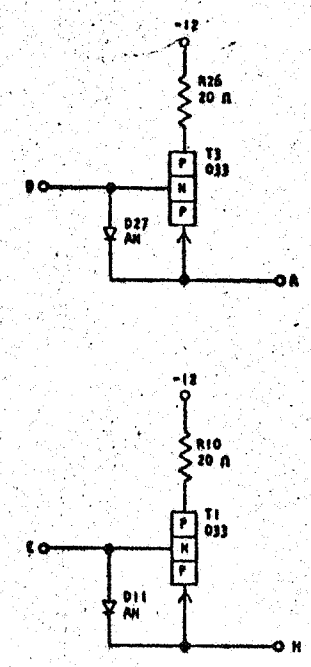
PP --

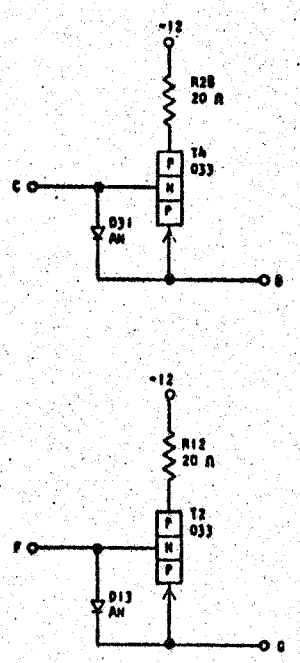
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371365

CTDL EMITTER FOLLOWER - PNP







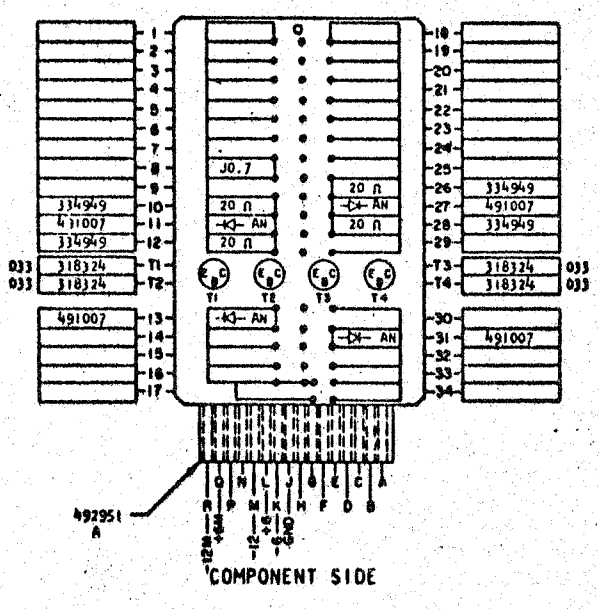
SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT DOWN
2. INPUT UP TRANSISTOR OFF OUTPUT UP
3. CIRCUIT MAY DRIVE UP TO 40 1-WAY LOGIC BLOCKS.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
D,E, C,F	U	INPUT		UP	-0.54	0.24
				DOWN	-9.66	-12.5
A,H, B,G	U	OUTPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

NO APPRECIABLE DELAY BETWEEN THE INPUT AND OUTPUT OF THE HIGH DRIVE EF.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- CTDL EMITTER FOLLOWER-PNP					12-62	EC115599					729891
DESIGN			MODEL	SMS		30.4.63	JT83687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRD			CHECK									

C

729891

729892

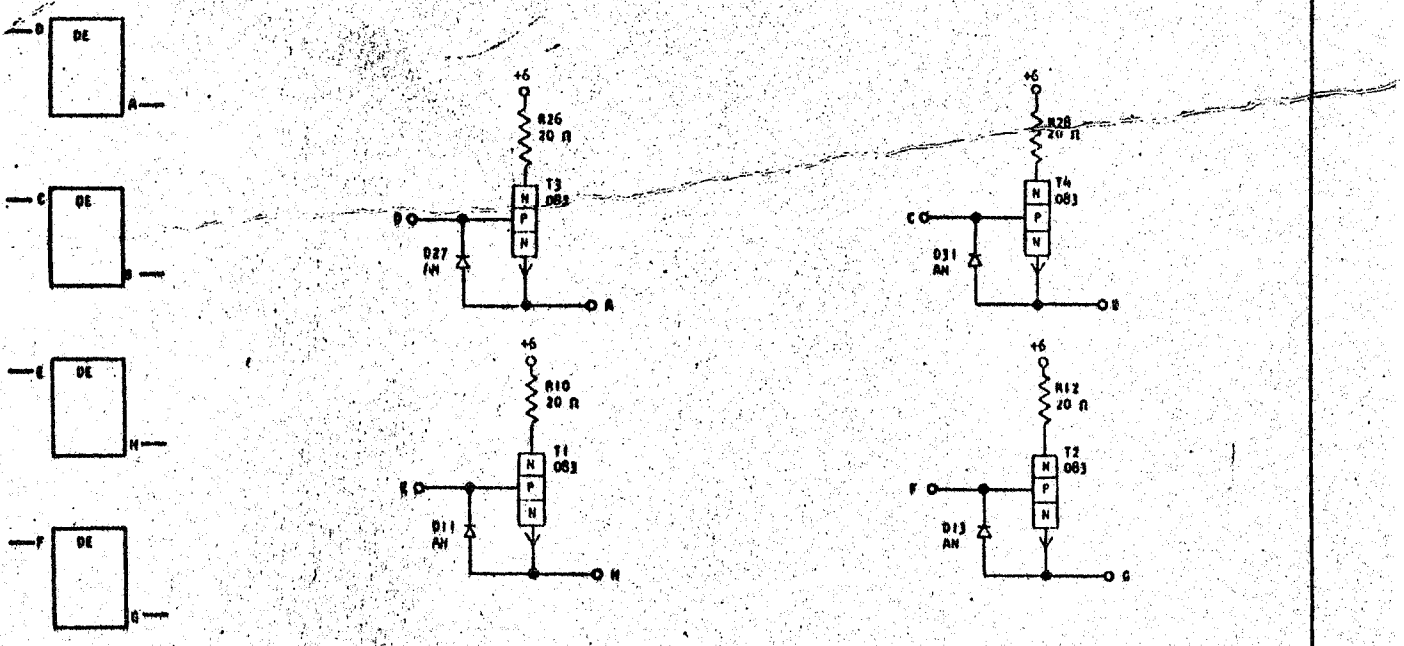
CARD CODE 729892

PQ --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371370

CTDL EMITTER FOLLOWER - NPN



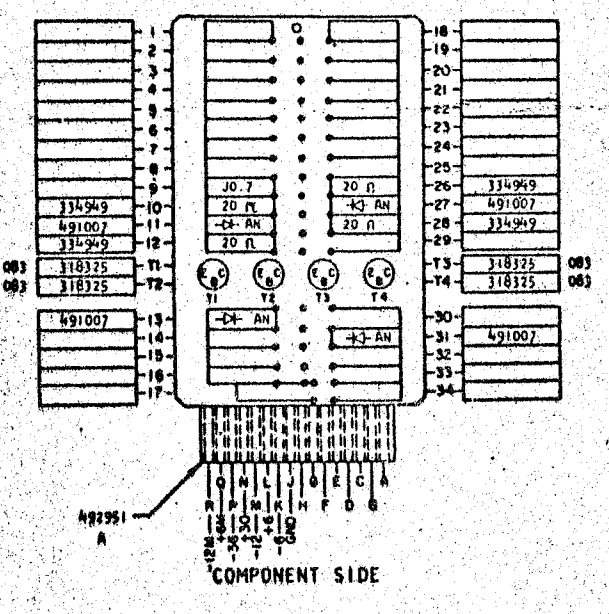
SEQUENCE OF OPERATION

1. OUTPUT WILL FOLLOW INPUT
2. CIRCUIT MAY DRIVE UP TO 40 1-WAY LOGIC BLOCKS.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D,C, E,F	T	INPUT		UP	4.26	6.24
				DOWN	-5.46	-6.24
A,B, H,G	T	OUTPUT		UP	3.89	6.24
				DOWN	-4.46	-6.24

DELAY - USEC

NO APPRECIABLE DELAY BETWEEN THE INPUT AND OUTPUT OF THE HIGH DRIVE EF.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-CTDL EMITTER FOLLOWER-NPN				6-14-62	EC 115599						729892
					30.4.63	TT83687						
DESIGN			MODEL	SMS								
DRAFT	RC	3-1-62	SCALE	NONE								
CHECK	WH	3-1-63	DRAW	LIG 3-17-63								
APPRO			CHECK									

C

729893 STANDARDS CODE

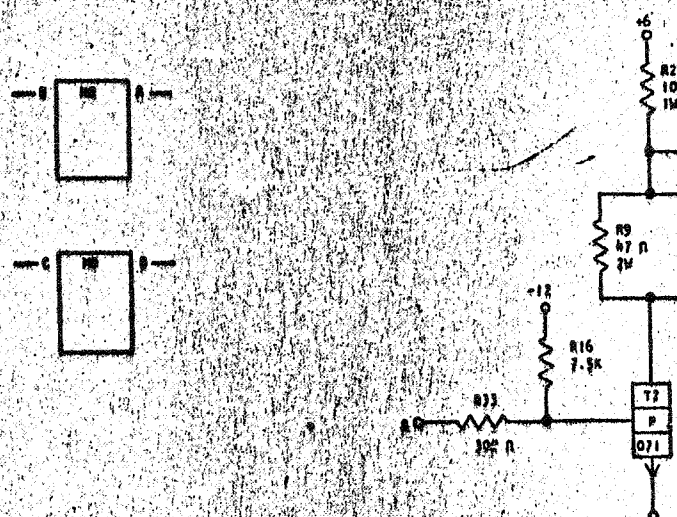
CARD CODE 729893

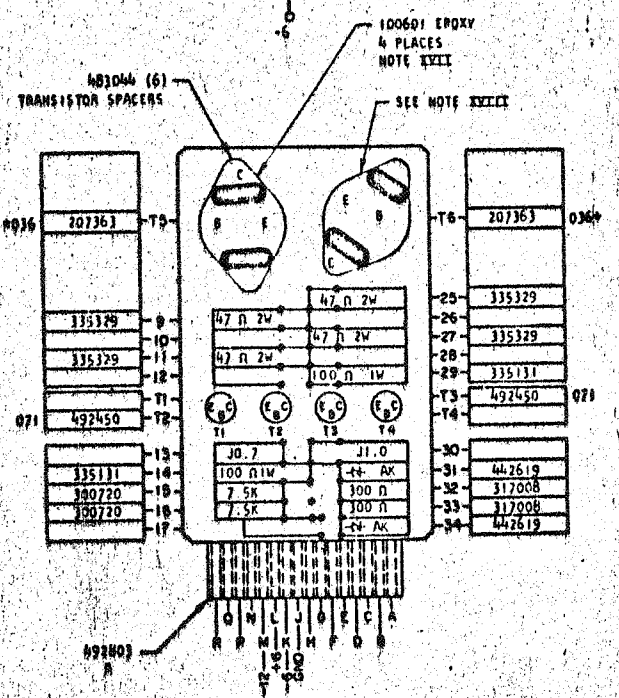
QC --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371633

ALLOY-CLUTCH MAGNETIC DRIVER





SEQUENCE OF OPERATION

INPUT UP TRANSISTORS ON OUTPUT UP

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
B,C	U	INPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
A,D		OUTPUT		UP	-1.24	+.24
				DOWN	-20	-20
F,E		CLAMP		UP	-20	-20
				DOWN	-20	-20

C

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-ALLOY CLUTCH MAGNETIC DRIVER					6-29-62	EC 115599					
					10-4-63	TT83687					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LTG 3-1-62							
APPRO			CHECK								

729893

STANDARDS CODE

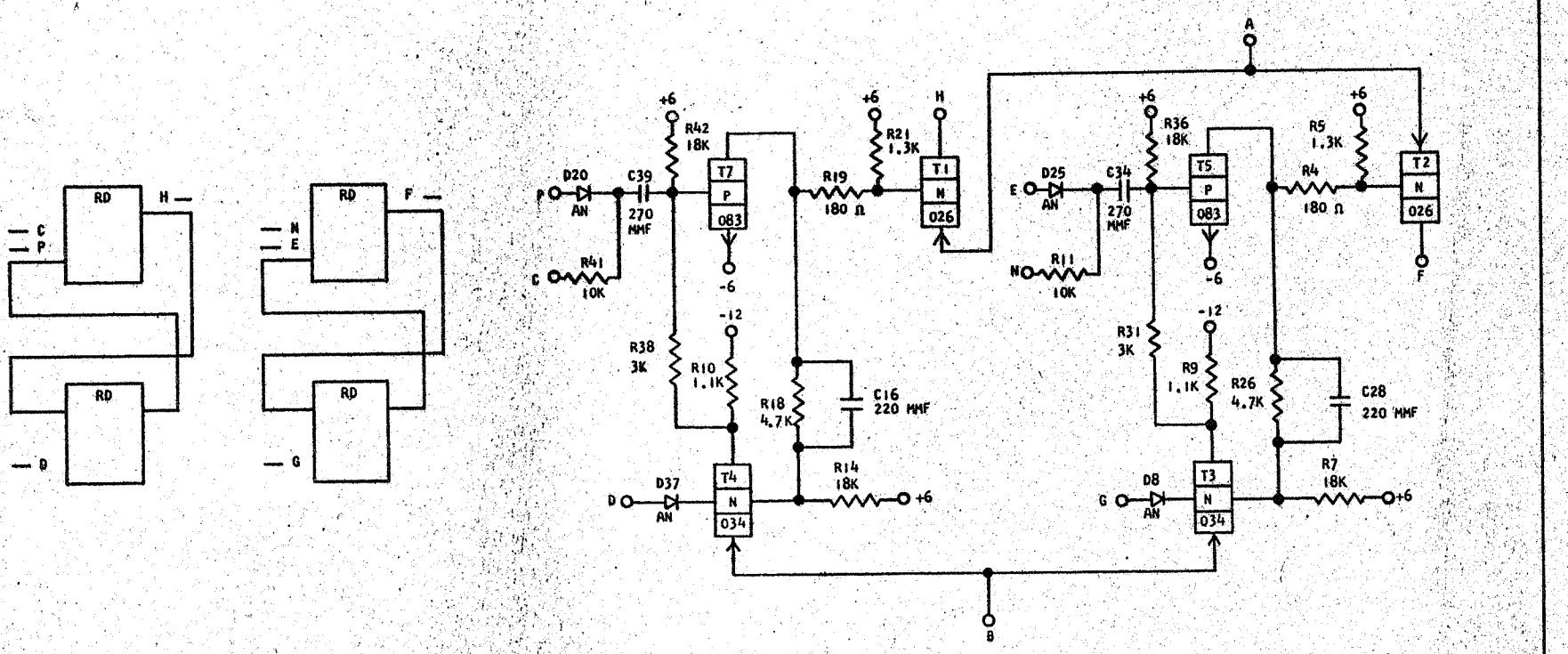
729894

CARD CODE	729894
QD --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371078

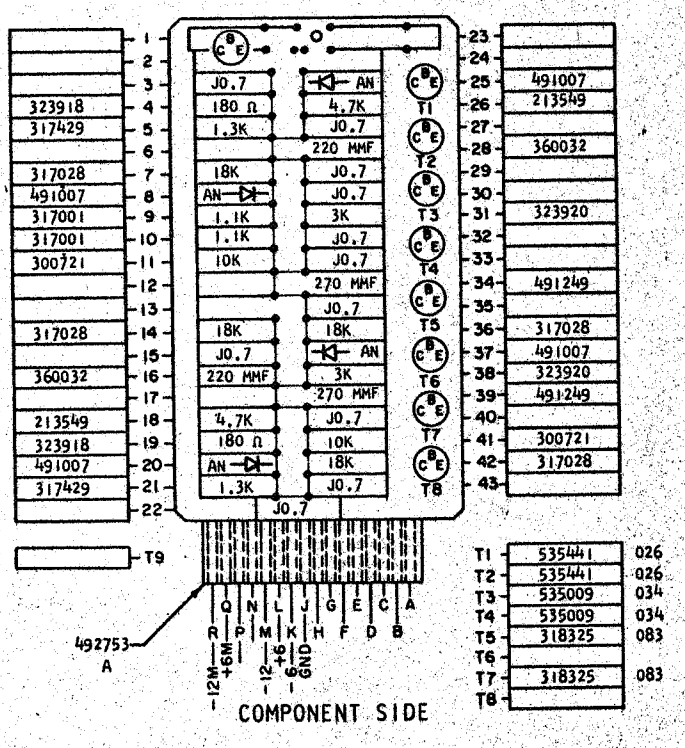
ALLOY-RELAY DRIVER



SEQUENCE OF OPERATION

1. PIN C MUST BE DOWN 7.5 U SEC BEFORE P GOES TO UP LEVEL, TURNING T7 ON. T7 ON TURNS TI & T4 ON. T4 PROVIDES LATCH BACK TO HOLD T7 ON.
2. UP LEVEL AT D OR MECHANICAL RESET AT B WILL TURN T4 OFF AND OPEN LATCH BACK TO T7.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
C, N	U	INPUT		UP	-3.0	0.2
				DOWN	-10.0	-12.5
P, E	U	INPUT		UP	-0.5	0.2
				DOWN	-8.5	-12.5
D, G	T	RESET		UP	1.4	6.2
				DOWN	-0.7	-6.2
H, F	W	OUTPUT		UP	0.2	
				DOWN		-45



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR DRIVER			MODEL	SMS	4 .. 62	115599					
DESIGN				SCALE	NONE							
DETAIL	RQ	3-1-62		DRAW	LIG 3-17-62							
CHECK	WH	3-1-62		CHECK								
APPRO												

729894

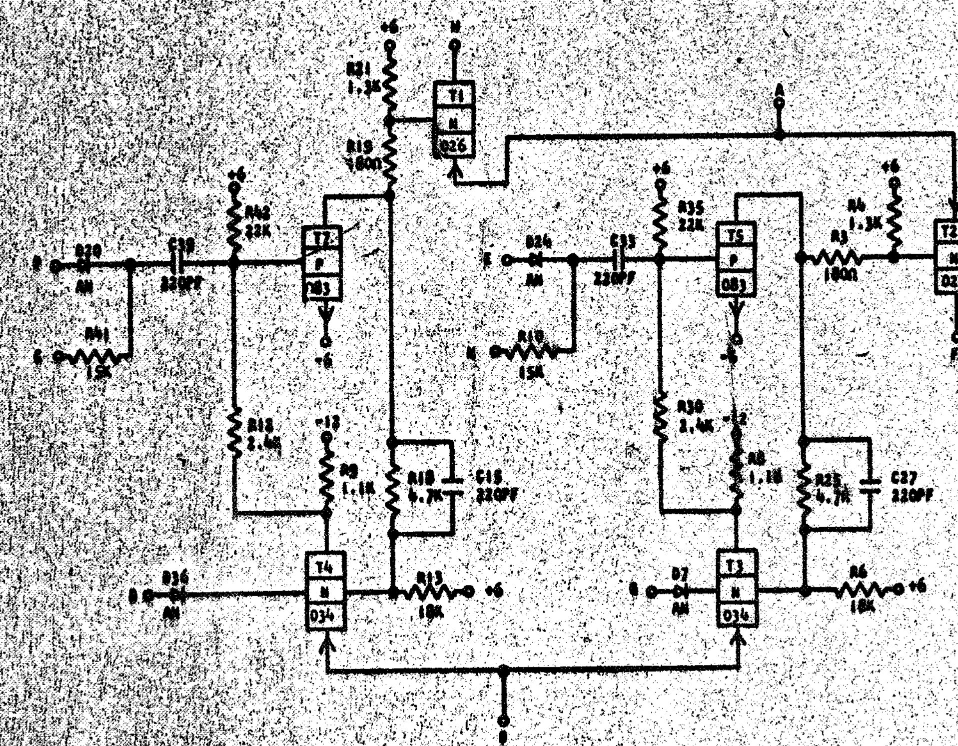
C

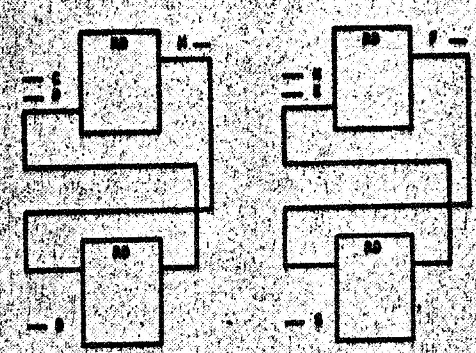
CARD CODE	729894
QD --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371078

ALLOY-RELAY DRIVER



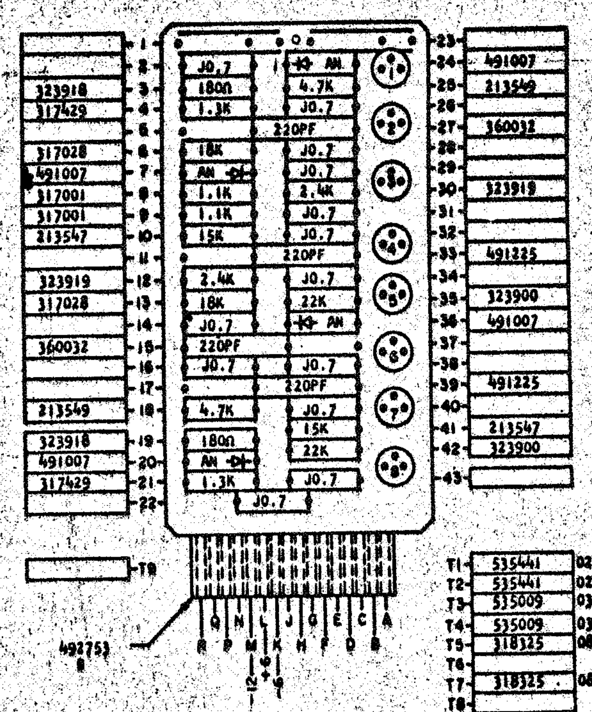


SEQUENCE OF OPERATION

1. PIN E MUST BE DOWN 7.5 U SEC BEFORE P GOES TO UP LEVEL, TURNING T7 ON. T7 ON TURNS T1 & T4 ON. T4 PROVIDES LATCH BACK TO HOLD T7 ON.

2. UP LEVEL AT D OR MECHANICAL RESET AT G WILL TURN T4 OFF AND OPEN LATCH BACK TO T7.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
C, N	U	INPUT		UP	-3.0	0.2
				DOWN	-10.0	-12.5
P, E	U	INPUT		UP	-0.5	0.2
				DOWN	-8.5	-12.5
D, G	T	RESET		UP	1.4	6.2
				DOWN	-0.7	-6.2
M, F	W	OUTPUT		UP	0.2	
				DOWN		-45



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR				6-26-62	115599					
	DRIVER				1-11-63	EC 116072					
DESIGN			MODEL	SMS	30-4-63	JT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	VH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729894

C

729894

729894

STANDARDS CODE

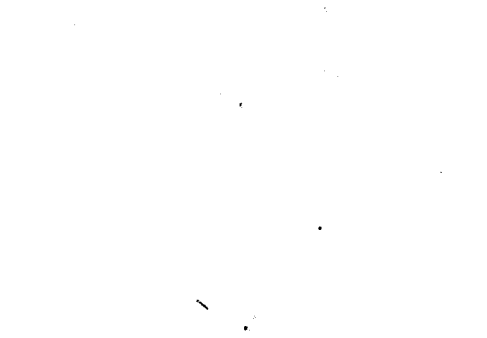
729894

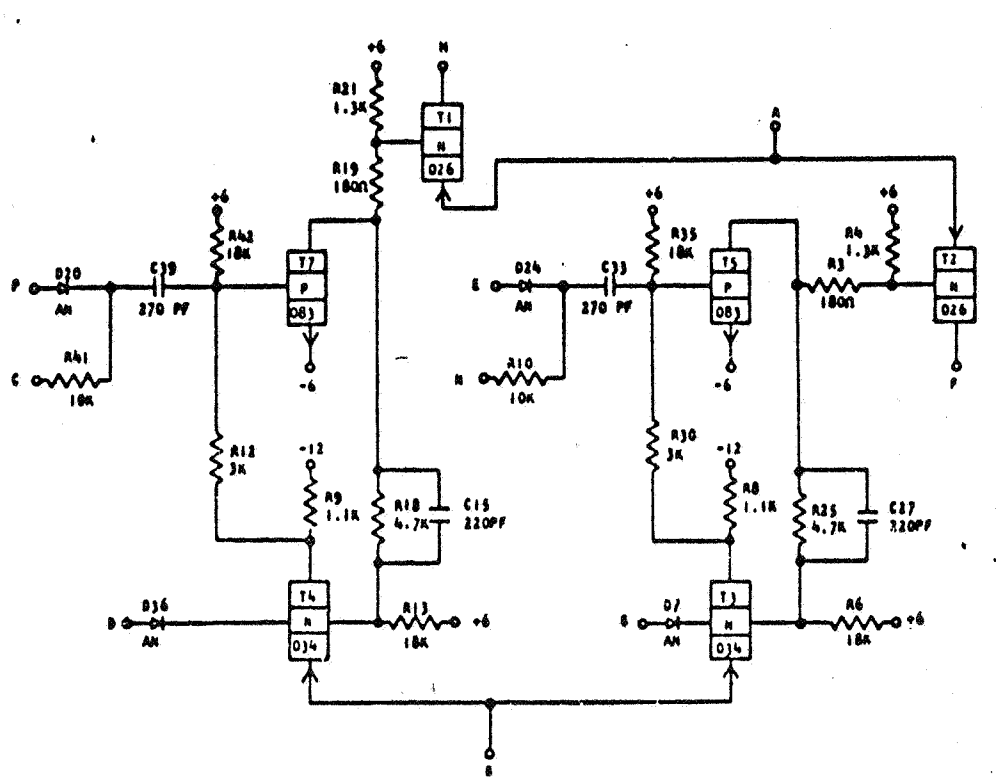
QD --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371078

ALLOY-RELAY DRIVER

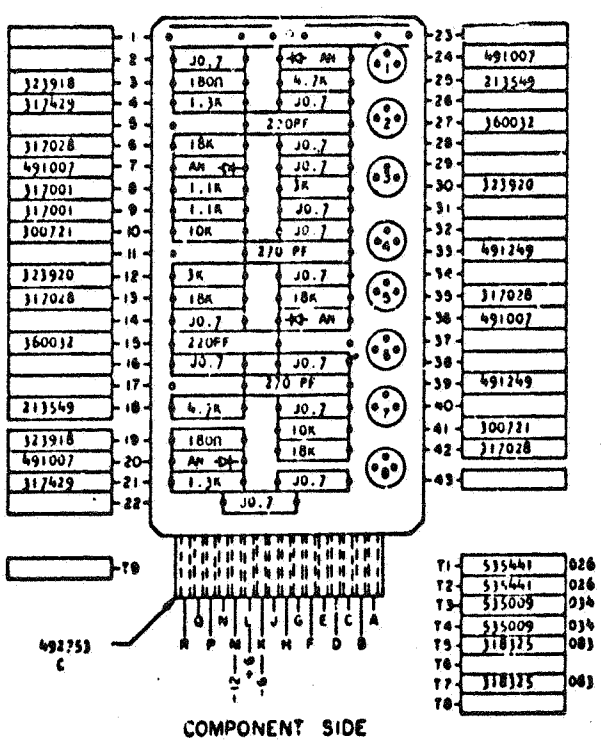




SEQUENCE OF OPERATION

1. PIN C MUST BE DOWN 7.5 U SEC BEFORE P GOES TO UP LEVEL, TURNING T7 ON. T7 ON TURNS T1 & T4 ON. T4 PROVIDES LATCH BACK TO HOLD T7 ON.
2. UP LEVEL AT B OR MECHANICAL RESET AT B WILL TURN T4 OFF AND OPEN LATCH BACK TO T7.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C, H	U	INPUT		UP	-5.0	0.2
				DOWN	-10.0	-12.5
P, E	U	INPUT		UP	-0.5	0.2
				DOWN	-8.5	-12.5
B, G	T	RESET		UP	1.4	6.2
				DOWN	-0.7	-6.2
H, F	M	OUTPUT		UP	0.2	
				DOWN		-45



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

APPROVAL	CHECK	MAT. LAB.	COMP. LAB.
Geb			
26.6.64			

C

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM YSYA DRIVER		MODEL	SMS	6-26-63	115599					
DESIGN					1-11-64	116072					
DETAIL	AQ	3-1-63	SCALE	NONE	4-4-63	116126					
CHECK	WH	3-1-63	DRAW	LIG 3-17-63	2-11-64	119678					
APPRO			CHECK		26.6.64 TA 769						

729894

729894

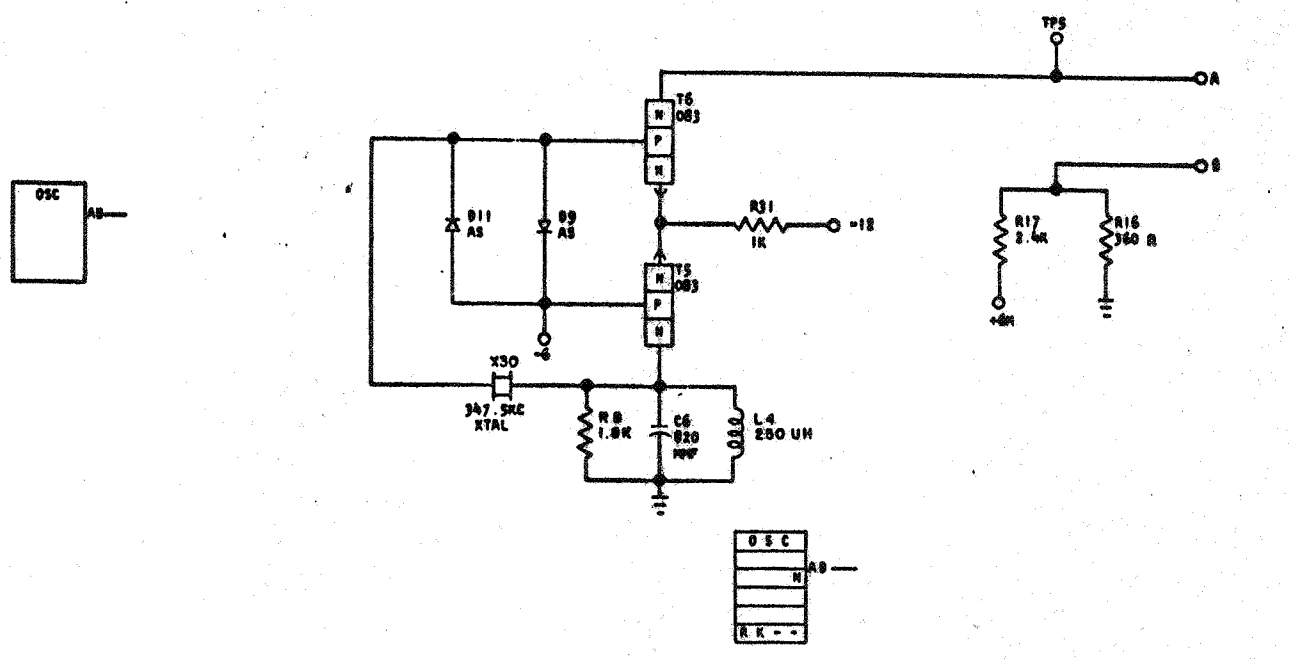
729895 STANDARD CODE

CARD CODE 729895
RK --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371788

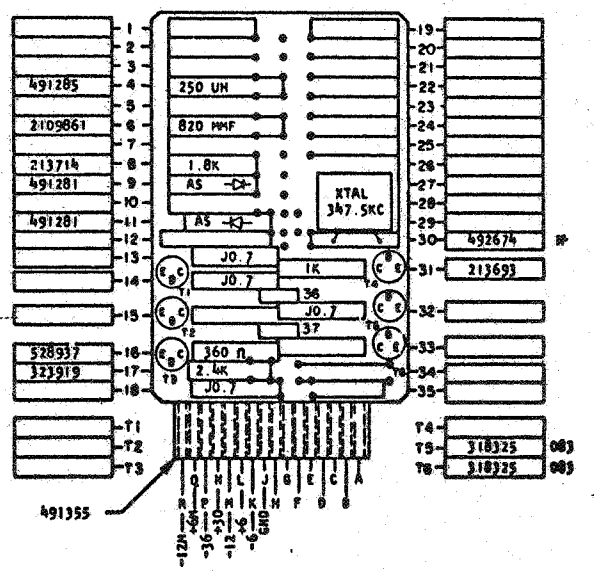
ALLOY - OSCILLATOR 347.5KC FREE RUNNING (CRYSTAL)



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR IS TURNED ON
2. PIN A MUST BE TIED TO PIN B FOR LOAD

PINS	SIGNAL NAME	WAVE SHAPE	LEVEL	MIN	MAX
A	OUTPUT		UP	.69	.86
			DOWN	-.9	-2.04



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-ALLOY-OSC				
347.5KC FREE RUNNING (CRYSTAL)					
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LTG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-16-62	EC 115599					
30.4.63	JT 83687					

729895

C

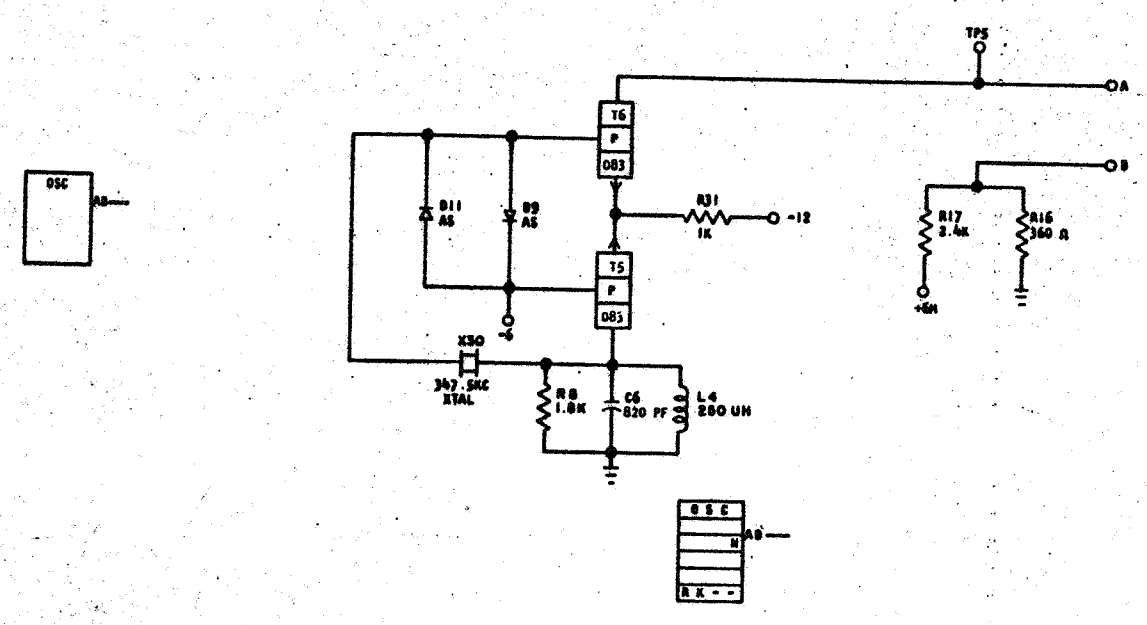
729895

CARD CODE 729895
RK --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371788

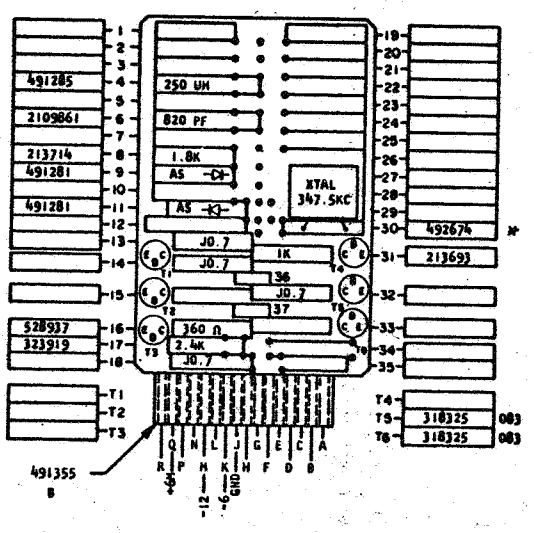
ALLOY - OSCILLATOR 347.5KC FREE RUNNING (CRYSTAL)



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR IS TURNED ON
2. PIN A MUST BE TIED TO PIN B FOR LOAD

PINS	SIGNAL NAME	WAVE SHAPE	LEVEL	MIN	MAX
A	OUTPUT		UP	.69	.86
			DOWN	-.9	-2.04



C

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-ALLOY-OSC 347.5KC FREE RUNNING (CRYSTAL)				6-16-62	115599					
DESIGN			MODEL	SMS	8-28-63	117802					
DETAIL	RQ	3-1-62	SCALE	NONE	19.2.64 TA 1841D						
CHECK	WH	3-1-62	DRAW	LTG 3-17-62							
APPRO			CHECK								

729895

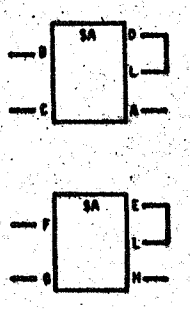
STANDARDS CODE	729896

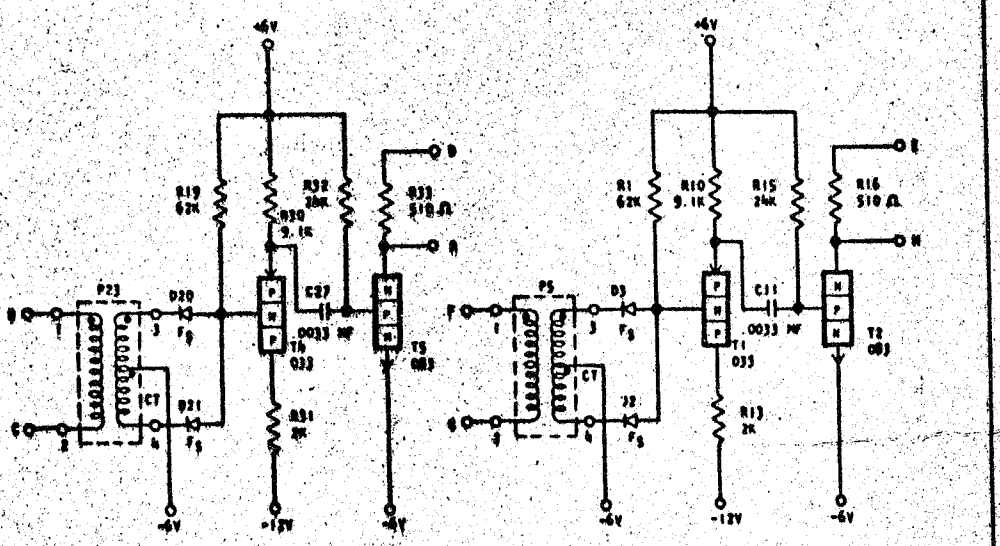
CARD CODE	729896
WL --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371898

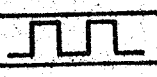
ALLOY-SENSE AMPLIFIER NO. 2
MOUNT CARD ON ONE INCH CENTERS

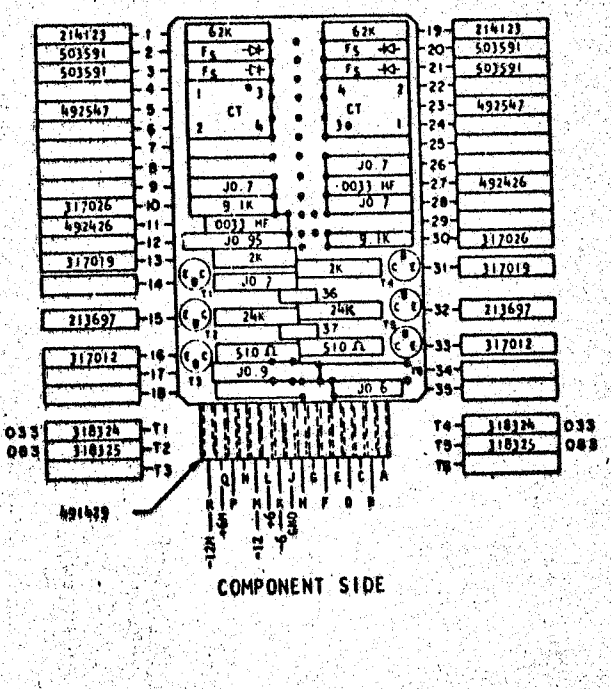




SEQUENCE OF OPERATION

1. WITH NO INPUT ALL TRANSISTORS ARE IN CONDUCTION; OUTPUT IS DOWN. E AND D ARE TIED TO +6V.
2. 50 MV MIN. P-P ACROSS B AND C IS STEPPED UP AND RECTIFIED APPEARING AS NEGATIVE SHIFT ON BASE OF T4. A NEGATIVE 1V SHIFT FROM T4 EMITTER THEN TURNS T5 OFF AND THE OUTPUT IS UP.
3. AMPLIFIER OUTPUT DELAY IS 1.0 USEC MAXIMUM. AMPLIFIER DELAY SHALL BE DEFINED AS THE TIME TAKEN FROM THE 50% POINT ON THE RISE OF THE "ONE" SIGNAL TO THE 10% POINT OF THE LEADING EDGE VOLTAGE TRANSITION AT THE OUTPUT.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,M.	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729896
NAME	CARD ASM TSTR - ALLOY SENSE AMPLIFIER NO. 2				6-27-62	EC 115599						
					10-4-63	TT 83687						
DESIGN			MODEL	SMS								
DETAIL	BG	8-1-62	SCALE	NONE								
CHECK	WH	8-1-62	DRAW	LIG 9-17-62								
APPRO			CHECK									

C

CARD CODE	729897
WX --	

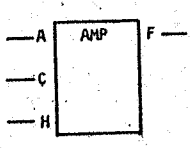
STANDARD CODE

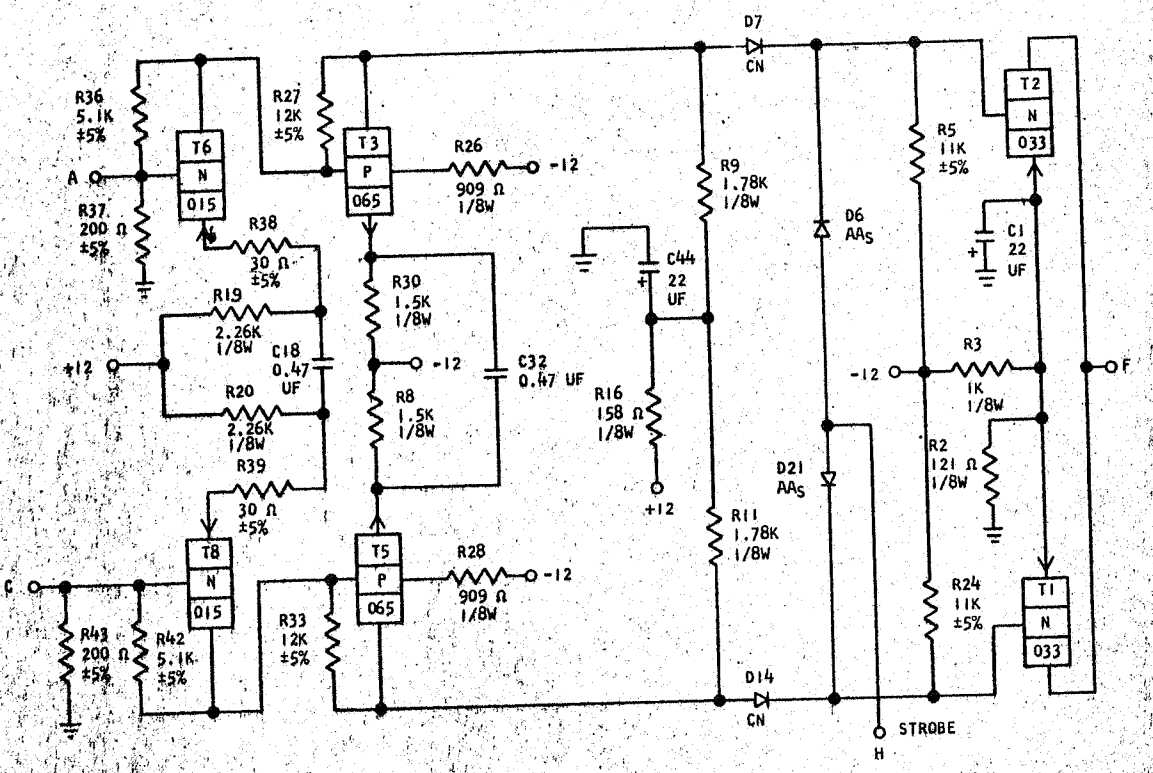
7 97

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371899

ALLOY-AMPLIFIER, PRE SENSE NUMBER 1

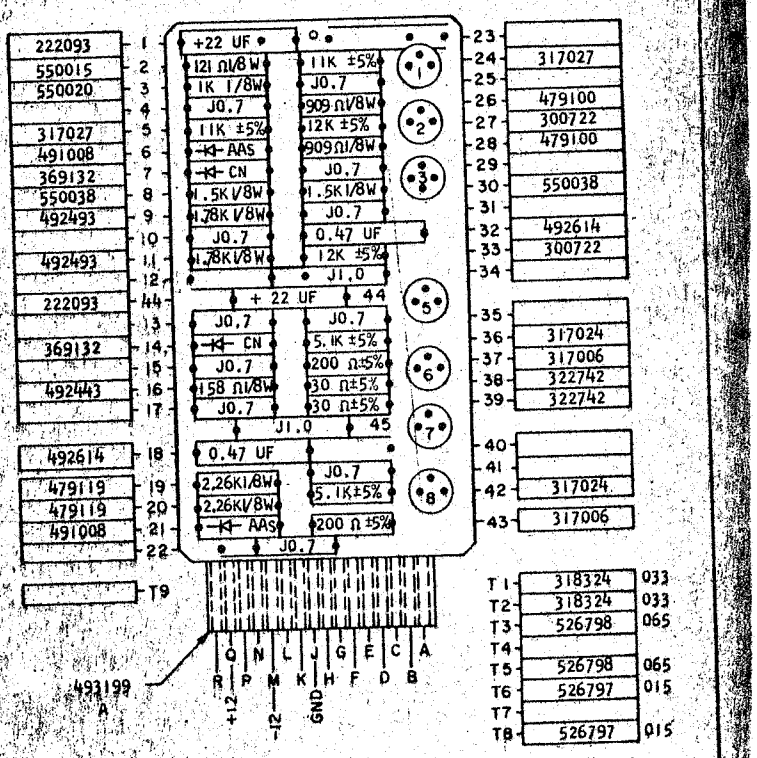




SEQUENCE OF OPERATION

1. THE T-LINE STROBE PLUSE GATES THE CORE PULSE FROM THE DIFFERENTIAL AMPLIFIER INTO EITHER Q33, WHICH THEN GOES INTO THE FINAL SENSE AMPLIFIER (370836)
2. AMPLIFIER OUTPUT DELAY IS <0.4 USEC. AMPLIFIER OUTPUT DELAY SHALL BE DEFINED AS THE TIME TAKEN FROM 10% POINT ON THE RISE OF THE INPUT SIGNAL TO THE 10% POINT OF THE LEADING EDGE VOLTAGE TRANSITION AT THE OUTPUT.

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,C	INPUT		UP	40 M	VOLTS
			DOWN	0	
F	OUTPUT		UP	-5.2	+.24
			DOWN	-11.52	-12.48
H	STROBE		UP	+1.44	+6.24
			DOWN	-.74	-6.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR - ALLOY AMPLIFIER PRE SENSE NUMBER 1				3-17-62	F15599						729897
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRD			CHECK									

C

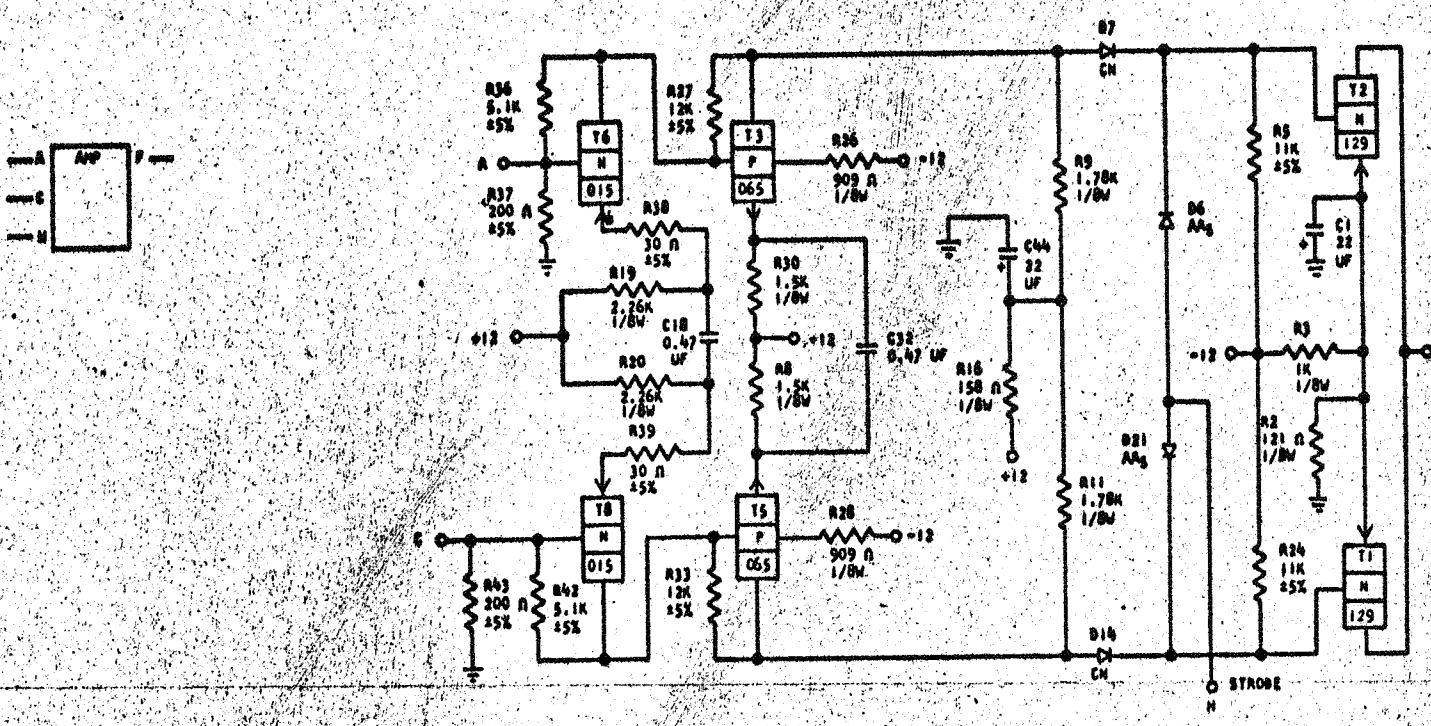
729897 STANDARDS CODE

CARD CODE 729897
WX --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371899

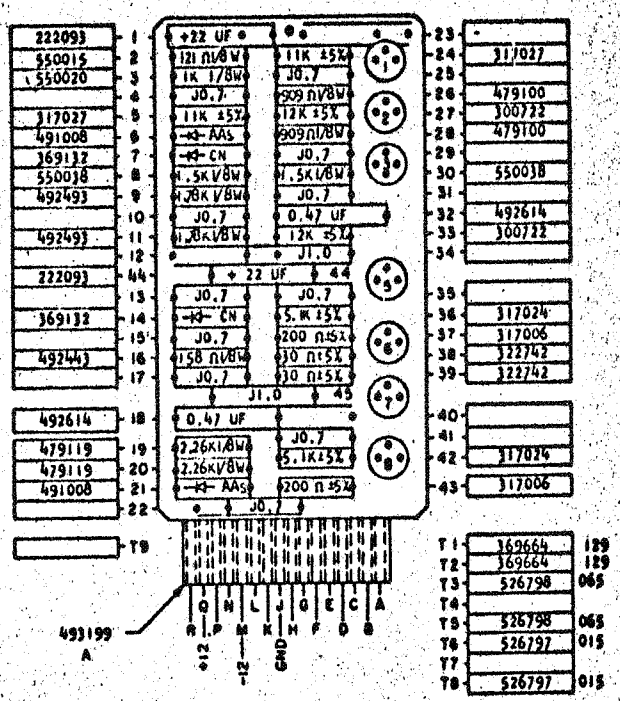
ALLOY-AMPLIFIER, PRE SENSE NUMBER 1



SEQUENCE OF OPERATION

1. THE T-LINE STROBE PLUSE GATES THE CORE PULSE FROM THE DIFFERENTIAL AMPLIFIER INTO EITHER 033, WHICH THEN GOES INTO THE FINAL SENSE AMPLIFIER (370836)
2. AMPLIFIER OUTPUT DELAY IS <0.4 USEC. AMPLIFIER OUTPUT DELAY SHALL BE DEFINED AS THE TIME TAKEN FROM 10% POINT ON THE RISE OF THE INPUT SIGNAL TO THE 10% POINT OF THE LEADING EDGE VOLTAGE TRANSITION AT THE OUTPUT.

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,C	INPUT		UP	40 M VOLTS	
			DOWN	0	
P	OUTPUT		UP	-5.2	+.24
			DOWN	-11.52	-12.48
M	STROBE		UP	+1.44	+6.24
			DOWN	-.74	-6.24



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - ALLOY AMPLIFIER PRE SENSE NUMBER 1					6-22-62	115599					729897
DESIGN			MODEL	SMS	9-10-63	117842					
DETAIL	RQ	3-1-62	SCALE	NONE	8.11.63	TA 1841B					
CHECK	WH	3-1-62	DRAW	L1B 3-7-62							
APPRO			CHECK								

C

729897 B

729898

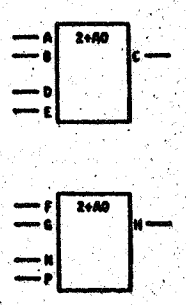
CARD CODE 729898

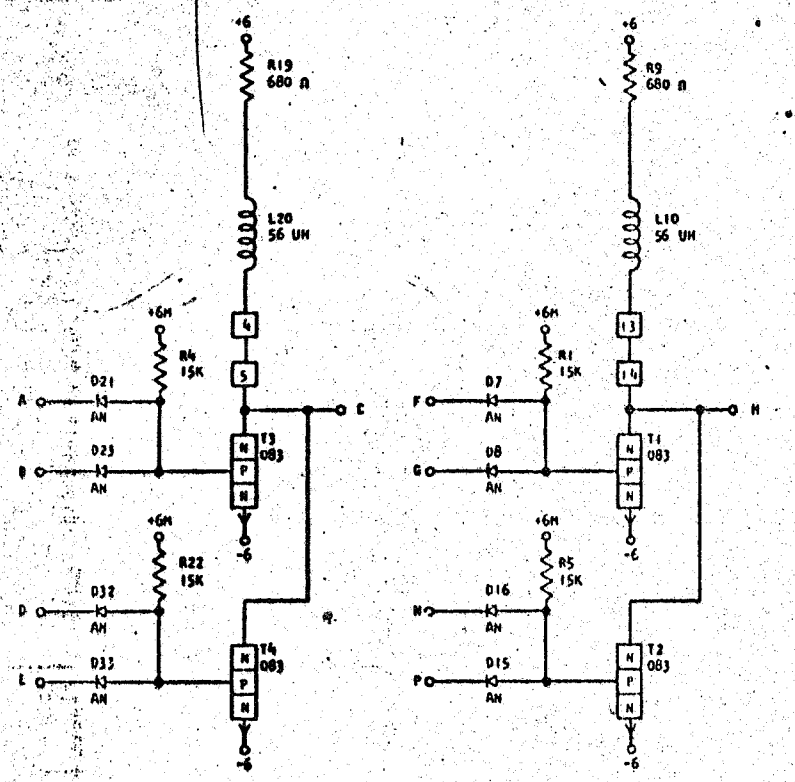
2J MX

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370144

CTDL NPN TWO WAY GATE W/ COLLECTOR LOAD





SEQUENCE OF OPERATION

1. BOTH INPUTS TO A TRANSISTOR UP, TRANSISTOR ON OUTPUT DOWN
2. FOR UP OUTPUT, EITHER INPUT TO BOTH TRANSISTORS MUST BE DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

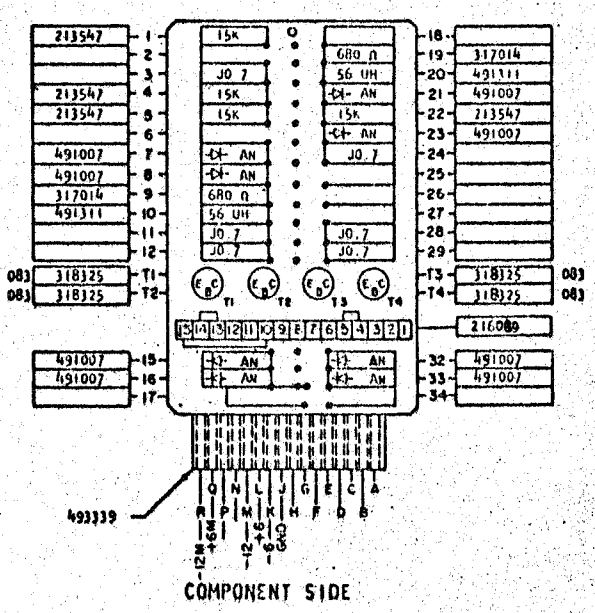
PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN.	MAX
A,D, F,N	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
B,G, E,P	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
C,H	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL NPN TWO WAY GATE W/ COLLECTOR LOAD					4-19-62	EC 115599					729898
						30-4-63	TT 83687					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRV			CHECK									

C

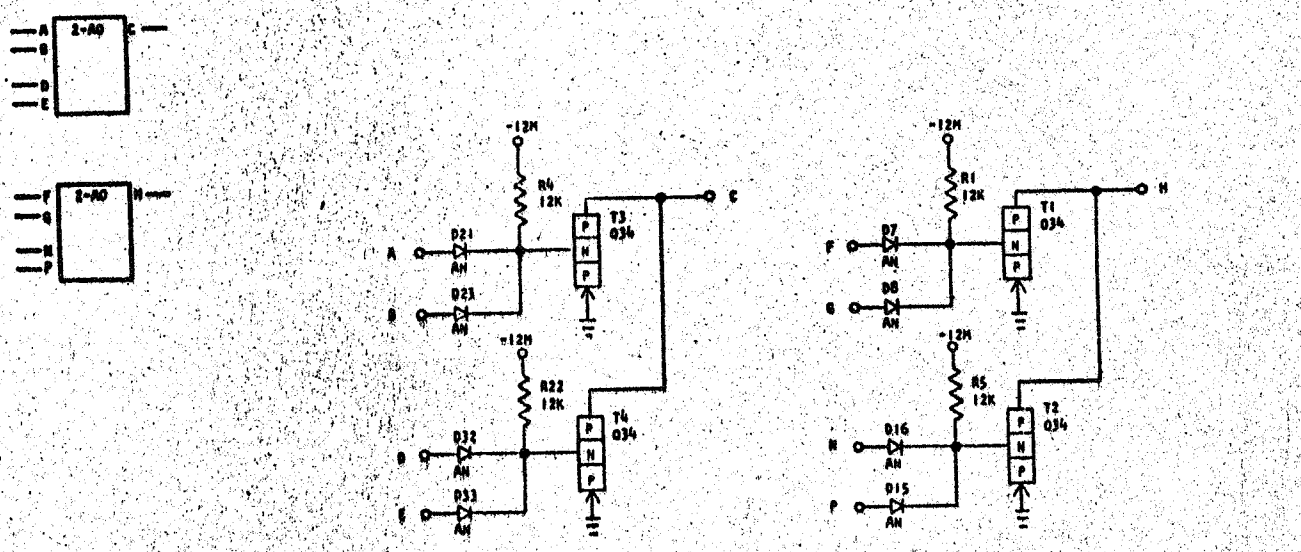
1 of 3

729899

CARD CODE	729899
3J MX	

REFERENCE DRAWING
SEE PRODUCTION DRAWING 370141

CTDL PNP TWO WAY GATE WITHOUT COLLECTOR LOAD



SEQUENCE OF OPERATION

1. BOTH INPUTS TO A TRANSISTOR DOWN, TRANSISTOR ON OUTPUT UP
2. FOR DOWN OUTPUT, EITHER INPUT TO BOTH TRANSISTORS MUST BE UP
3. EXTERNAL LOADING OF COLLECTORS REQUIRED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

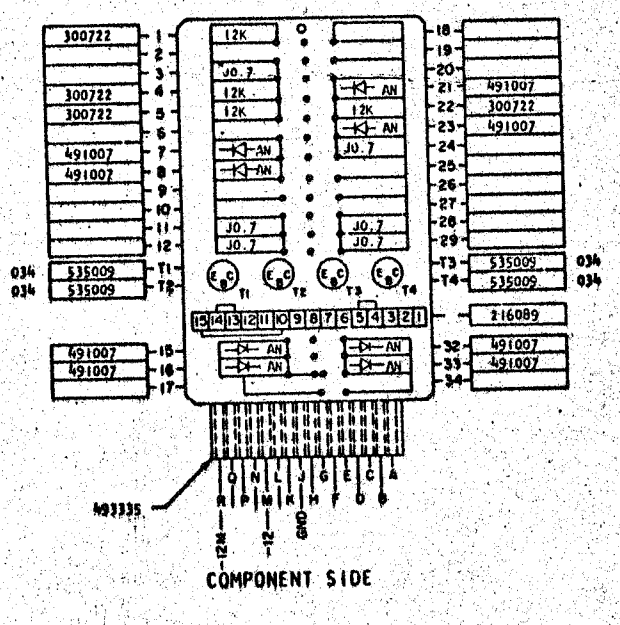
PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,B, F,H	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
D,G, E,P	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C,M	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHARGE NO.	APPROVAL	DATE	CHARGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-CTDL PNP TWO WAY GATE WITHOUT COLLECTOR LOAD	4-20-62	EC 115599					729899
DESIGN MODEL SMS	30.4.62	TT 83687					
DRAWN RO 3-1-62 SCALE NONE							
CHECK WH 3-1-62 DRAW LTR 3-17-62							
APPRD COPIES							

C

669 571

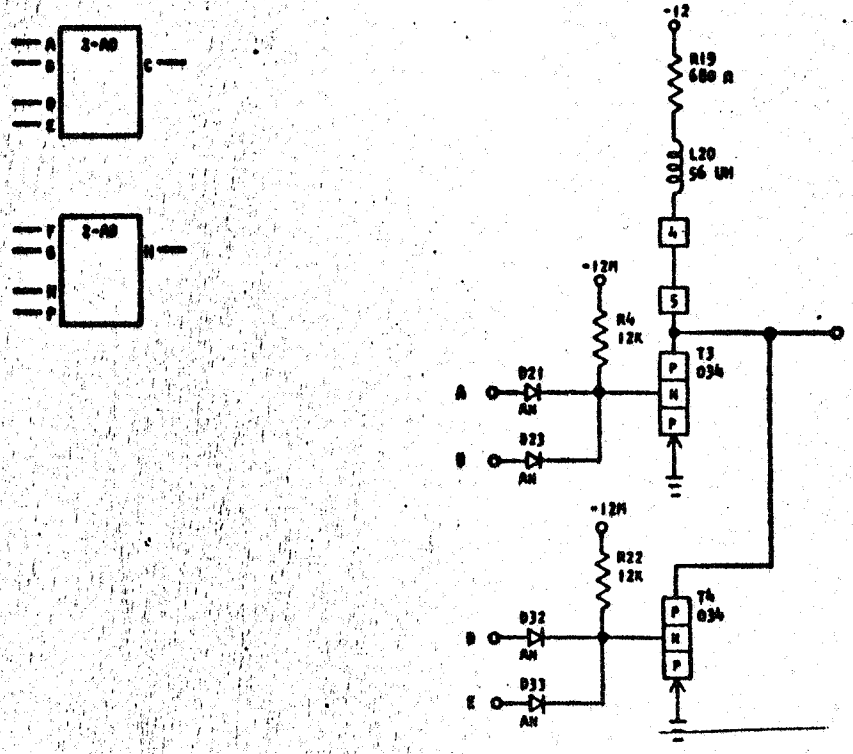
729900

CARD CODE	729900
4J MX	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370142

CTDL PNP TWO WAY GATE WITH COLLECTOR LOAD



SEQUENCE OF OPERATION

1. BOTH INPUTS TO A TRANSISTOR DOWN, TRANSISTOR ON OUTPUT UP
2. FOR DOWN OUTPUT, EITHER INPUT TO BOTH TRANSISTORS MUST BE UP
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

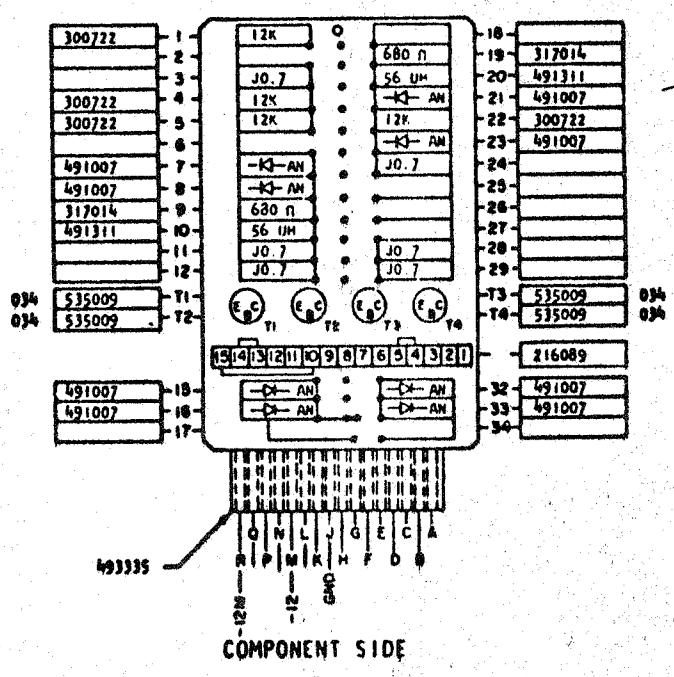
PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,F B,N	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
B,G E,P	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C,M	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL PNP					6-19-62	EC 115599					729900
TWO WAY GATE WITH COLLECTOR LOAD						10-4-63	TT83687					
DESIGN			MODEL	SMS								
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LTG	3-17-62							
APPRO			CHECK									

C

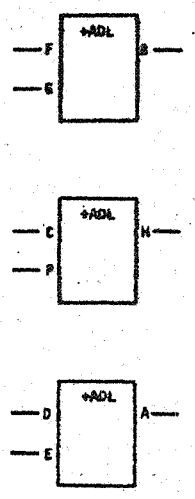
729900

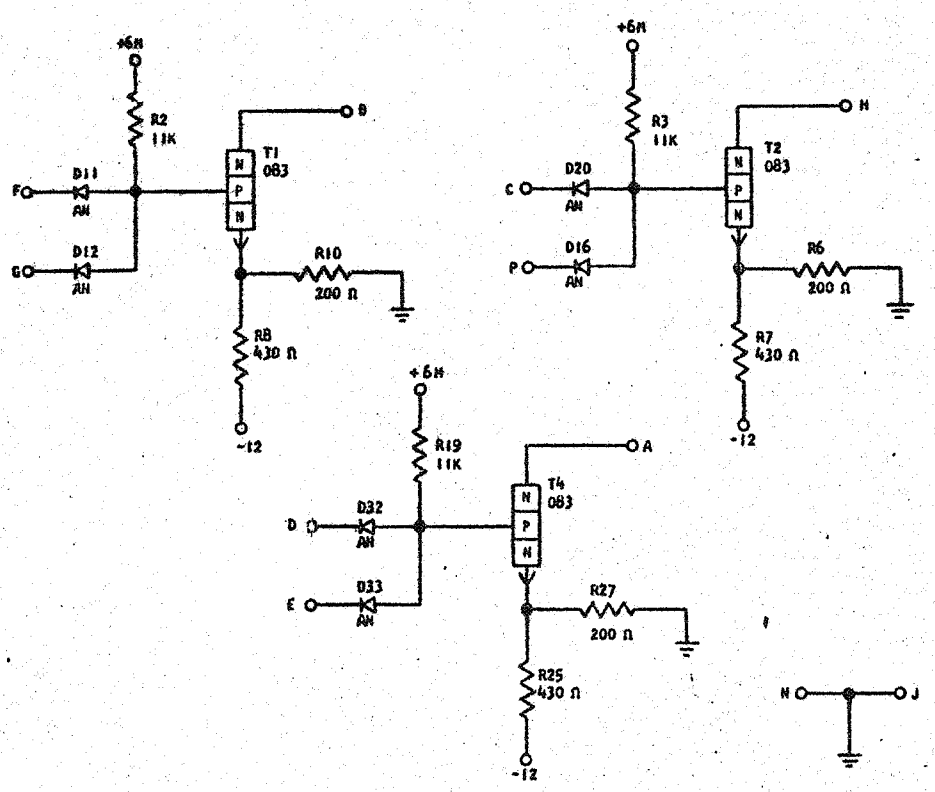
CARD CODE	729901
6J XD	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370089

CTDL STANDARD CABLE DRIVER





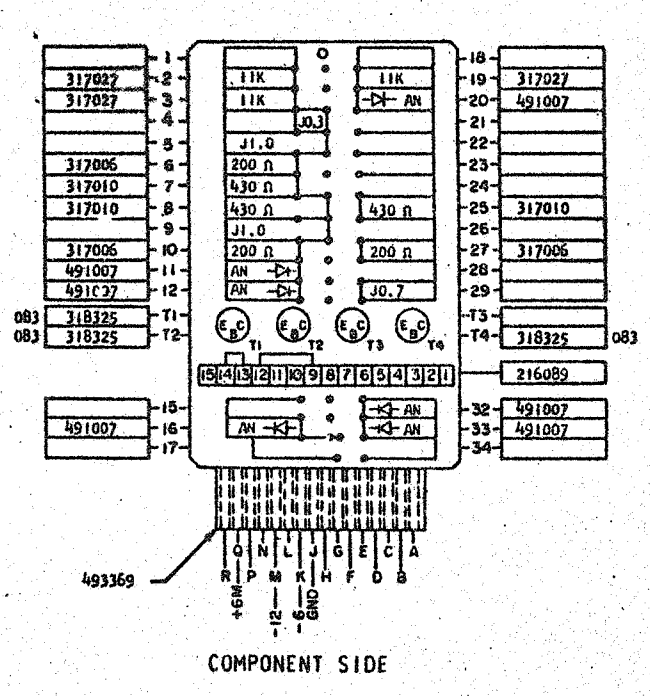
SEQUENCE OF OPERATION

1. ALL INPUTS UP TRANSISTOR ON OUTPUT DOWN
2. ANY INPUT DOWN TRANSISTOR OFF OUTPUT UP

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
F,C, D	U	INPUT		UP	-0.98	0.24
				DOWN	-7.44	-12.5
G,P, E	U	INPUT		UP	-0.98	0.24
				DOWN	-7.44	-12.5
B,H, A	N	OUTPUT		UP		
				DOWN	-1.25	-2.66
N,J		GROUND		UP		
				DOWN		

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	455	652
TURN OFF	48	94



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-CTDL DRIVER					-62	115599						729901
DESIGN				MODEL	SMS								
DETAIL	AQ	3-1-62		SCALE	NONE								
CHECK	WH	3-1-62		DRAW	LEG 3-17-62								
APPRO				CHECK									

C

729901

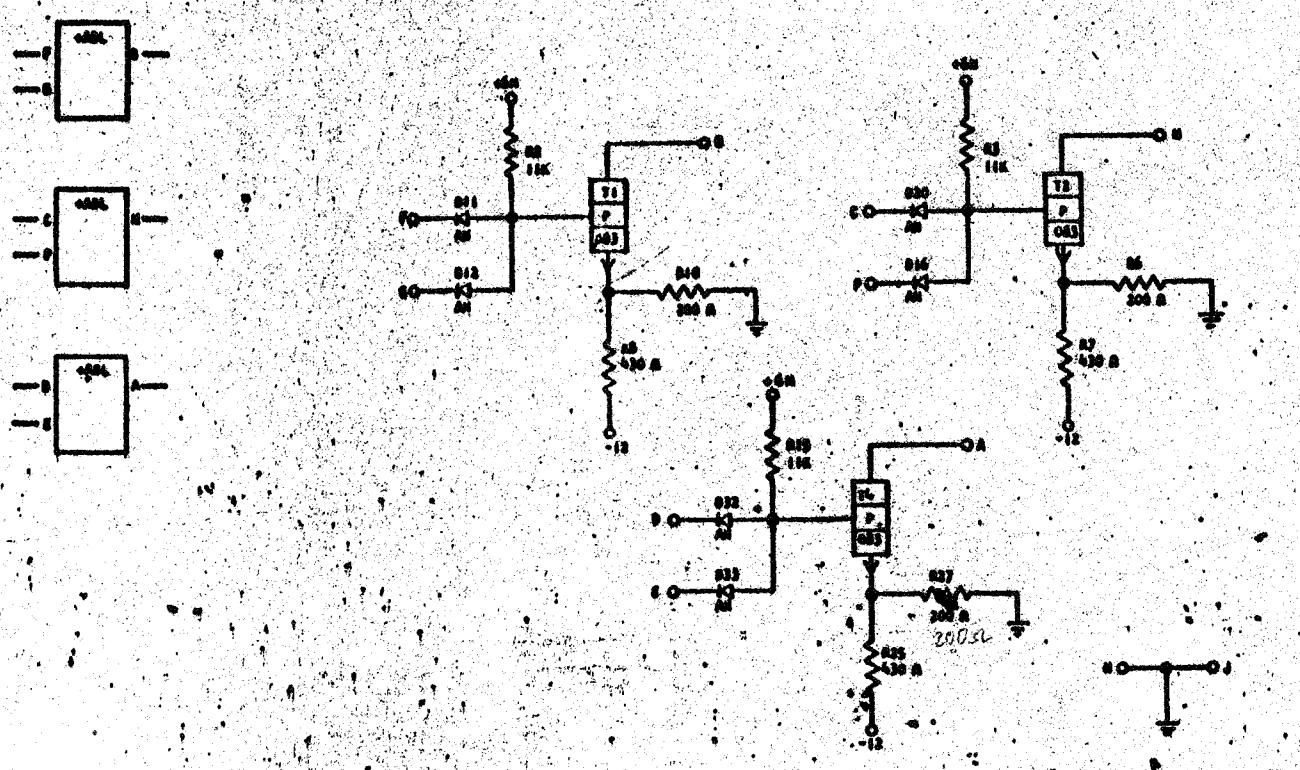
729901

6.5 XD

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370089

CTOL SIMPLEX INTERFACE DRIVER



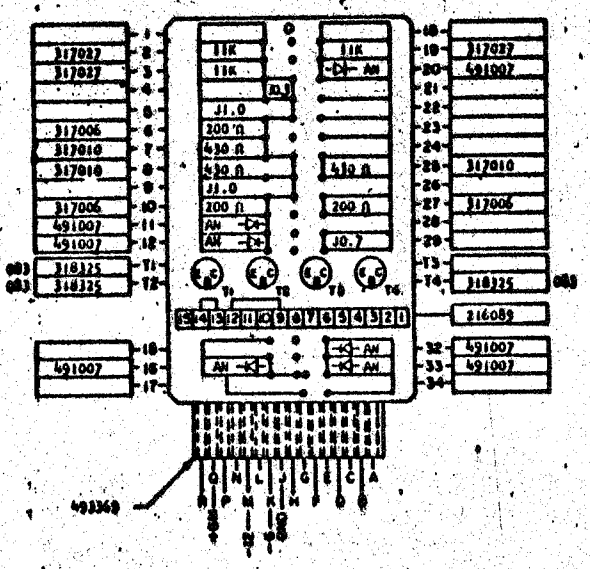
SEQUENCE OF OPERATION

1. ALL INPUTS UP TRANSISTORS ON OUTPUT DOWN
2. ANY INPUT DOWN TRANSISTOR OFF OUTPUT UP

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,C, B	U	INPUT		UP	-0.98	0.24
				DOWN	-7.44	-12.5
B,P, E	U	INPUT		UP	-0.98	0.24
				DOWN	-7.44	-12.5
B,Mo A	U	OUTPUT		UP		
				DOWN	-1.35	-2.66
H,J		GROUND		UP		
				DOWN		

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	455	652
TURN OFF	48	94



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
CARD ASM TSTR-CTOL SIMPLEX INTERFACE DRIVER	6-27-62	115599					729901
	1-3-63	EC 116034					
DESIGN	MODEL SMS	40-6-63	ST 83687				
DRAFT BG 1-1-63	SCALE NONE						
CHECK MM 1-1-63	DRAW LIG 1-17-63						
APPRD	CHECK						

C

729901

729902 STANDARDS CODE

CARD CODE A J T - 729902

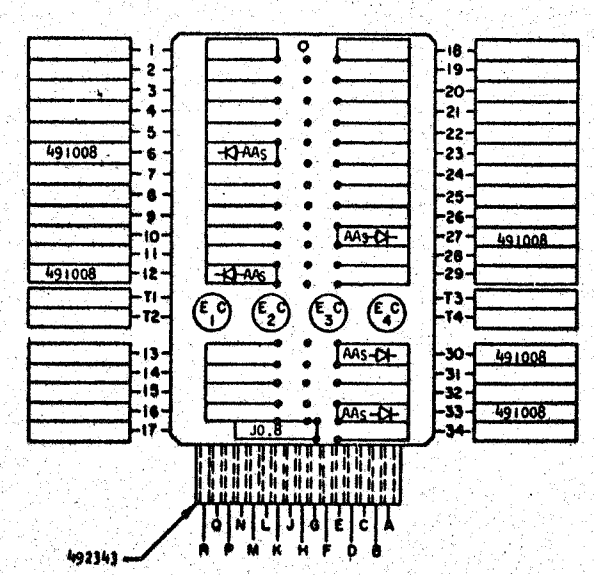
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370564

ALLOY-DIODES, TYPE AA_S

APPLICATION NOTES

THESE DIODES CAN BE USED AS INPUTS TO EITHER P OR N TYPE LOGIC BLOCKS DEPENDING ON HOW THE PINS ARE CONNECTED.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - ALLOY - DIODES, TYPE AAS					4-19-62	EC 115599					
					30.4.63	JT 83687					
DESIGN			MODEL	SMS							
DETAIL	RO	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

729902

729902

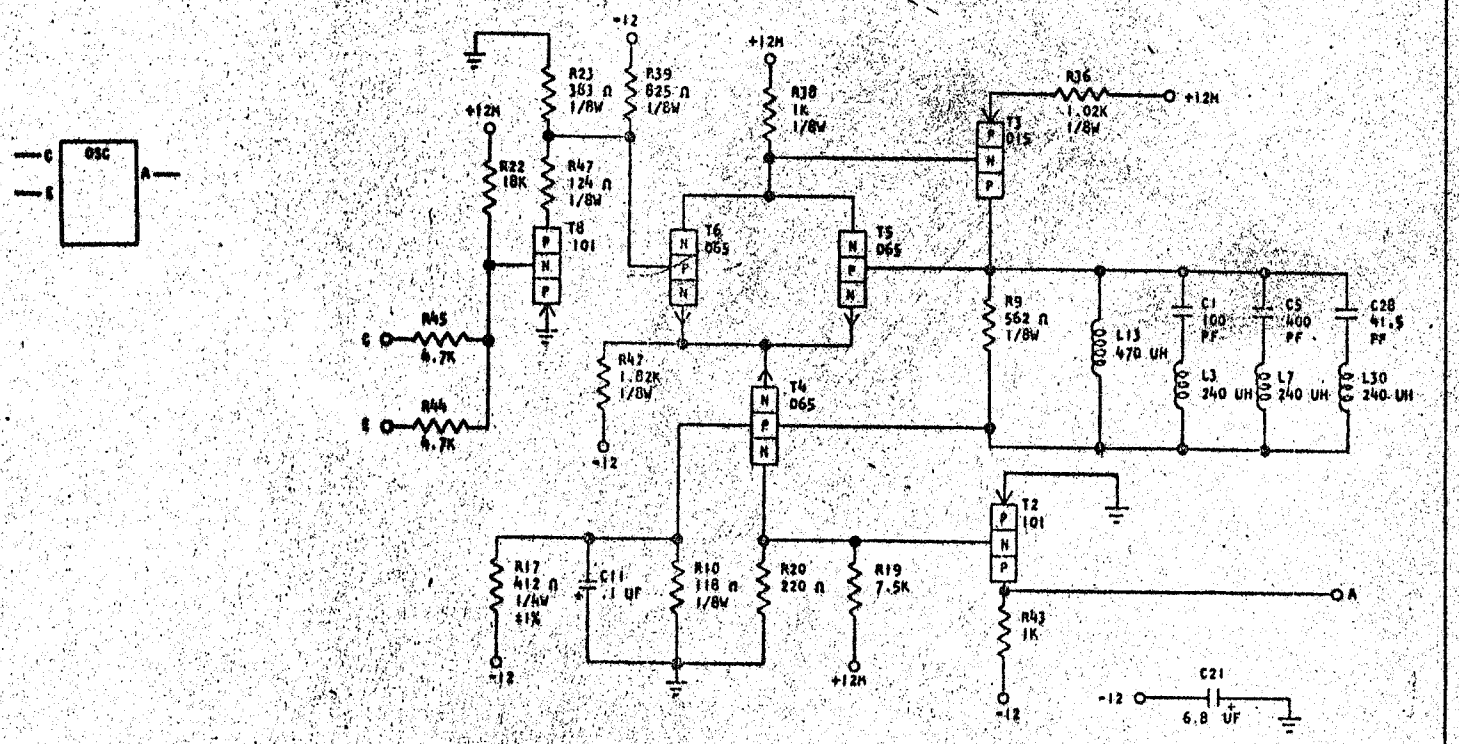
729903 STANDARD CORD

CARD CODE D A Z - 729903

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370127

DIFF BASE - OSCILLATOR, 240 KC S LINE GATED



SEQUENCE OF OPERATION

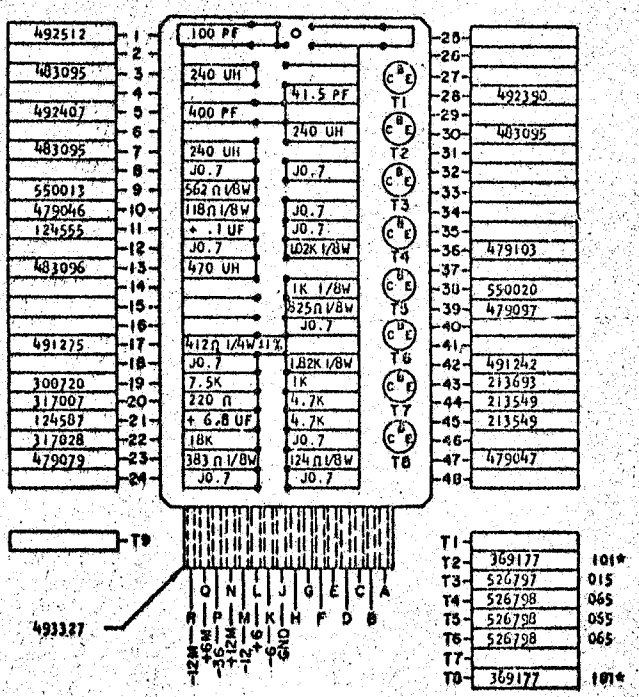
1. WHEN INPUTS CE ARE UP, T8 TURNS OFF OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C,E	S	INPUT		UP	-.45	+.05
				DOWN	-6.87	+12.5
A	S	OUTPUT	240 KC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	120
TURN OFF*	160	200

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-DIFF. BASE OSCILLATOR 240 KC S LINE GATED				4.29-62	EC 115599						729903
DESIGN			MODEL	SMS	30.4.63	JT 83607						
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRO			CHECK									

C

729903

729904

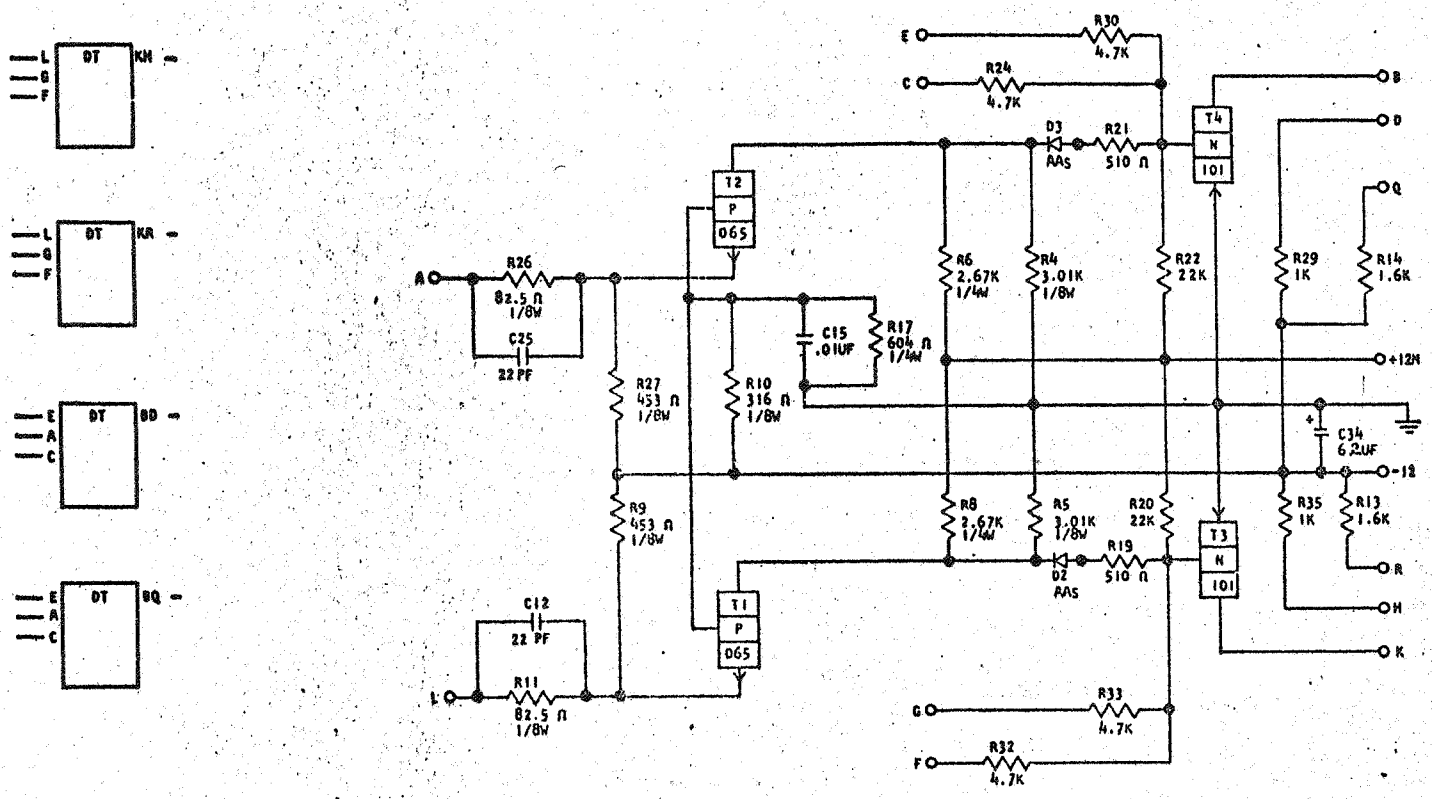
STANDARDS CODE

CARD CODE D B Z - 729904

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370385

CONVERTER-DIFFUSED BASE P-LINE TO SDTRL, OR SDTDL



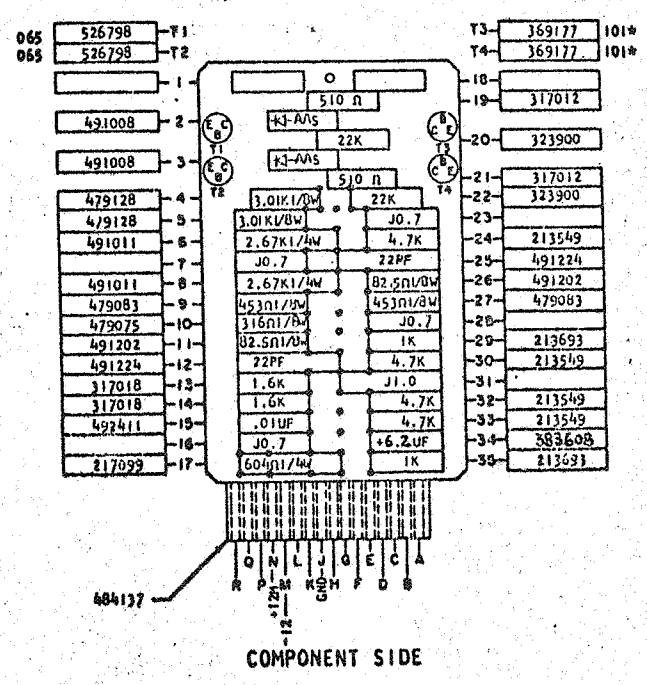
SEQUENCE OF OPERATION

INPUT A UP LEVEL, T2 CONDUCTS. THIS CAUSES T4 TO CONDUCT AND THE OUTPUT IS UP. EITHER PIN D OR Q IS TIED TO B DEPENDING IF SDTRL OR SDTDL BLOCKS ARE DRIVEN. THE OTHER CIRCUIT WITH INPUT L WORKS IN THE SAME MANNER. THE CIRCUIT ACCEPTS A P-LINE SIGNAL FROM THE COAXIAL LINE AND CONVERTS IT TO AN S LEVEL. THE GATES ACCOMPLISH A THREE WAY NOR FUNCTION; THAT IS, ANY NEGATIVE INPUT ON E, C OR OUTPUT OF T2 IN DOWN LEVEL WILL GIVE AN UP LEVEL OUTPUT FROM T4. IF THE 4.7K GATE IS NOT TO BE USED, IT MUST BE TIED TO GROUND.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
L,A	P	INPUT		UP	-5.6	5.2
				DOWN	-6.52	-6.4
E,C, F,G	S	GATE		UP	-.45	-.05
				DOWN	-6.07	-12.48
B,D, Q	S	OUTPUT		UP	-.45	-.05
				DOWN	-6.87	-12.48
R,H, K	S	OUTPUT		UP	-.45	-.05
				DOWN	-6.87	-12.48

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	50	80
TURN OFF	50	80



INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHARGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM ISTR-CONV-DIFF BASE S P-LINE TO SDTRL, OR SDTDL				4-27-62	EC 115599					
					30-4-63	JT83687					
DESIGN			MODEL								
DRAWN	RO	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIB 3-1-62							
APPRO			CHECK								

C

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

729904

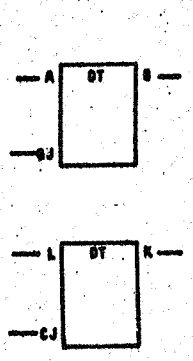
STANDARDS CODE	
729905	

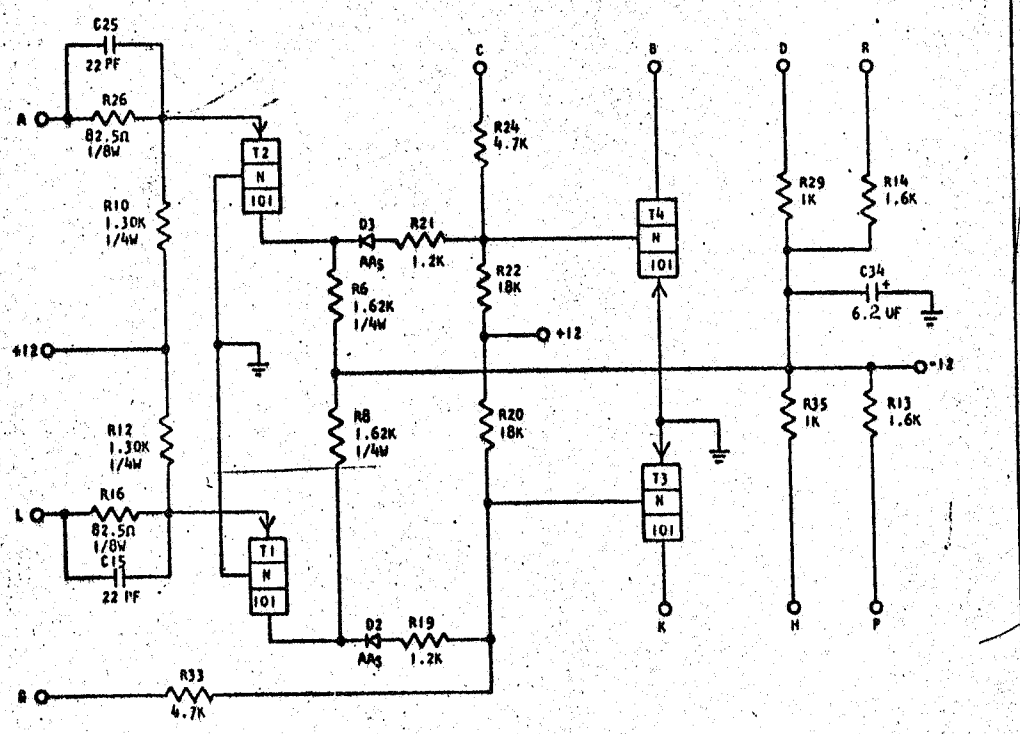
CARD CODE	729905
D C K -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370468

CONVERTER-DIFFUSED BASE N-LINE TO SDTRL OR SDTDL





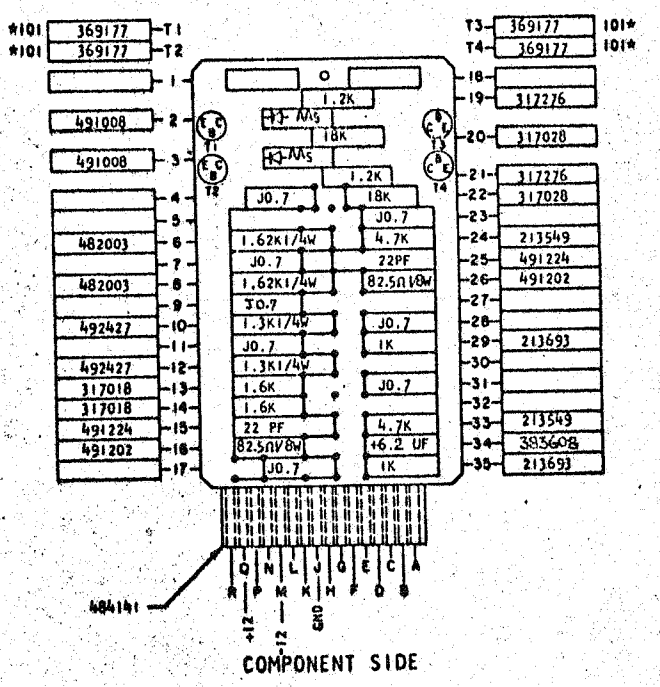
SEQUENCE OF OPERATION

1. WITH GATE INPUT UP OR TIED TO GROUND A DOWN INPUT AT A TURNS T2 OFF AND T4 ON AND GIVES AN UP OUTPUT
2. T4 AND T3 COLLECTORS MUST BE LOADED:
   1.6 K RESISTOR FOR SDTDL OUTPUT
   1 K RESISTOR FOR SDTRL OUTPUT
3. IF THE 4.7K RESISTOR (PIN C, G) IS NOT TO BE USED, IT MUST BE TIED TO GROUND.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,L	N	INPUT		UP	+0.4	+0.5
				DOWN	-0.4	-0.8
B,C	S	GATE INPUT		UP	-0.5	-.05
				DOWN	-6.9	-12.5
B,K	S	SDTDL OUTPUT		UP	-.65	-0.1
				DOWN	-5.81	-12.5
B,K	S	SDTRL OUTPUT		UP	-0.45	-0.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	50.0	72.0
TURN OFF	60.0	72.0



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- CONVERTER- DIFFUSED BASE N-LINE TO SDTDL OR SDTDL					6-27-62	EC 115599					
				MODEL	SMS	30-4-63	JT 83689					
DESIGN												
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LTG	3-17-62							
APPRO			CHECK									

C

729905

729906

STANDARDS CODE

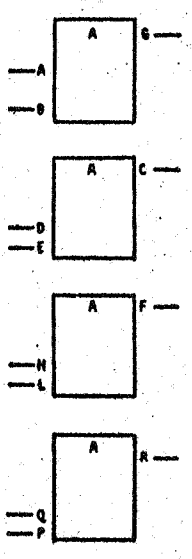
CARD CODE 729906

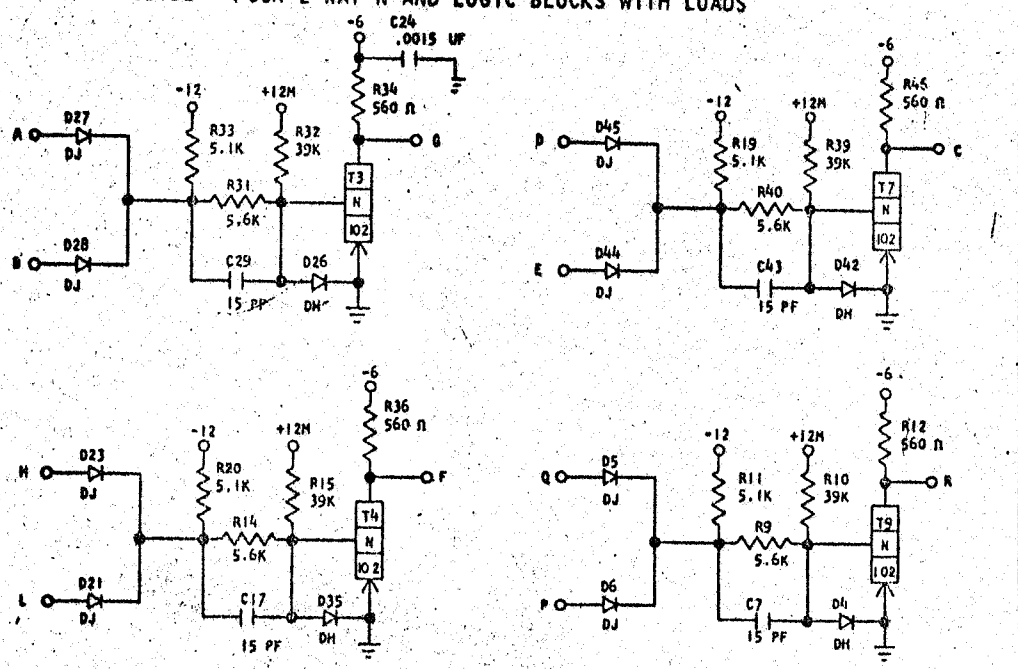
D E F -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370216

SDTDL - FOUR 2 WAY N AND LOGIC BLOCKS WITH LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,F, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8

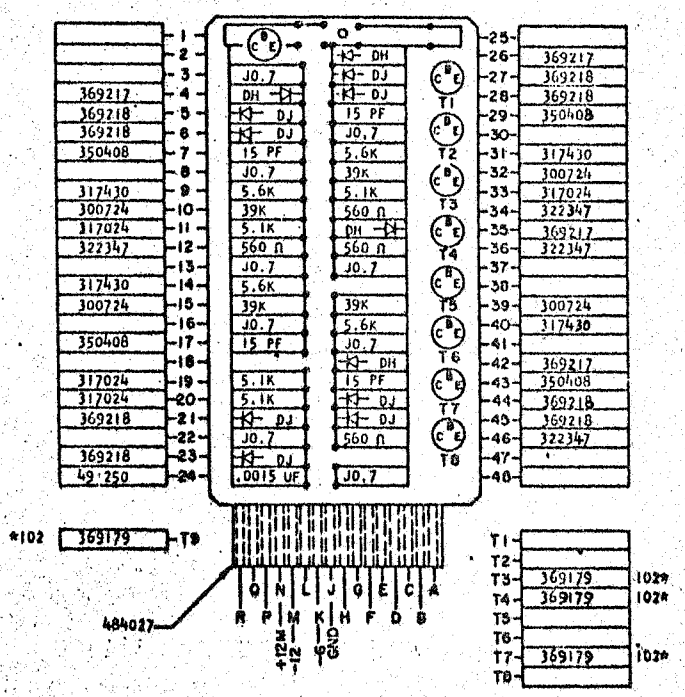
DELAY: SDTDL - HIGH SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	5	30*
TURN OFF (NSEC)	10	80**

*THIS DELAY CAN INCREASE TO 75 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 120 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM ISTR-SDTDL-FOUR 2-WAY N AND LOG BCKS WITH LOADS					6 1 62	EC 115599					
DESIGN				MODEL	SMS	30.4.63	JT 83687					
DETAIL	RO	3-1-62		SCALE	NONE							
CHECK	WH	3-1-62		DRAW	LIG 3-17-62							
APPRO				CHECK								

C

729906

729907

STANDARDS CODE

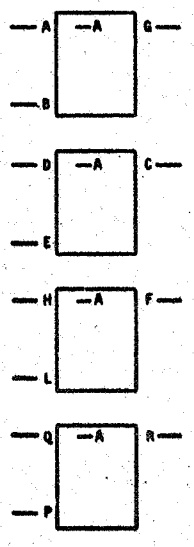
CARD CODE 729907

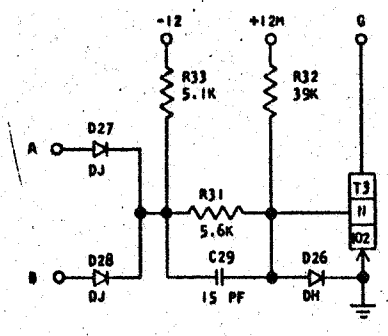
D E G *

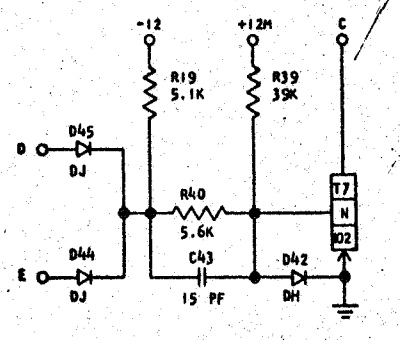
REFERENCE DRAWING

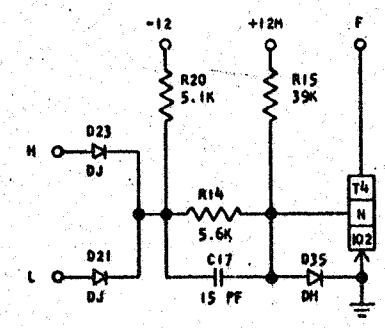
SEE PRODUCTION DRAWING 370217

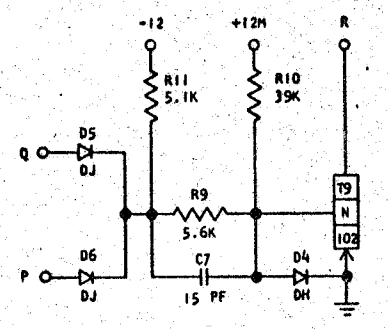
SDTDL FOUR 2-WAY N AND LOGIC BLOCKS WITHOUT LOADS











SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8

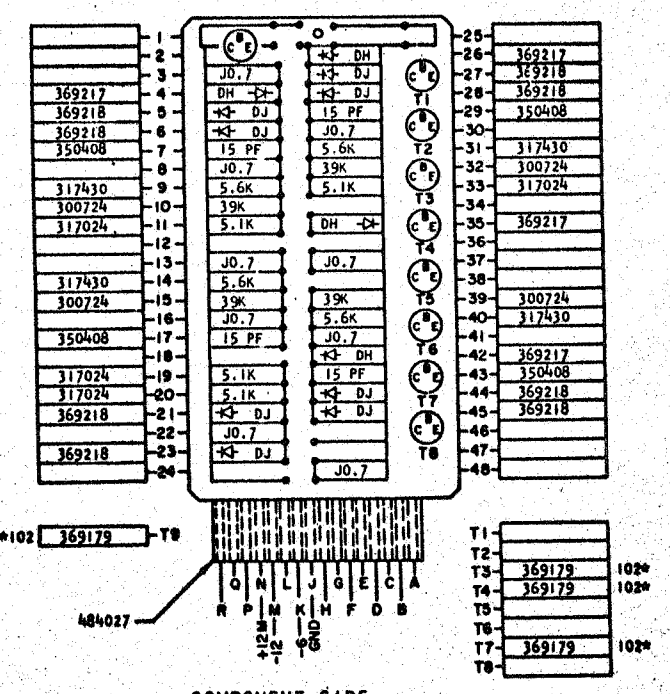
DELAY; SDTDL - HIGH SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	5	30*
TURN OFF (NSEC)	10	80**

*THIS DELAY CAN INCREASE TO 75 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 120 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARDS	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 4 2-WAY				6-29-62	EC 115599					
	N AND LOGIC BLOCKS WITHOUT LOADS				30-4-63	TT 83687					
DESIGN			MODEL	SMS							
DETAIL	RO	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

729907

729907

729908

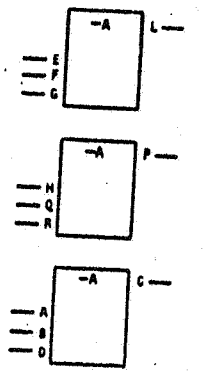
REDRAWN

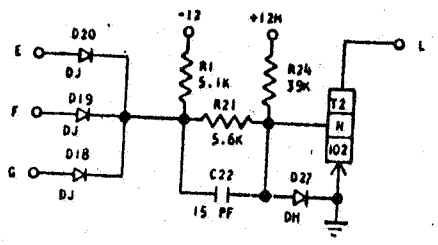
CARD CODE 729908 D E J -

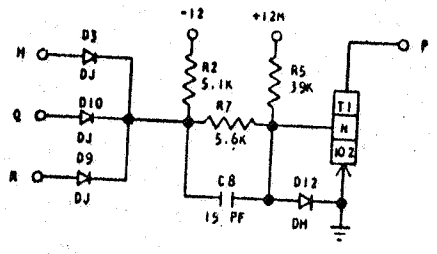
REFERENCE DRAWING

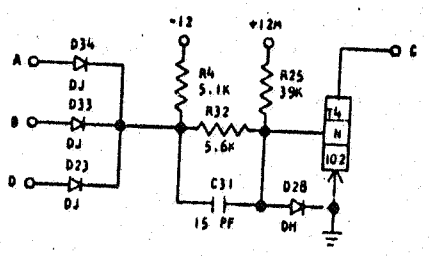
SEE PRODUCTION DRAWING 370219

SDTDL THREE 3-WAY N AND LOGIC BLOCKS WITHOUT LOADS









SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E, H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F, Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G, R, D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L, P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8

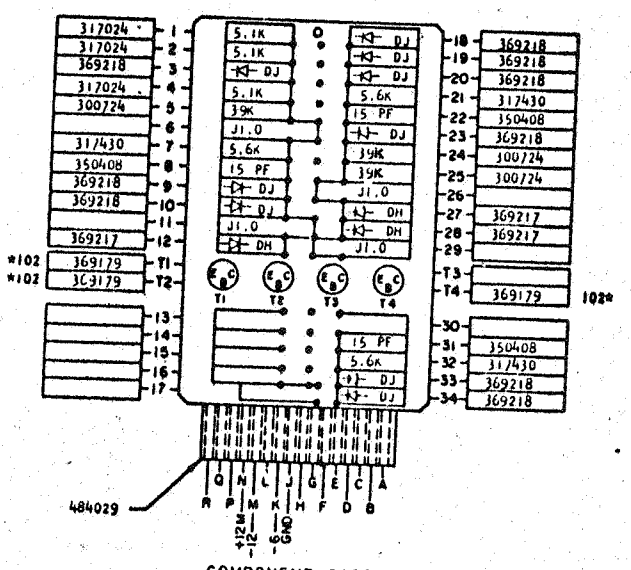
DELAY: SDTDL - HIGH SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	5	30*
TURN OFF (NSEC)	10	80**

*THIS DELAY CAN INCREASE TO 75 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 120 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL THREE 3-WAY N AND LOG BCKS WITHOUT LDS				6-27-62	115599					
DESIGN			MODEL	SMS	12-22-62	EC 114838					
DETAIL	RQ	3-1-62	SCALE	NONE	30-4-63	JT 83687					
CHECK	WH	3-1-62	DRAW	LIG 3-1-62							
APPRO			CHECK								

729908

C

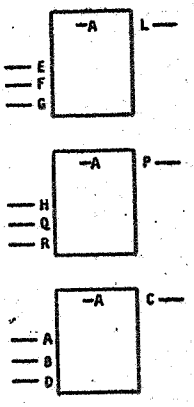
STANDARDS CODE 729908

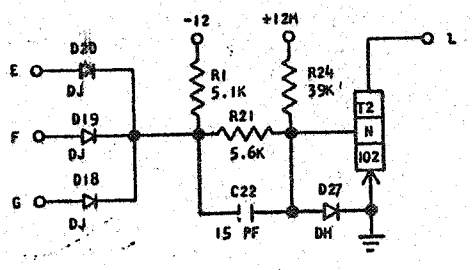
CARD CODE DEJ- 729908

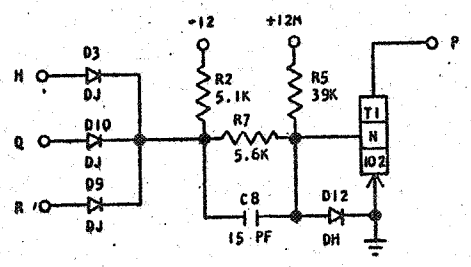
REFERENCE DRAWING

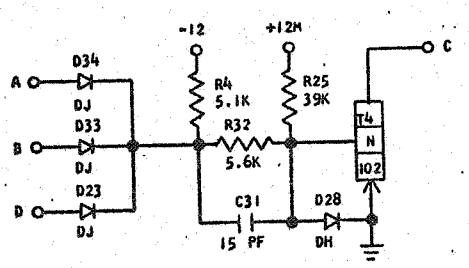
SEE PRODUCTION DRAWING 370219

SDTDL THREE 3-WAY N AND LOGIC BLOCKS WITHOUT LOADS









SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E, H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F, Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G, R, D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L, P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8

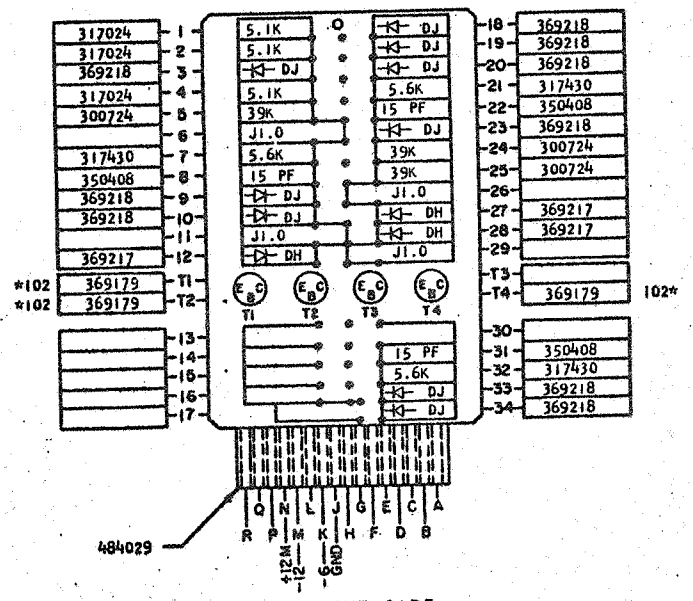
DELAY: SDTDL = HIGH SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	5	30*
TURN OFF (NSEC)	10	80**

*THIS DELAY CAN INCREASE TO 75 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 120 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL THREE 3-WAY N AND LOG BCKS WITHOUT LDS					4-27-62	115599					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729908

C

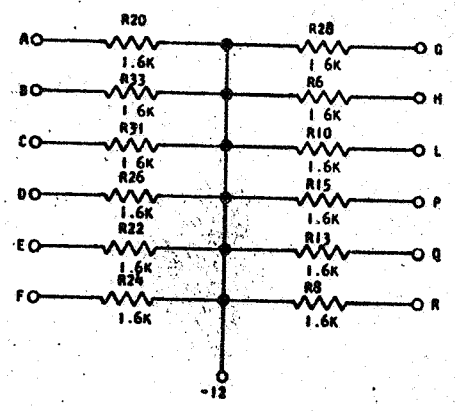
729909 STANDARDS CODE

CARD CODE 729909
D F J -

REFERENCE DRAWING

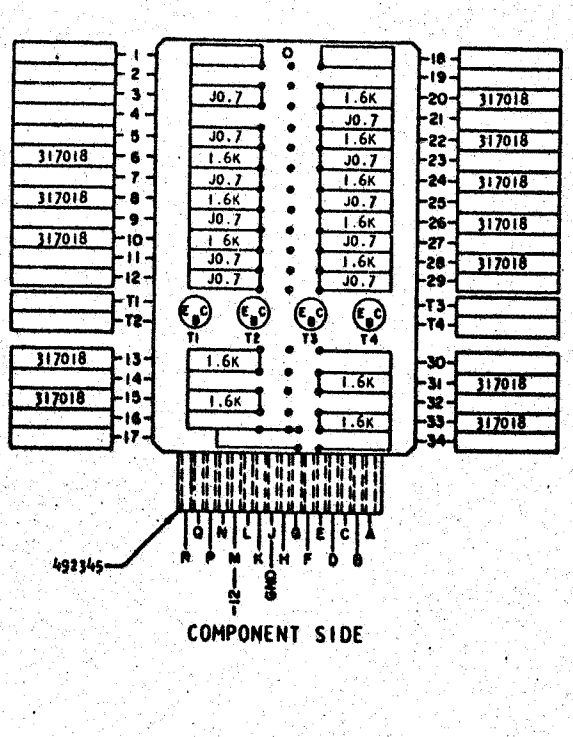
SEE PRODUCTION DRAWING 370232

TDL & TRL LOAD CARD



APPLICATION

1. USED FOR TDL AND TRL COLLECTOR LOADING
2. MAY BE USED IN PARALLEL IN CERTAIN APPLICATIONS.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-TDL AND TRL LOAD CARD					4-19-62	EC 115599					
DESIGN			MODEL	SMS		30-6-63	TT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729909

C

CODE 729909

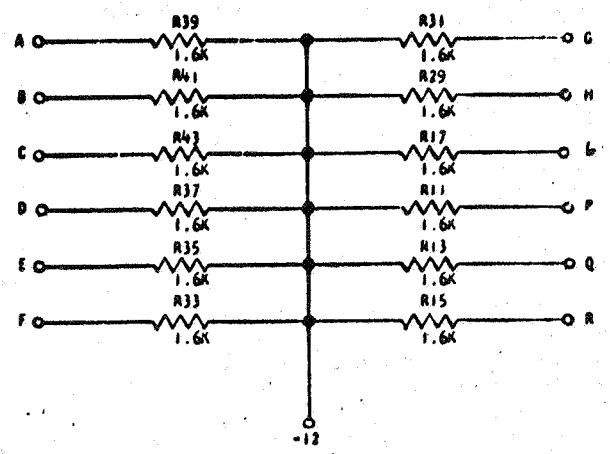
729909

D I J -

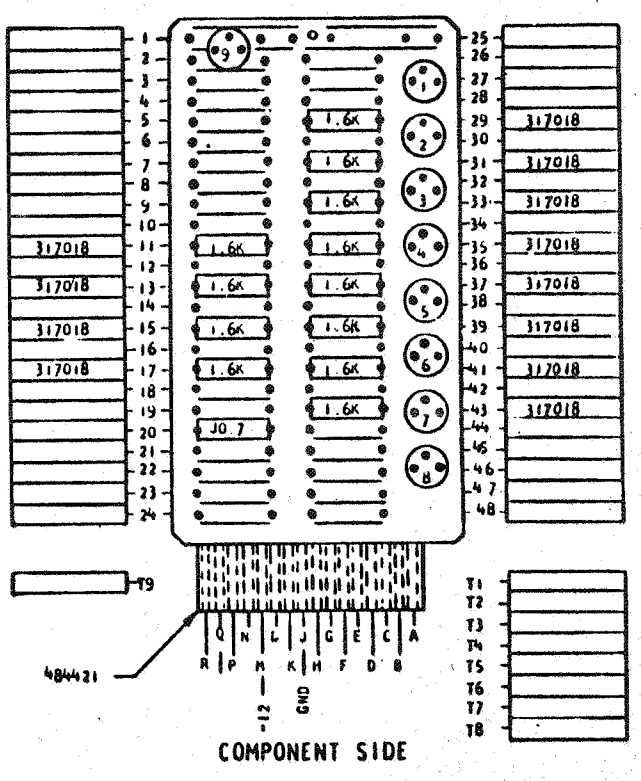
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370232

TDL & TRL LOAD CARD



APPLICATION
1. USED FOR TDL AND TRL COLLECTOR LOADING
2. MAY BE USED IN PARALLEL IN CERTAIN APPLICATIONS



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-TDL AND TRL LOAD CARD				
DESIGN			MODEL	SLS 8018	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	JRP	7-11-63
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO
6-29-62	115599					
7-30-63	117824					

729903

729909

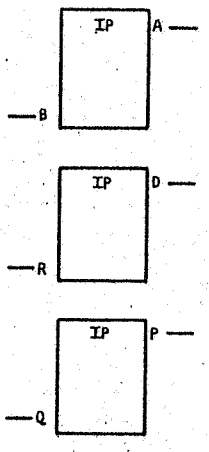
STANDARDS CODE 729910

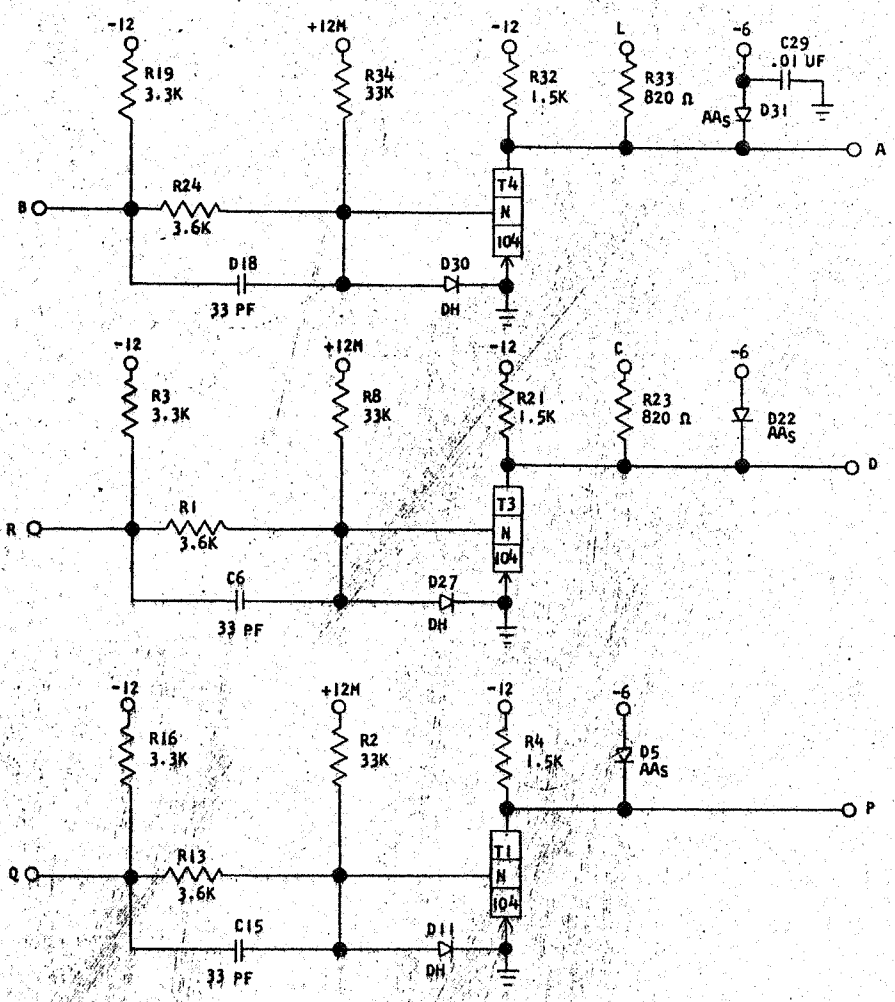
CARD CODE 729910
D F Q -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370225

SDTDL INVERTING POWER DRIVER





SEQUENCE OF OPERATION

1. INPUT DOWN, TRANSISTOR ON, OUTPUT UP
2. INPUT UP, TRANSISTOR OFF, OUTPUT DOWN
3. 820Ω COLLECTOR RESISTOR RETURNED TO -12 VOLTS WHEN DRIVING NEGATIVE "OR" INPUTS OF DOUBLE LEVEL LOGIC BLOCKS & WHEN DRIVING TRIGGER AC INPUTS

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
B,R, Q	Y	INPUT		UP	-0.65	-0.10
				DOWN	-7.14	-5.84
A,D, P	Y	OUTPUT		UP	-0.65	-0.10
				DOWN	-6.06	-6.8

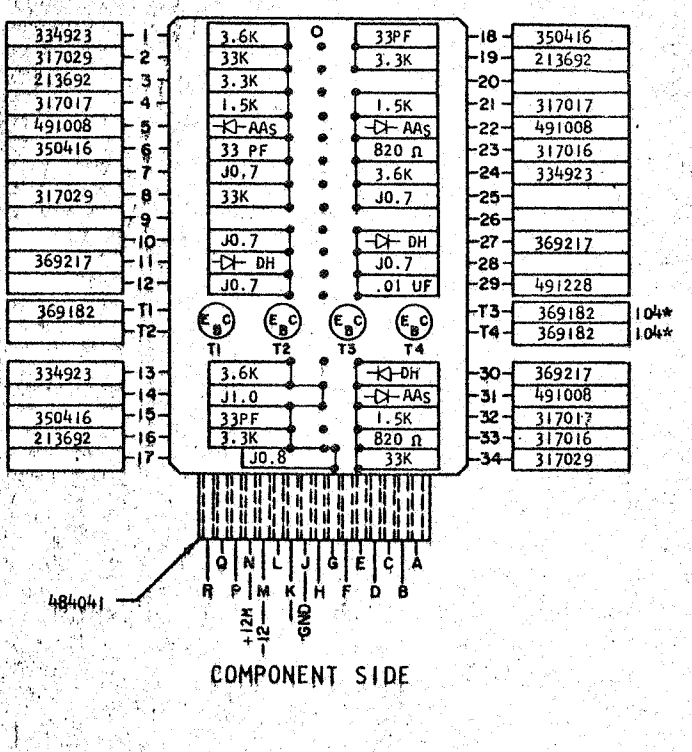
DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	10.0**	50.0*
TURN OFF	14.0**	35.0*

*ASSUMES LOAD OF 10 LOGIC BLOCKS AND TR INPUT OF 70 NSEC AND INPUT TF OF 135 NSEC.
**ASSUMES LOAD OF 4 LOGIC BLOCKS AND INPUT TR OF 35 NSEC AND INPUT TF OF 70 NSEC.

RISE TIME	16.0	70.0# TO 110.0##
FALL TIME	75.0	125.0## TO 190.0#

#OCCURS WHEN DRIVING TRIGGERS
##OCCURS WHEN DRIVING LOGIC BLOCKS



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL INVERTING POWER DRIVER				6-29-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729910

C

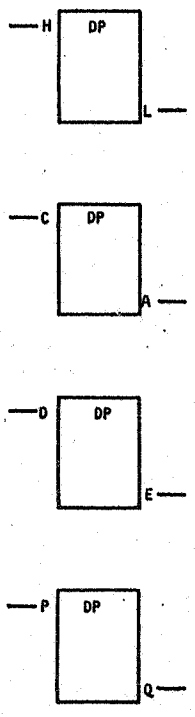
STANDARDS CODE	729911

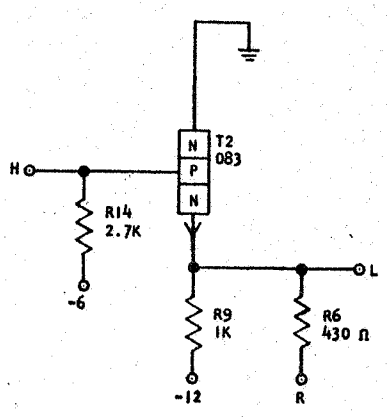
CARD CODE	729911
D F R -	

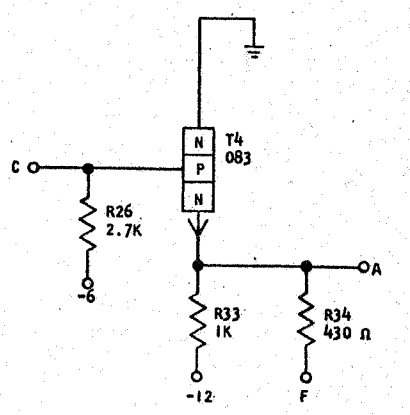
REFERENCE DRAWING

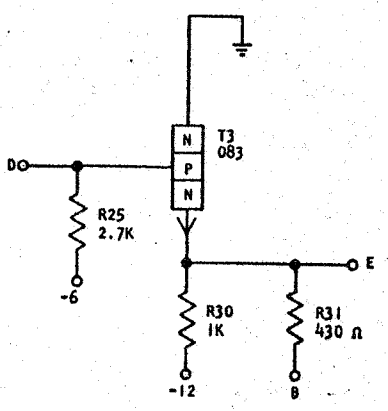
SEE PRODUCTION DRAWING 370226

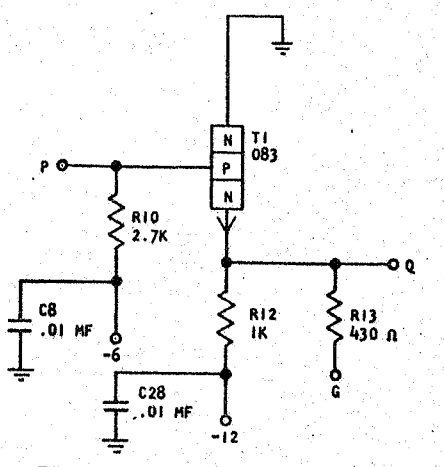
SDTDL NON-INVERTING POWER DRIVER











SEQUENCE OF OPERATION

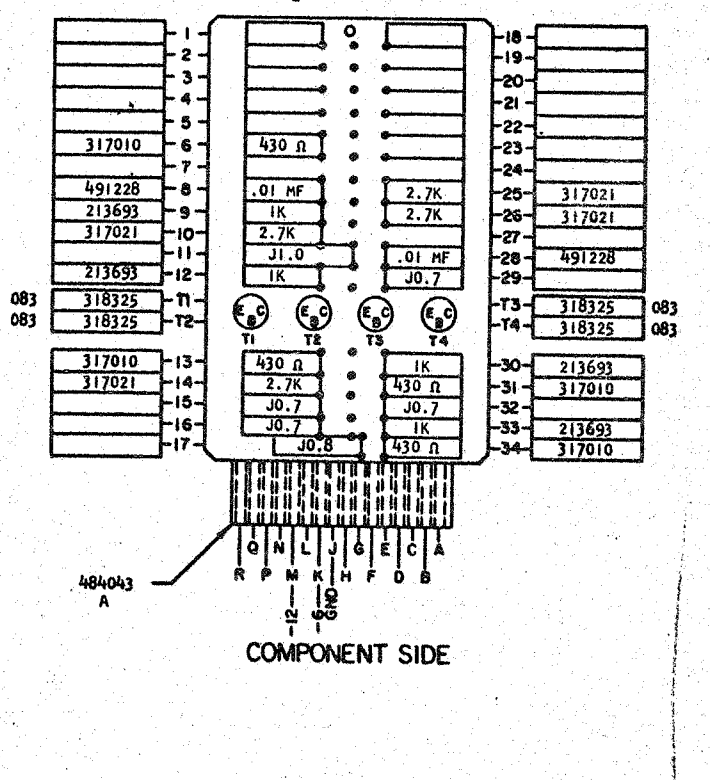
1. OUTPUT WILL FOLLOW INPUT
2. PINS R, F, B, AND G MAY BE CONNECTED TO PIN M (-12) FOR CERTAIN APPLICATIONS.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,C, D,P	Y	INPUT		UP	≤0.65	-0.10
				DOWN	-5.81	-8.8
L,A, E,Q	Y	OUTPUT		UP	-1.10	-0.22
				DOWN	-7.30	-5.83

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	6.0	20.0
TURN OFF	6.0	28.0

OUTPUT RISE AND FALL TIMES ARE WITHIN ±10 NSEC'S OF THE INPUT RISE AND FALL TIMES, RESPECTIVELY.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-SDTDL NON-INVERTING POWER DRIVER					6-19-62	115599						729911
DESIGN			MODEL	SMS									
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRO			CHECK										

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STANDARD CODE 729911

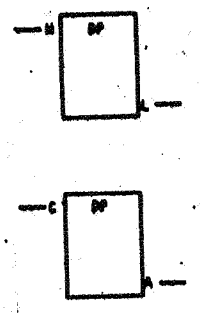
729911

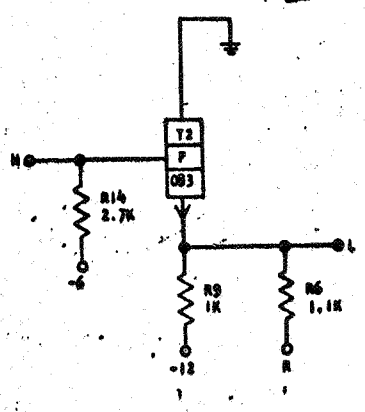
DFR -

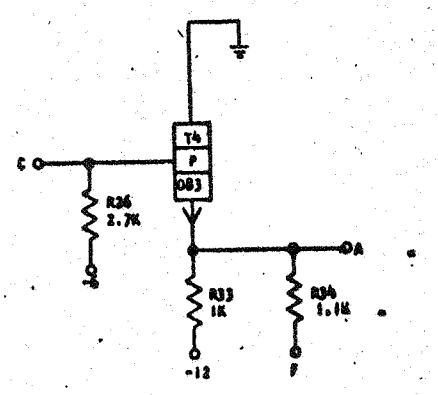
REFERENCE DRAWING

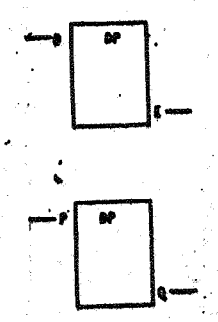
SEE PRODUCTION DRAWING 370226

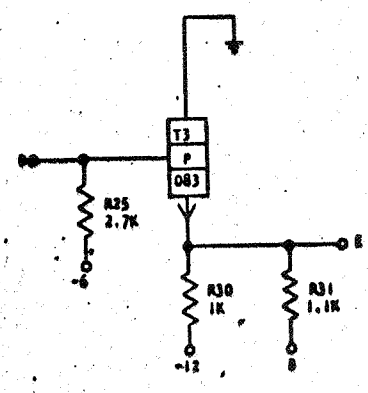
SDTDL NON-INVERTING POWER DRIVER

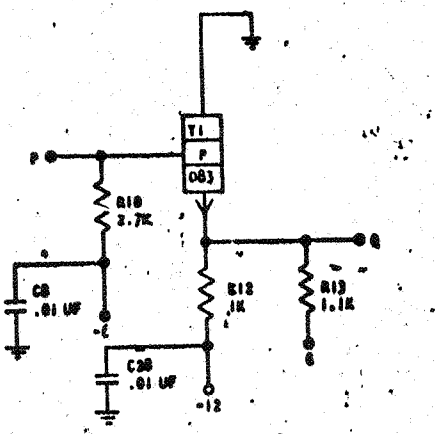












SEQUENCE OF OPERATION

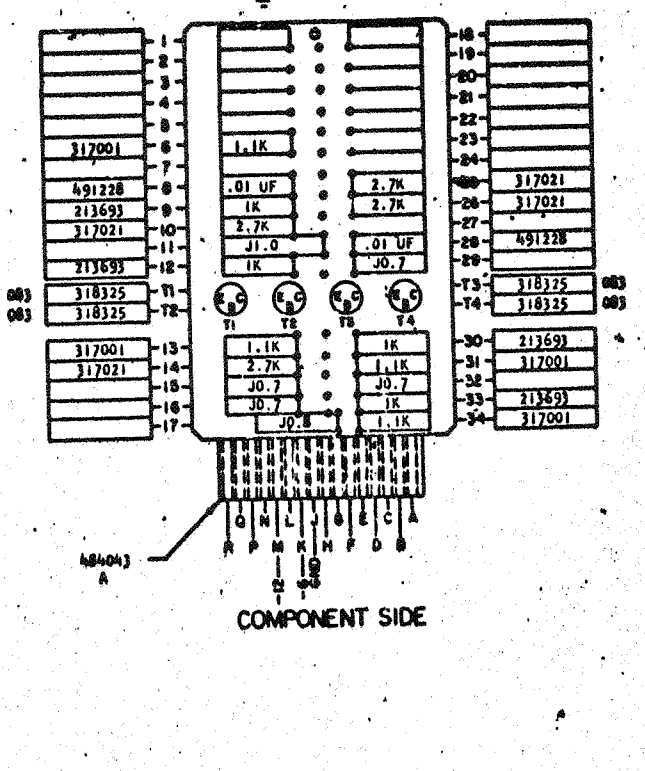
1. OUTPUT WILL FOLLOW INPUT
2. PINS R, F, S, AND B MAY BE CONNECTED TO PIN M (-12) FOR CERTAIN APPLICATIONS.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
M,C, D,P	V	INPUT		UP	-0.65	-0.10
				DOWN	-5.81	-8.8
L,A, E,Q	V	OUTPUT		UP	-1.10	-0.22
				DOWN	-7.30	-5.83

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	6.0	20.0
TURN OFF	6.0	28.0

OUTPUT RISE AND FALL TIMES ARE WITHIN ±10 NSEC'S OF THE INPUT RISE AND FALL TIMES, RESPECTIVELY.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARDS

APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL				6-19-62	115599					
	NON-INVERTING POWER DRIVER				1-3-63	EC 116034					
DESIGN			MODEL	SMS	30.4.63	JT 83687					
DETAIL	RG	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-63							
APPRO			CHECK								

729911 1

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729911

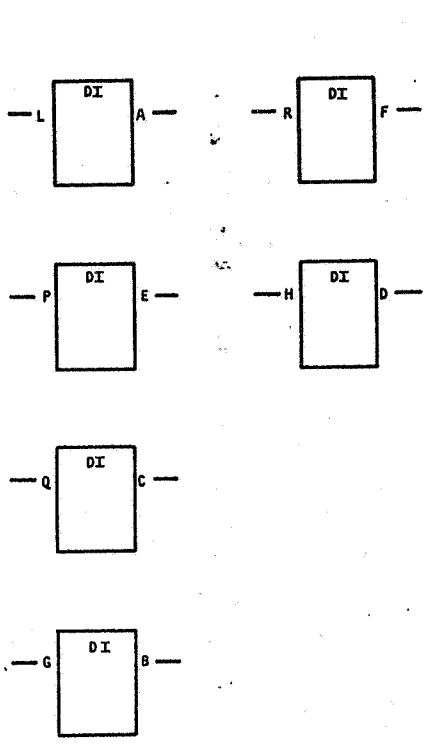
STANDARDS CODE	729912

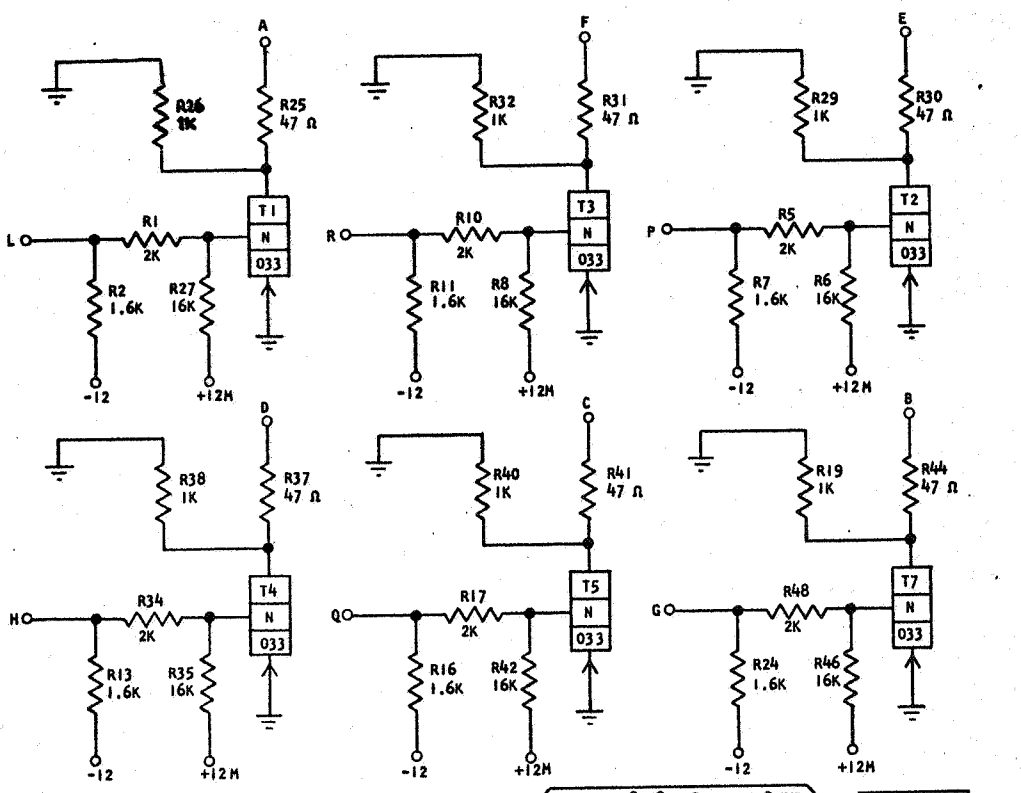
CARD CODE	729912
D G S -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370347

SDTDL INDICATOR DRIVER

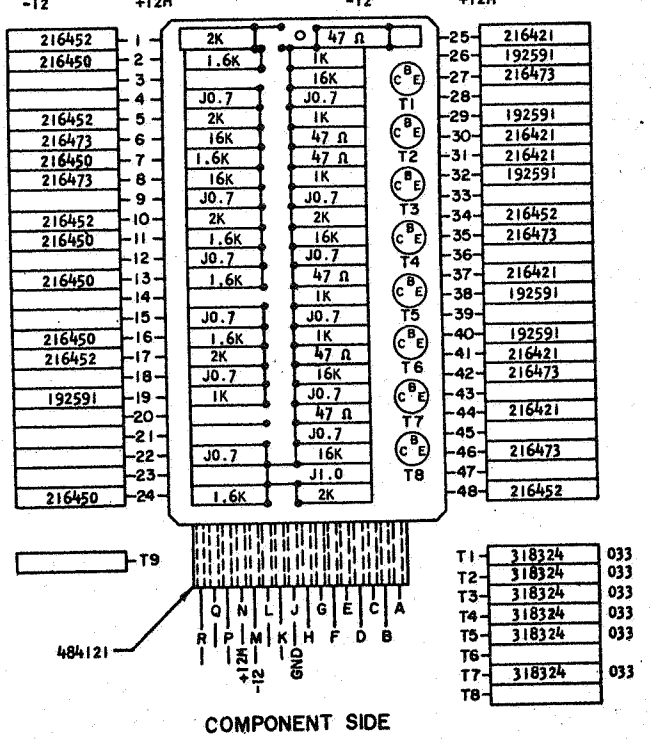




SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
L,R,P, H,Q,G	Y	INPUT		UP	-0.65	0.10
				DOWN	-5.81	-7.64
A,F,E, D,C,B	S	OUTPUT		UP	-1.67	
				DOWN	-9.62	



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SDTDL INDICATOR DRIVER					4-4-62	115599					729912
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

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729912

STANDARDS CODE

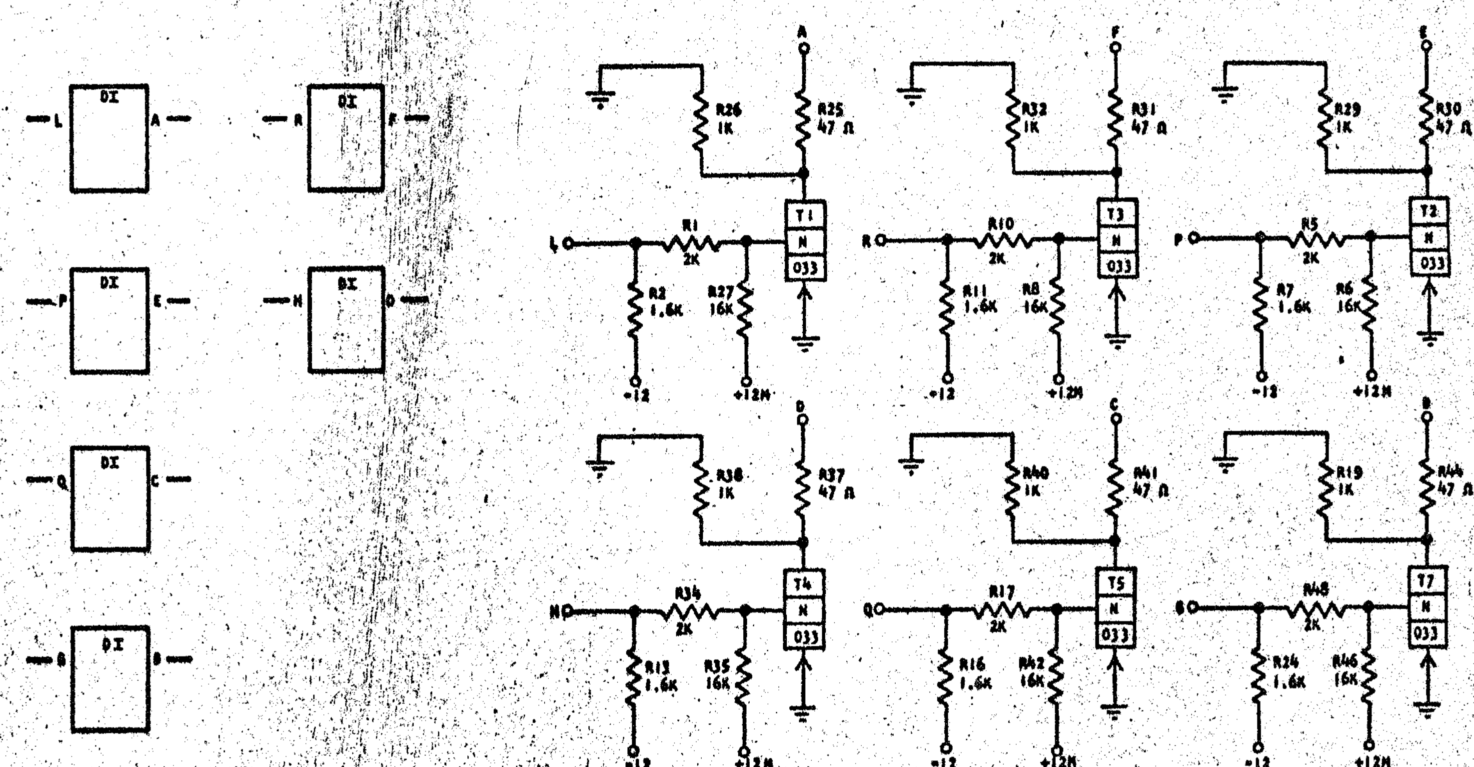
CARD CODE 729912

D G S -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370347

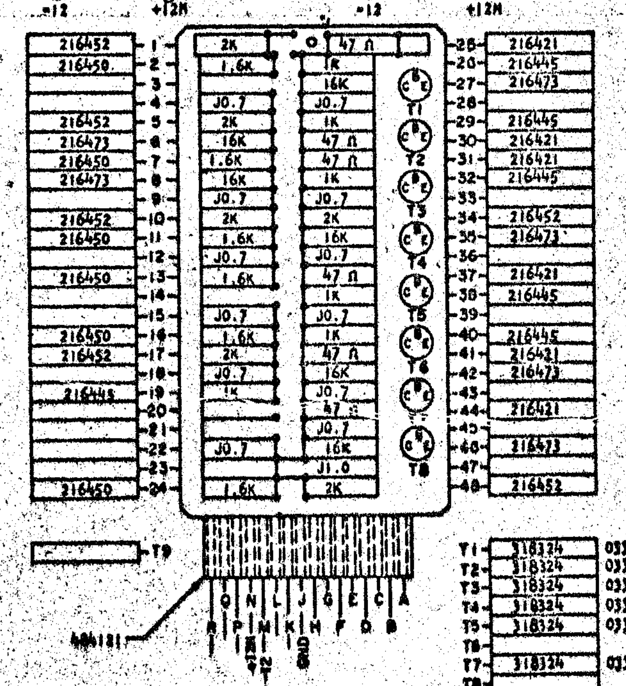
SDTDL INDICATOR DRIVER



SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
L, R, P, H, Q, G	Y	INPUT		UP	-0.65	0.10
				DOWN	-5.81	-7.64
A, F, E, D, C, B	S	OUTPUT		UP	-1.67	
				DOWN	-9.62	



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SDTDL					6-11-62	115599					
	INDICATOR DRIVER					3-1-63	EC 116026					
DESIGN		#	MODEL	SMS		30.4.63	JT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	L1G	3-17-62							
APPRO			CHECK									

729912

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729912

729913 STANDARDS CODE

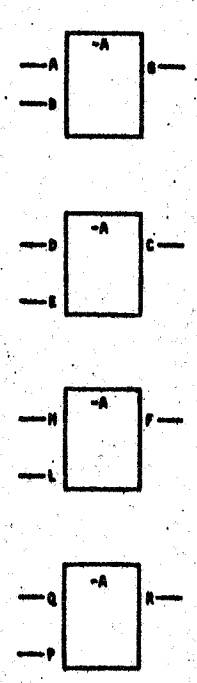
CARD CODE 729913

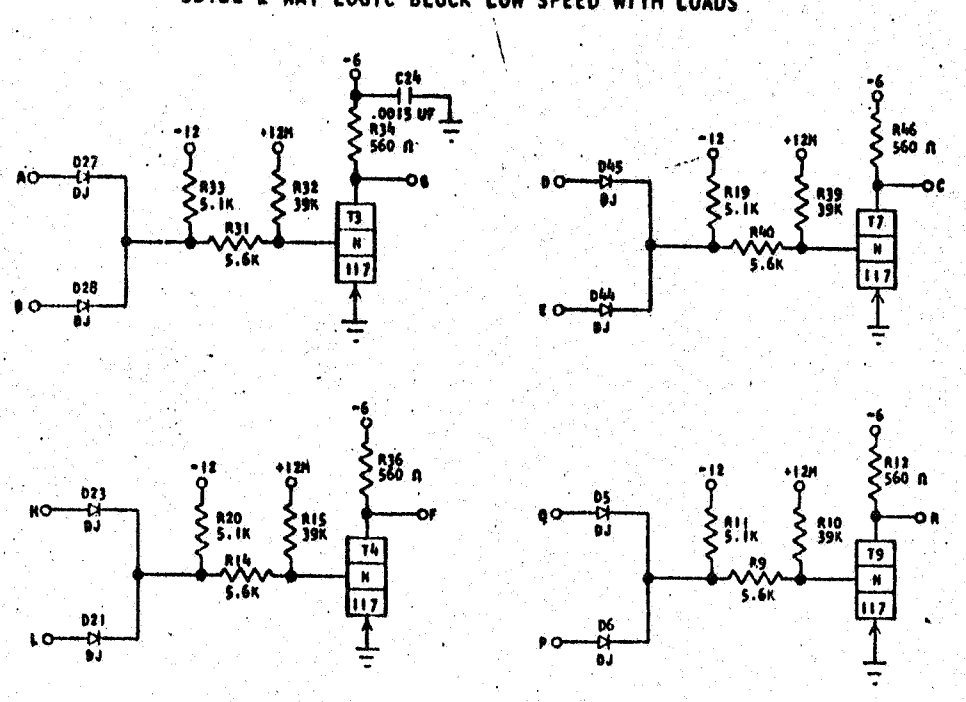
D G T -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370380

SDTDL-2 WAY LOGIC BLOCK LOW SPEED WITH LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

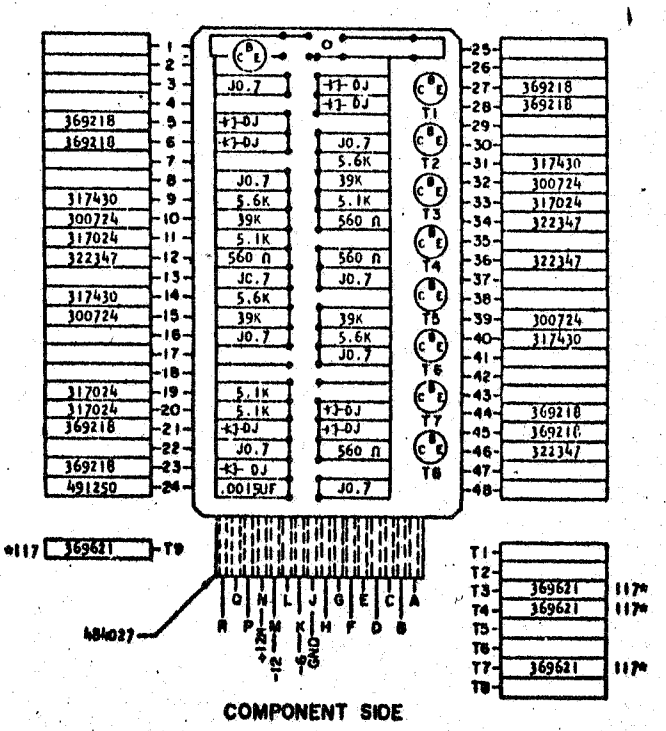
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL-2-WAY				6-29-62	EC 115599					729913
	LOGIC BLOCK LOW SPEED WITH LOADS				30.4.62	JT 83687					
DESIGN			MODEL	SMS							
DETAIL	RG	3-1-62	SCALE	NONE							
CHECK	WM	3-1-62	DRAW	LIG	3-17-62						
APPRO			CHECK								

729913

C

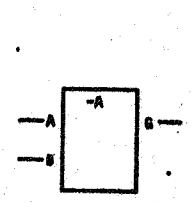
729914 | STANDARDS CODE

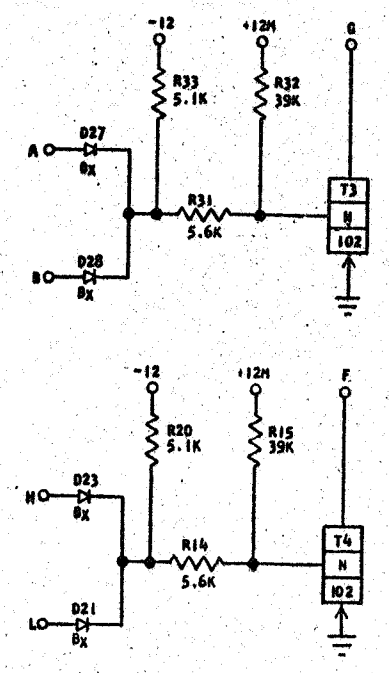
CARD CODE | 729914
D G U -

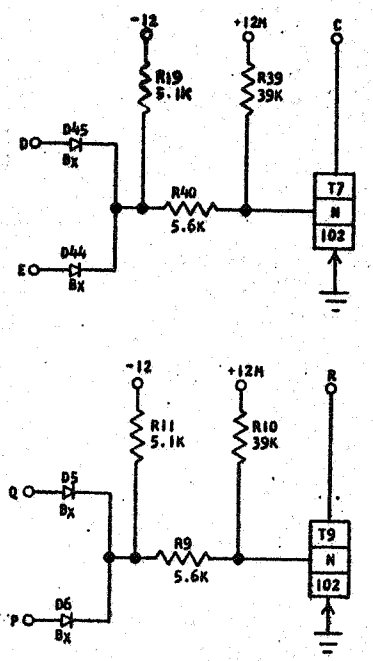
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370379

SDTDL 2-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS







SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT DOWN TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

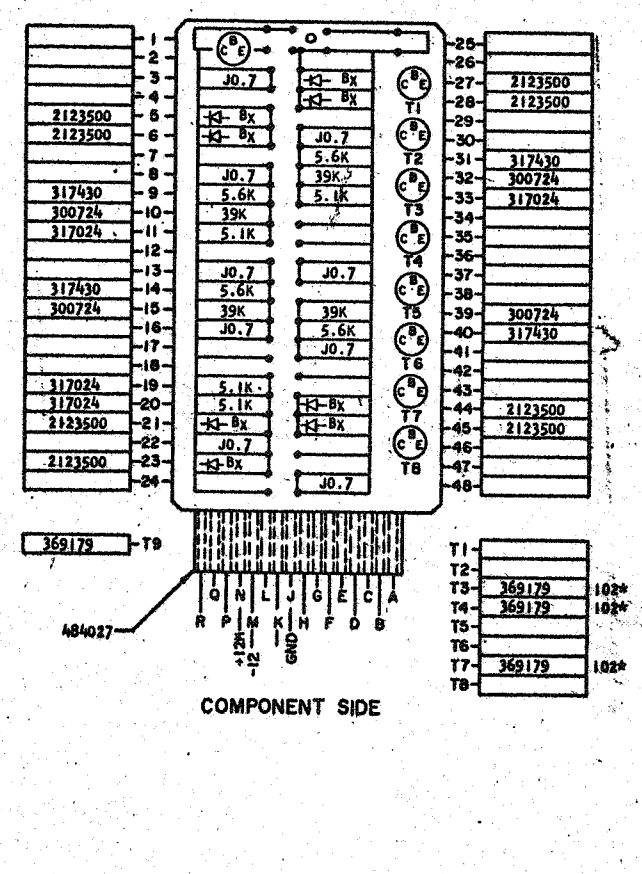
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-SDTDL 2-WAY LOGIC BCK LOW SPEED WITHOUT LOADS				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6 -y -62	115599					

729914

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729914
23741

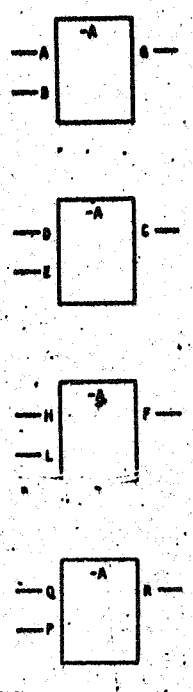
STANDARDS CODE	729914

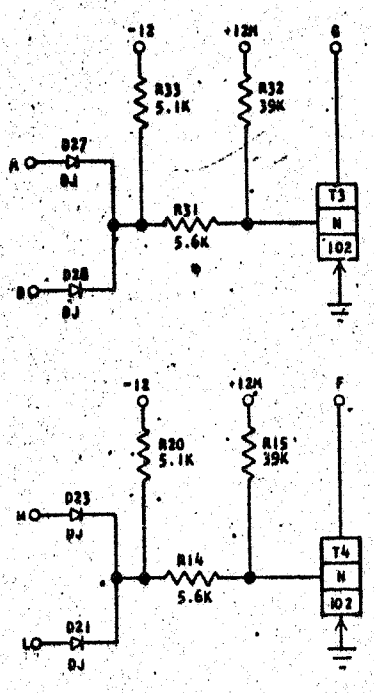
CARD CODE	729914
D G U -	

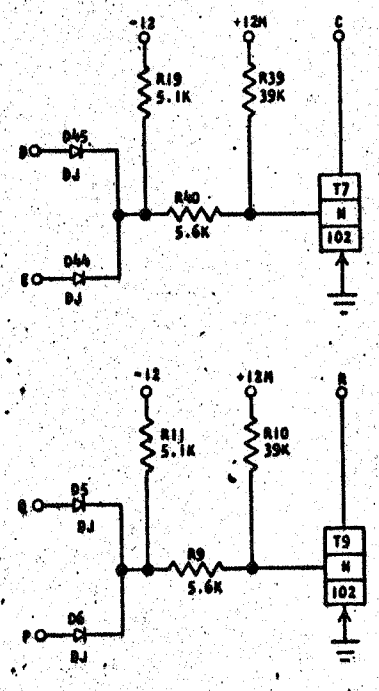
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370379

SDTDL 2-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS







SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT DOWN TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

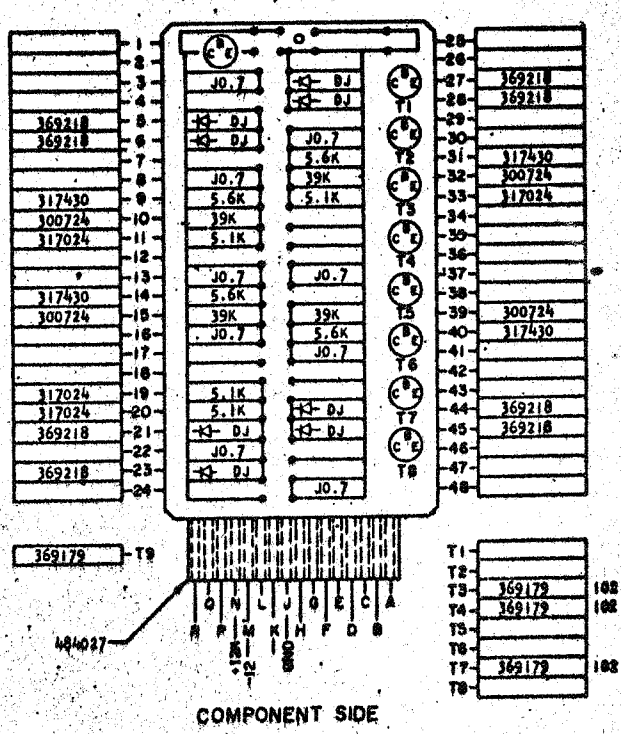
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40.	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 2-WAY LOGIC BCK LOW SPEED WITHOUT LOADS					4-29-63	115599					
DESIGN			MODEL	SMS		1-3-63	EC 116034					
DETAIL	RO	3-1-62	SCALE	NONE		30-4-63	TT 89687					
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729914

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729915 STANDARDS CODE

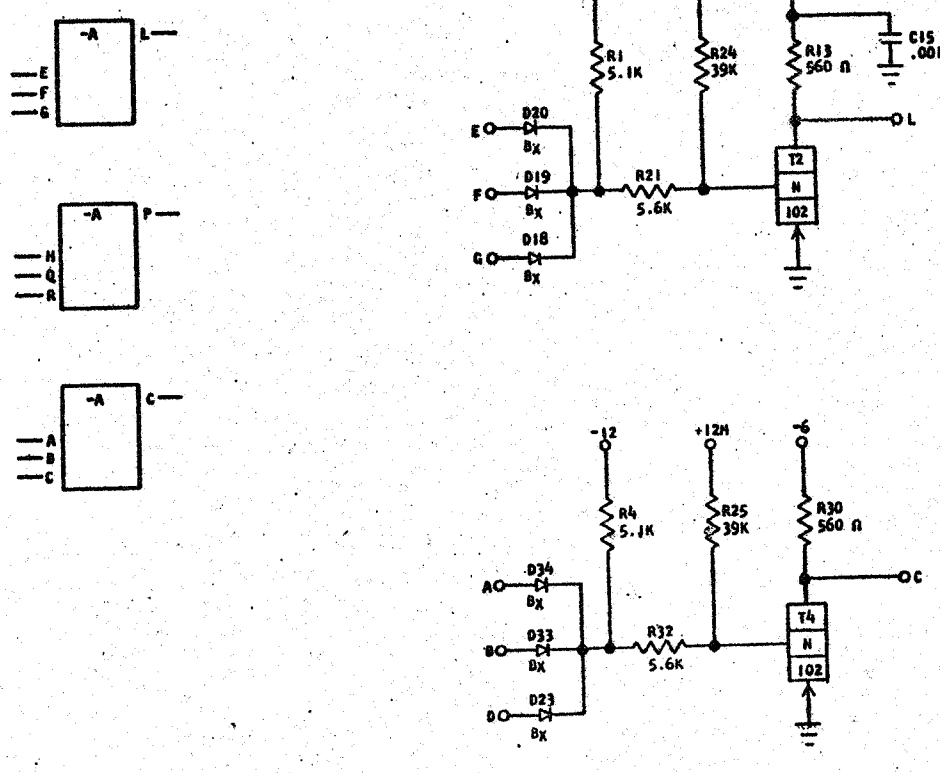
CARD CODE 729915

D G V K

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370378

SDTDL - 3-WAY LOGIC BLOCK LOW SPEED WITH LOADS



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F,Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,R, D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L,P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

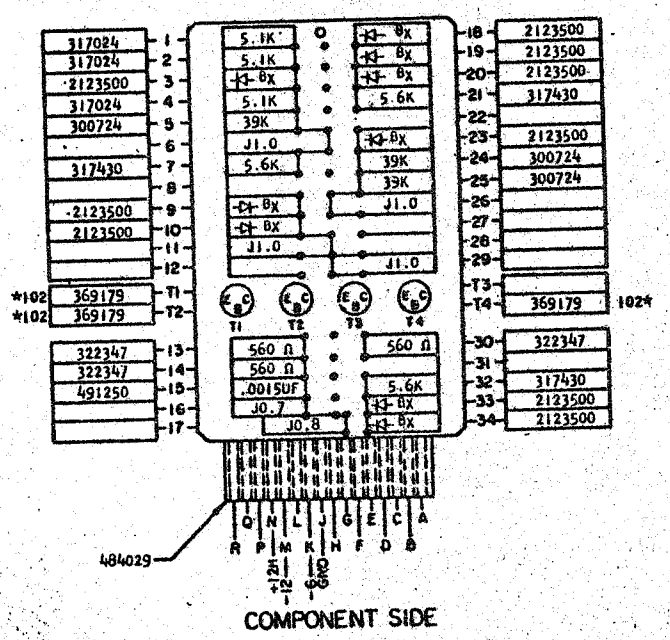
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729915
NAME	CARD ASM TSTR-SDTDL-3-WAY LOGIC BLOCK LOW SPEED WITH LOADS				6-29-62	115599						
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRO			CHECK									

C

729915

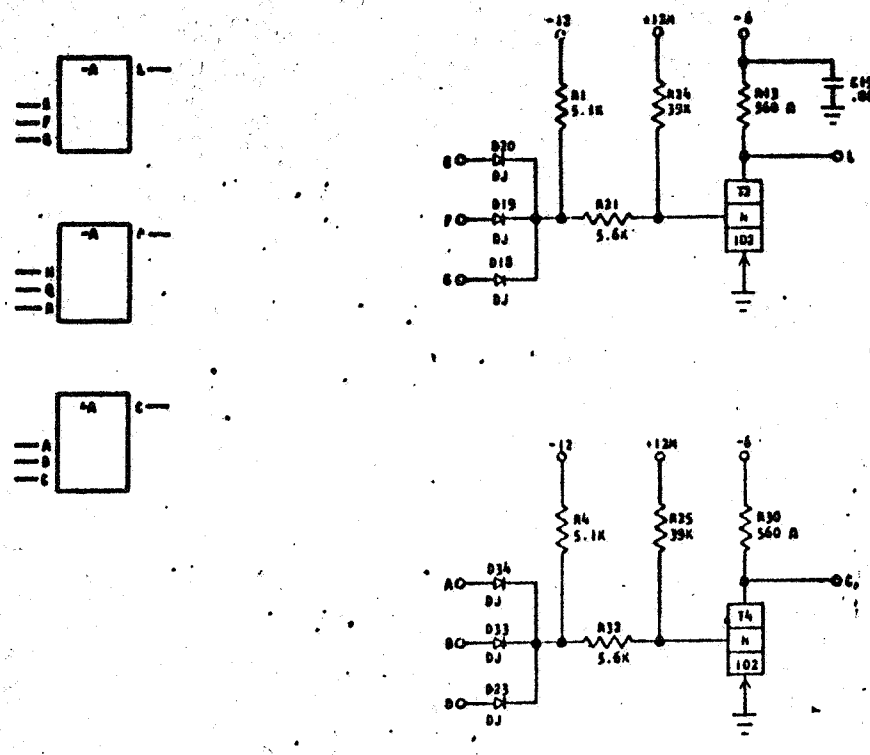
D C V -

729915

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370378

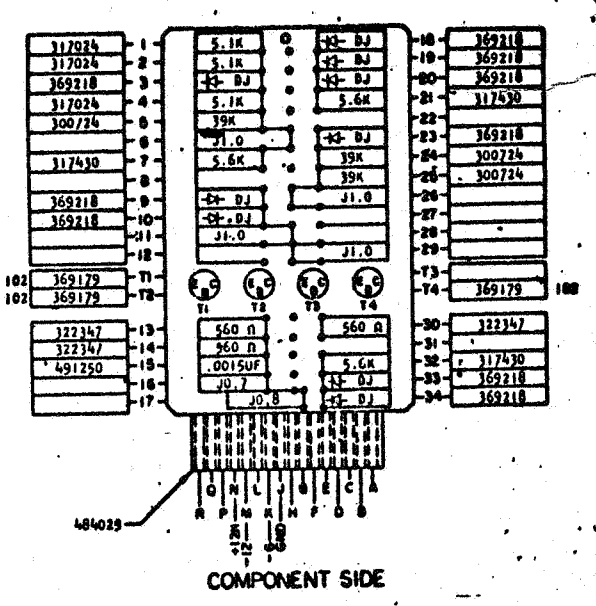
SDTDL - 3-WAY LOGIC BLOCK LOW SPEED WITH LOADS



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,H, A	V	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F,G, B	V	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
S,R, D	V	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L,P, C	V	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



COMPONENT SIDE

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	160*
TURN OFF (NSEC)	40	300**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	6-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL-3-WAY				6-21-62	115599					
	LOGIC BLOCK LOW SPEED WITH LOADS				1-3-63	EC 116034					
DESIGN			MODEL	SMS	30-4-63	77 B3687					
DETAIL	RO	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRD			CHECK								

729915

C

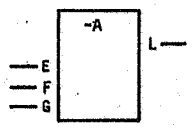
729916 | STANDARDS CODE

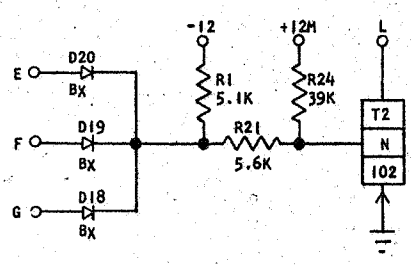
CARD CODE 729916
D G W -

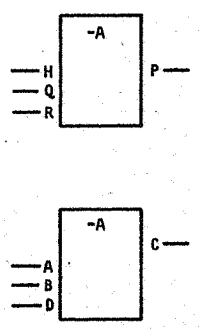
REFERENCE DRAWING

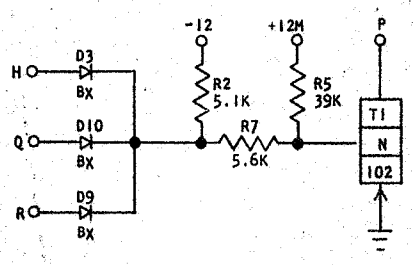
SEE PRODUCTION DRAWING 370377

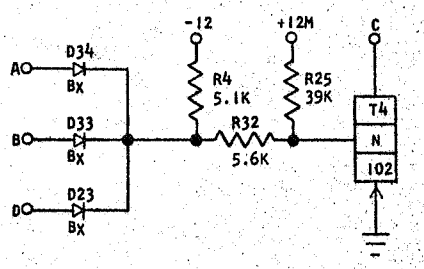
SDTDL 3-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS











SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F,Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,R, D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L,P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

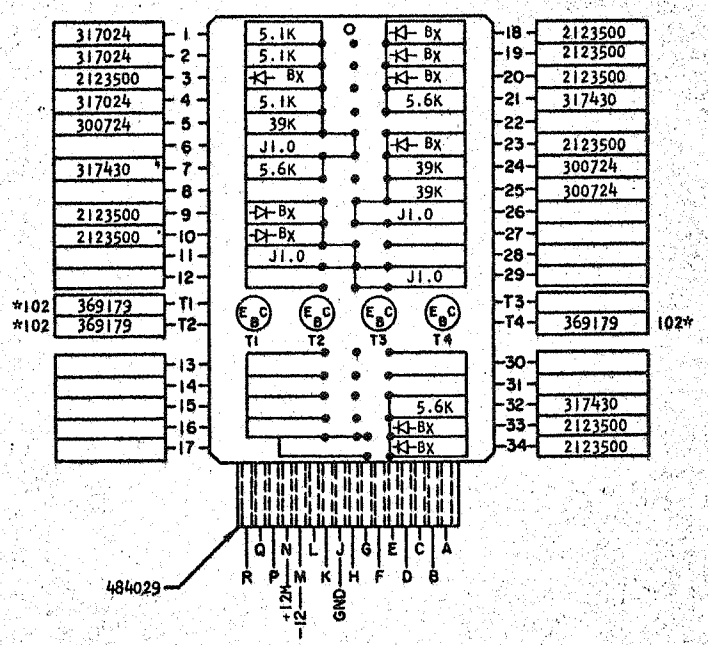
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 3-WAY					4-2-62	115599					
LOGIC BCK LOW SPEED WITHOUT LOADS												
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729916

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729916

STANDARDS CODE

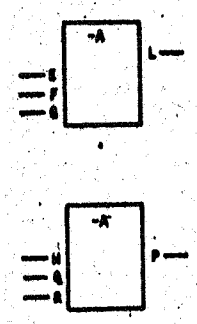
CARD CODE 729916

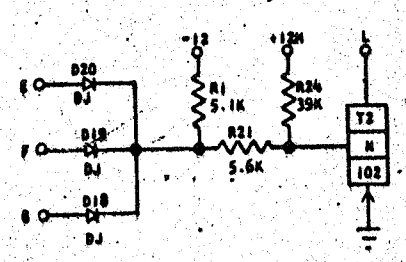
D G W -

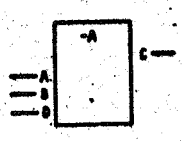
REFERENCE DRAWING

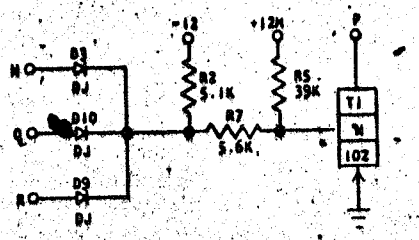
SEE PRODUCTION DRAWING 370377

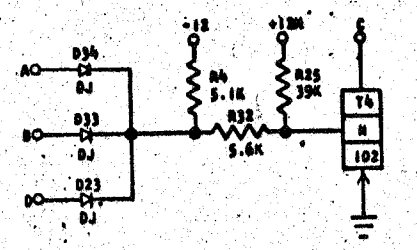
SDTDL 3-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS







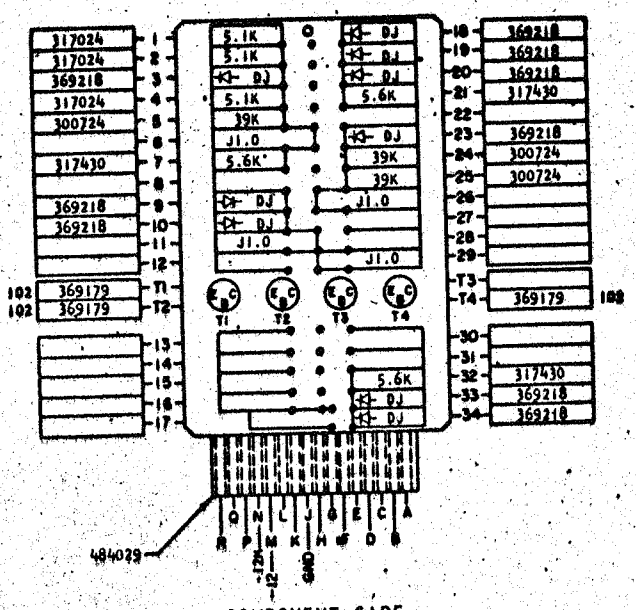




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,H,A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F,Q,B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,R,D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L,P,C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



COMPONENT SIDE

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 3-WAY				6-29-62	115599					
LOGIC BCK LOW SPEED WITHOUT LOADS					3-3-63	EC 116034					
DESIGN			MODEL	SMS	30-4-63	JT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIQ 3-12-62							
APPRO			CHECK								

729916

C

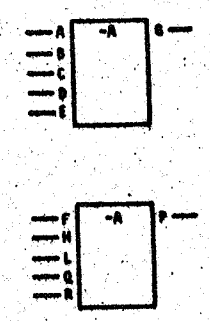
STANDARD CODE	729917
CARD CODE	D G X -

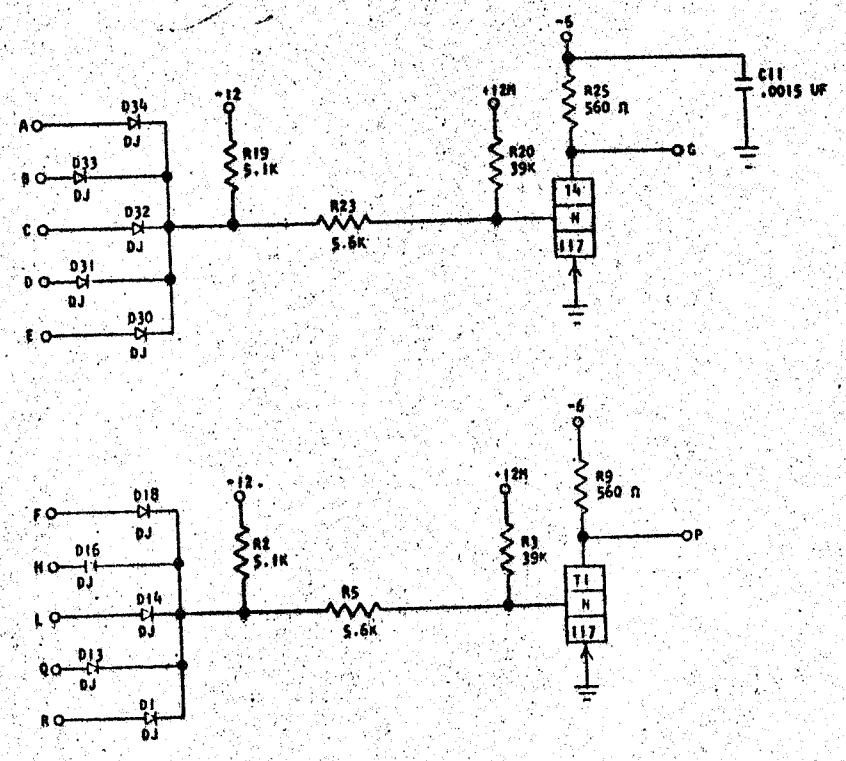
729917

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370376

SDTDL-5-WAY LOGIC BLOCK LOW SPEED WITH LOADS

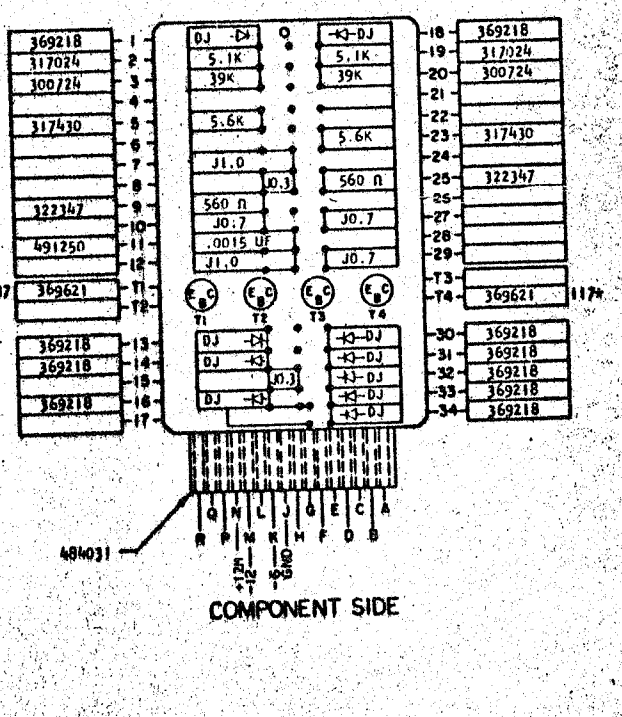




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C,L	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E,R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



COMPONENT SIDE

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 5-WAY				6-29-62	EC 115599					729917
	LOGIC BLOCK LOW SPEED WITHLOADS				30.4.63	TT83687					
DESIGN			MODEL	SMS							
DETAIL	RG	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIB 3-17-62							
APPRO			CHECK								

C

729917

729918

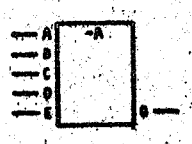
729918

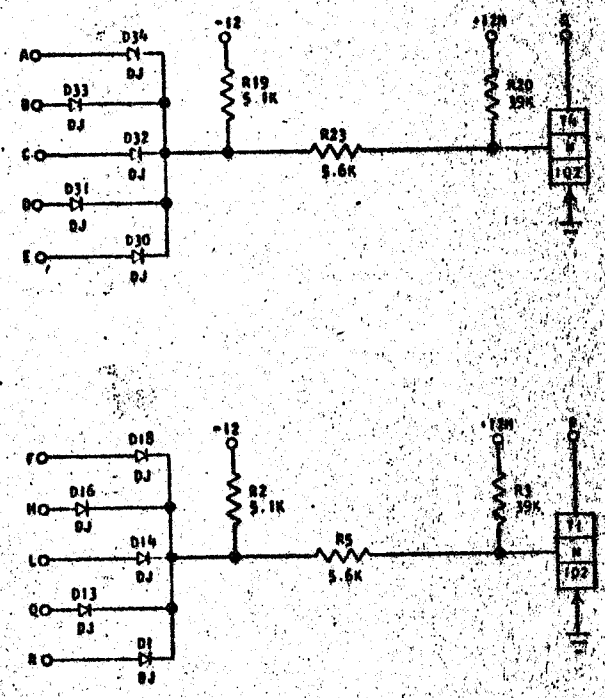
729918

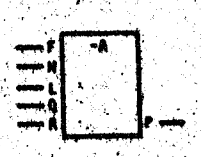
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370375

SDTDL 5 WAY LOGIC BLOCK LOW SPEED WITHOUT LOAD







SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
A,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
B,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
C,L	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
D,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
E,R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
G,P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

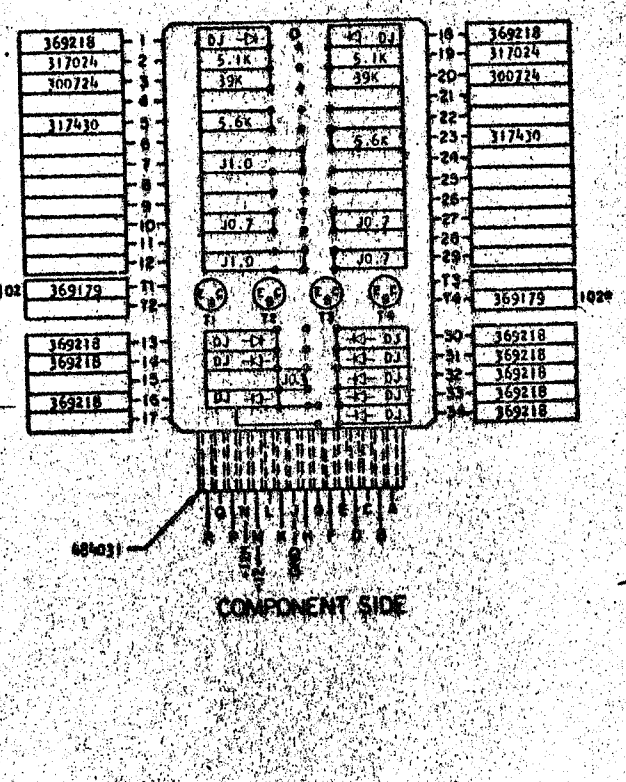
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	NO	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 5-WAY					6-29-62	EC 115599					
	LOGIC BLOCK LOW SPEED W0/LOAD					30-9-63	TT83687					
DESIGN			MODEL	SMS								
DRAWN	RG	5-1-62	SCALE	NONE								
CHECK	MB	5-1-62	DRAW	LIG	7-1962							
APPRO			CHECK									

729918

8-6677

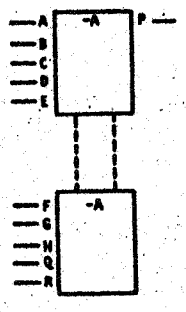
729919 STANDARDS CODE

CARD CODE 729919
D G Z -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370373

SDTDL 10 WAY LOGIC BLOCK LOW SPEED WITH LOAD



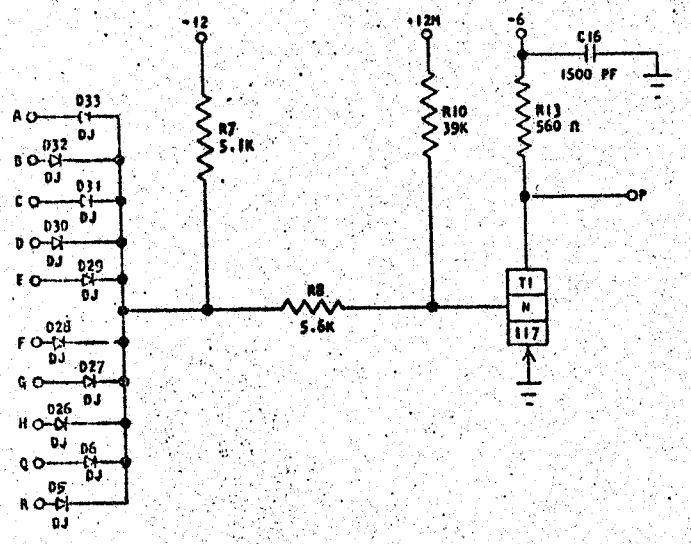
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

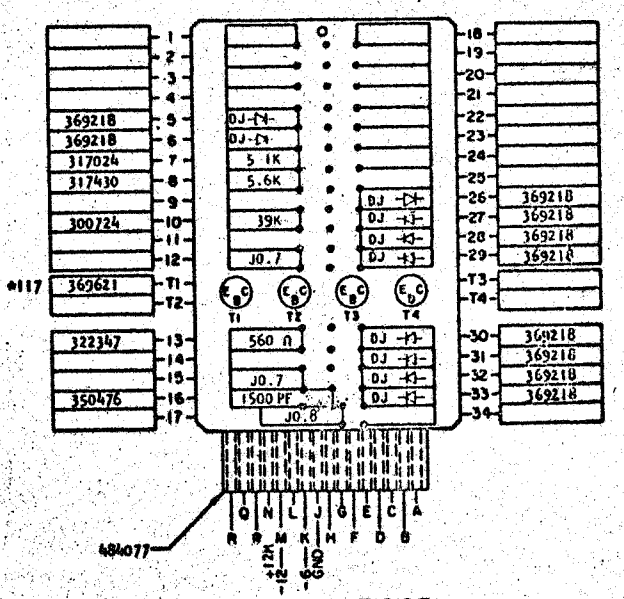
**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM 1STR-SDTDL 10 WAY LOGIC BLOCK LOW SPEED WITH LOAD					6-29-62	EC 115599					
						10-9-63	JT 83687					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIC	3-17-62							
APPRO			CHECK									

729919

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729919

STANDARDS CODE 729920

CARD CODE 729920
D H A -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370374

DELAY: SDTDL - LOW SPEED

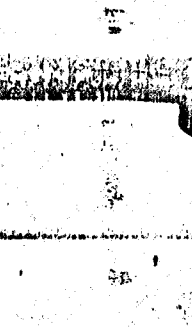
LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

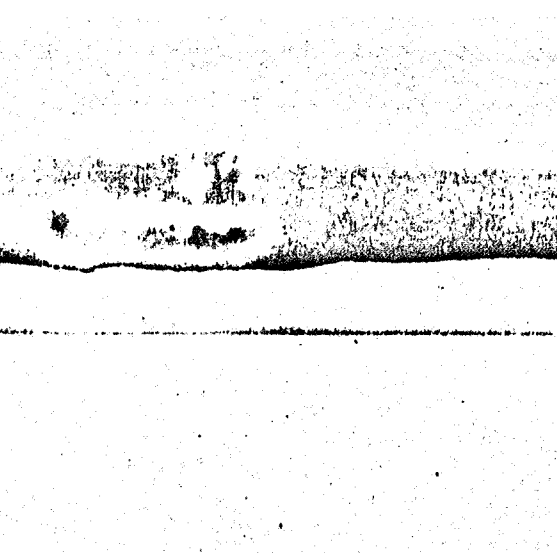
	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

SDTDL 10-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS

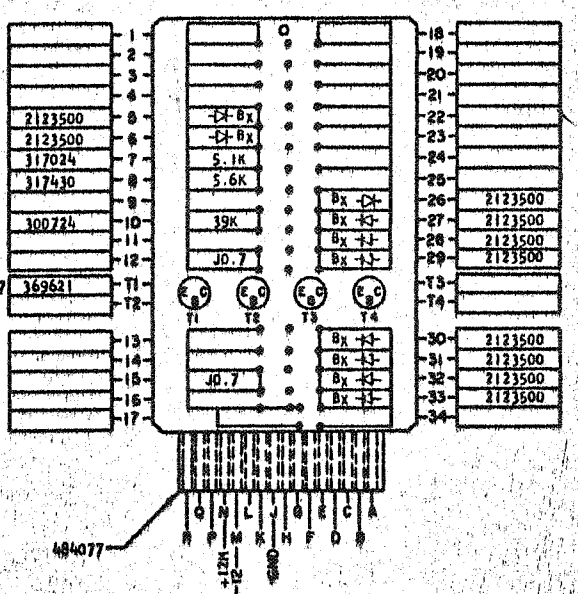




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP.
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN.
3. COLLECTOR MUST BE LOADED.
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



CIRCUIT ANR PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 10-WAY LOGIC BLOCK LOW SPEED W/O LOADS				-.62	115599					729920
DESIGN			MODEL	SMS							
DETAIL	RC	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIGD-17-62							
APPRD			CHECK								

C

729920

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729920

DHA -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370374

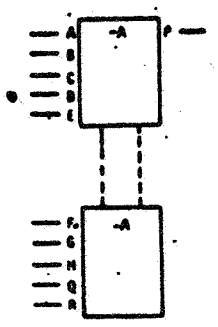
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

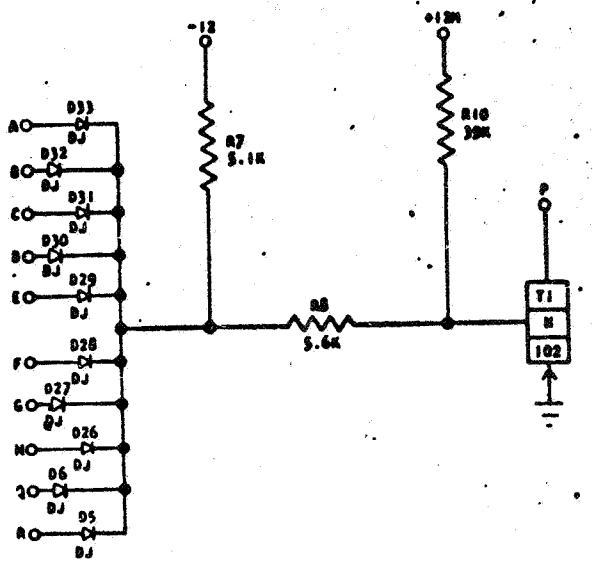
	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 300 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



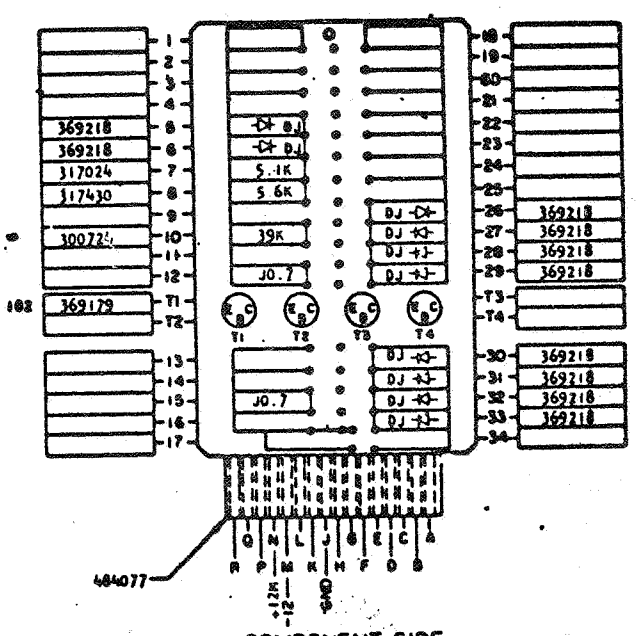
SDTDL 10-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP.
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN.
3. COLLECTOR MUST BE LOADED.
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
P	/R	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP											
NAME	CARD ASM TSTR-SDTDL 10-WAY				DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
	LOGIC BLOCK LOW SPEED W/O LOADS				4-19-62	115589					
DESIGN			MODEL	SMS	1-3-63	EC 116034					
DETAIL	RQ	3-1-62	SCALE	NONE	30.4.63	JT 83687					
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729920

C

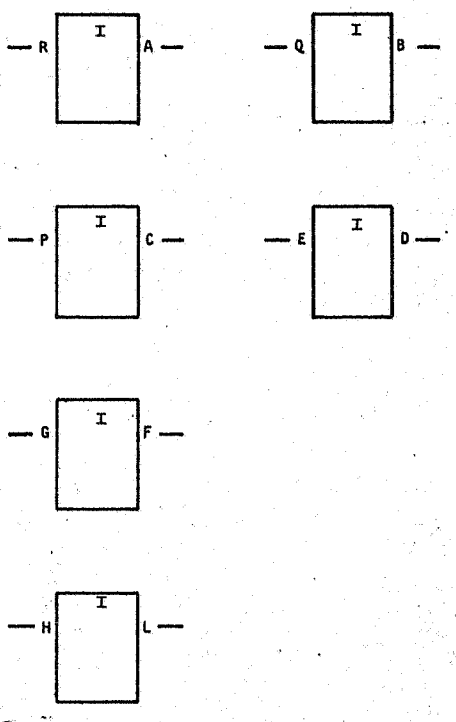
STANDARDS CODE	729921

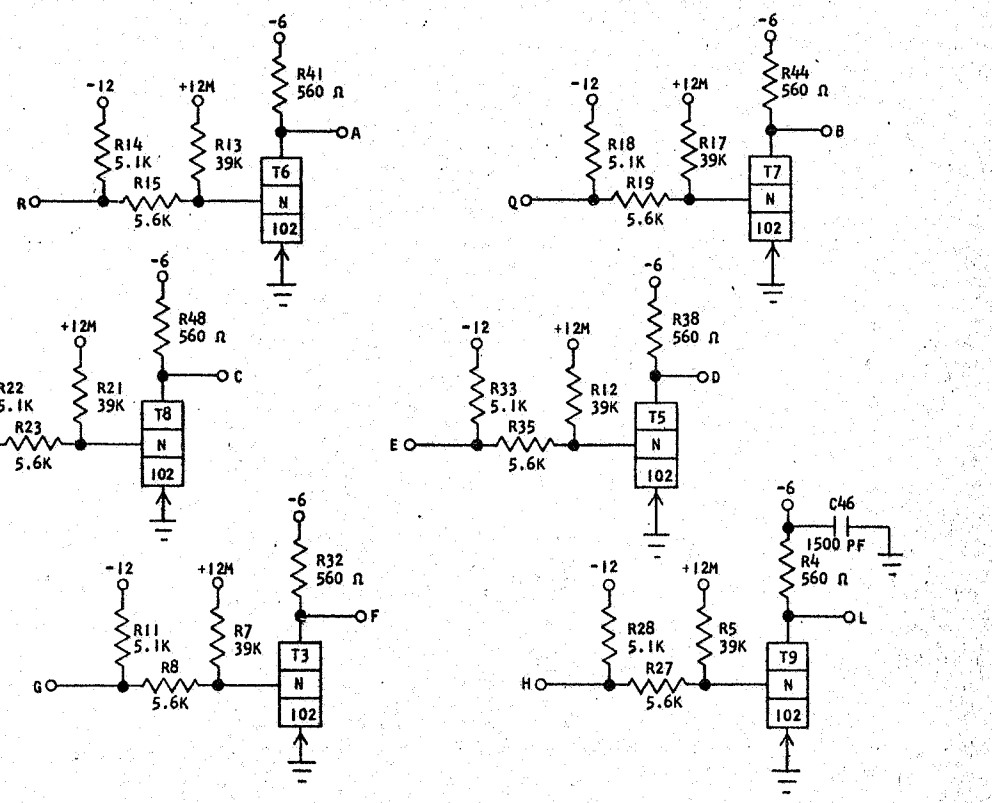
CARD CODE	729921
D H B -	

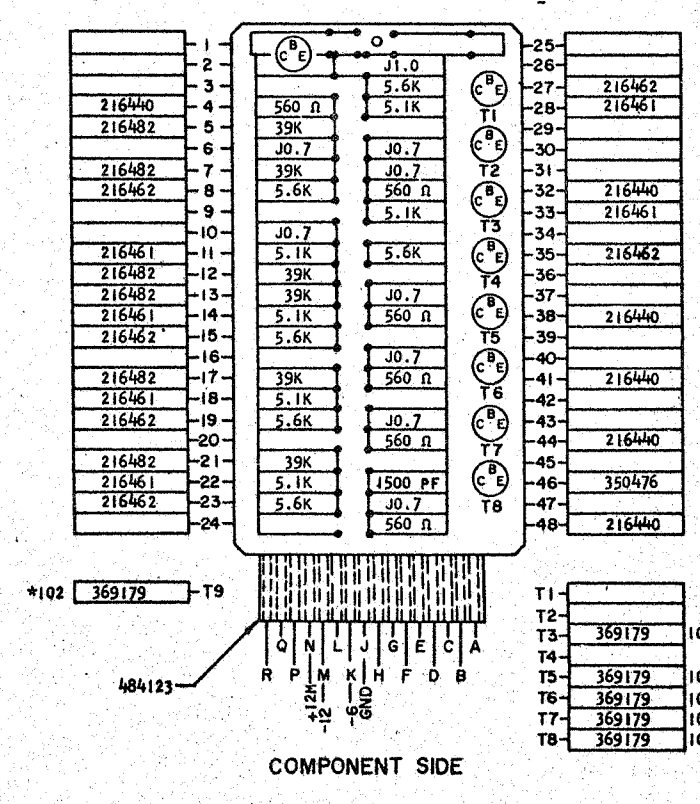
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370348

SDTDL INVERTER LOW SPEED WITH LOAD







COMPONENT SIDE

SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
R,Q,P, E,G,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,H	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESOSTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SDTDL					6 -62	115599					
INVERTER LOW SPEED WITH LOAD												
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729921

C

C. B. CO., NO. 878W 41774

729921

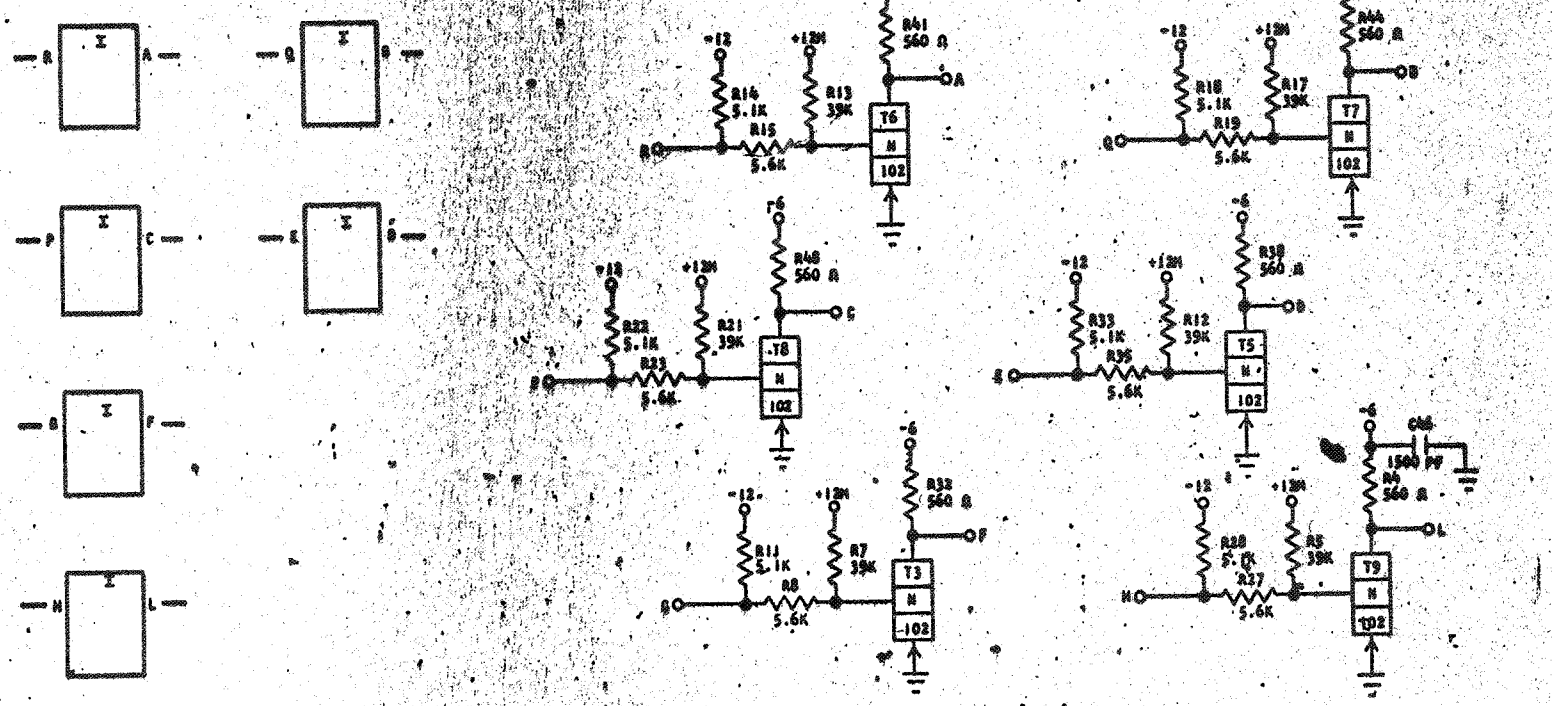
CARD CODE 729921

D H R -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370348

SDTDL INVERTER LOW SPEED WITH LOAD



SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
R,Q,P, E,G,N	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,M	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SDTDL					6-29-62	115599					
INVERTER LOW SPEED WITH LOAD						1-3-63	EC 116034					
DESIGN			MODEL	SMS		30.4.63	JT 83687					
DETAIL	RO	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729921

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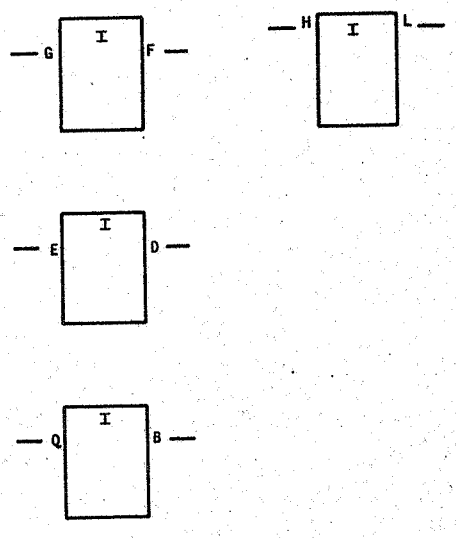
STANDARDS CODE 729922

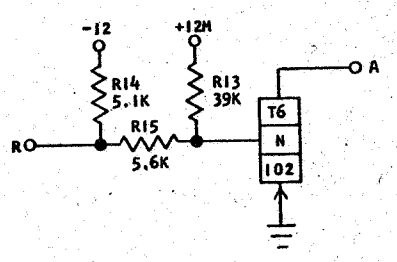
CARD CODE 729922
D H C -

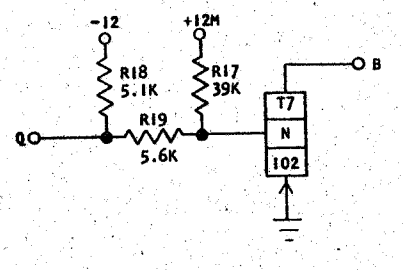
REFERENCE DRAWING

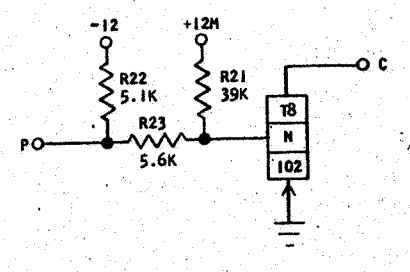
SEE PRODUCTION DRAWING 370372

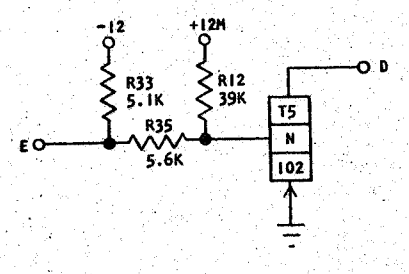


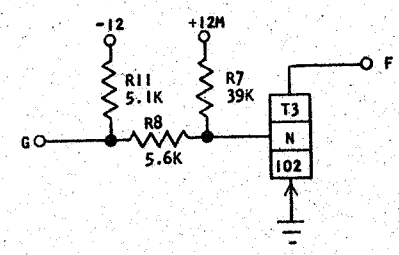
SDTDL INVERTER LOW SPEED W/O LOAD

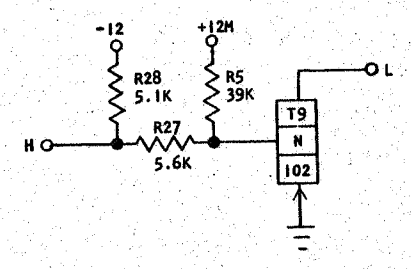












SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. ALL COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
R,Q,P, E,G,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

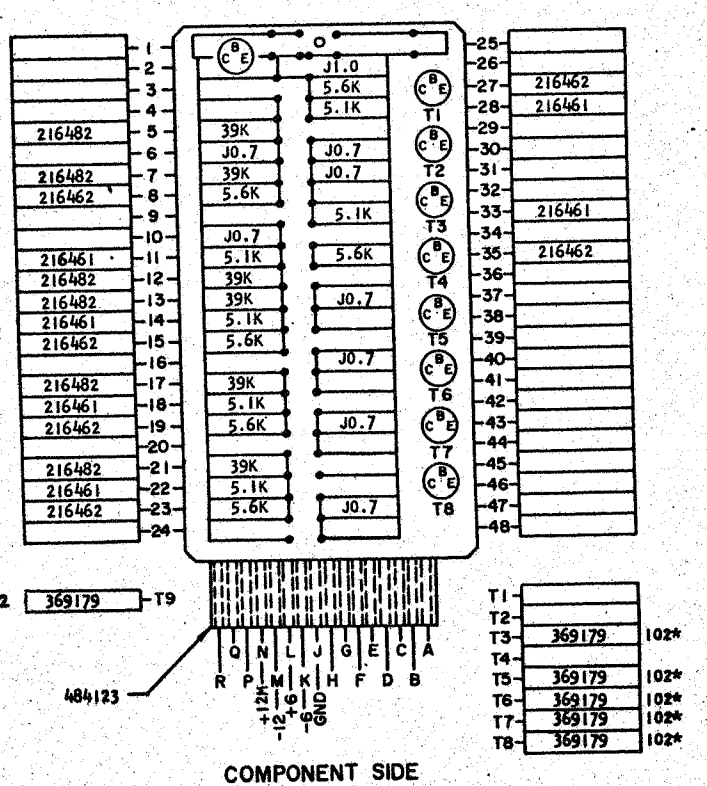
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR- SDTDL				
INVERTER LOW SPEED W/O LOAD					
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL
-62	115599				

DEVELOPMENT NO. 729922

C

729922

729923

STANDARDS CODE

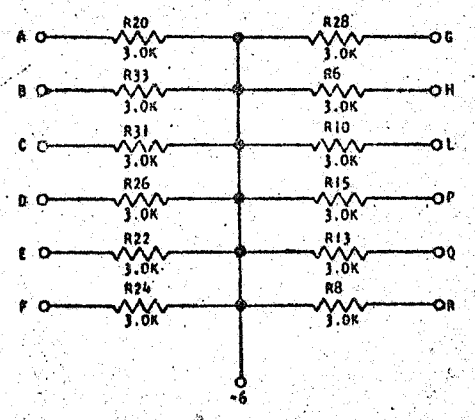
CARD CODE 729923

JHD-

REFERENCE DRAWING

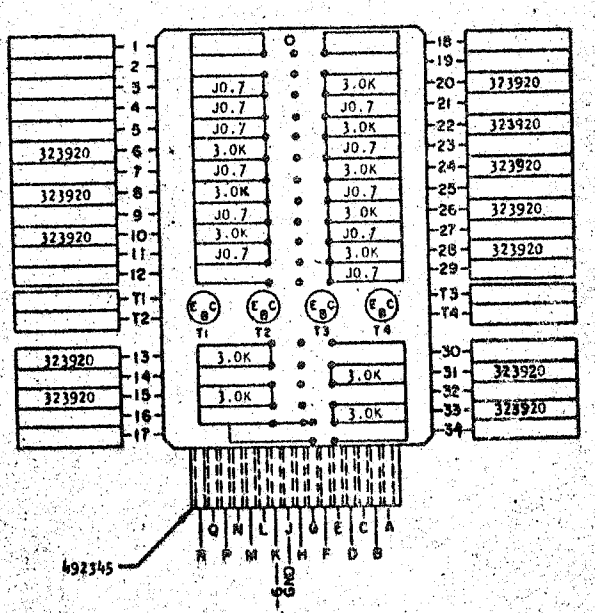
SEE PRODUCTION DRAWING 370371

SDTDL AND SDTRL 3K RESISTOR LOAD



APPLICATION

1. FOR COLLECTOR LOADING OF SDTDL AND SDTRL CARDS



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL AND SDTRL 3K RESISTOR CARD					6-29-62	EC 115599					729923
						30.4.68	JT 83687					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

C

729923

STANDARDS CODE	729924

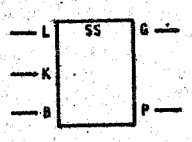
CARD CODE	729924
DHE-	

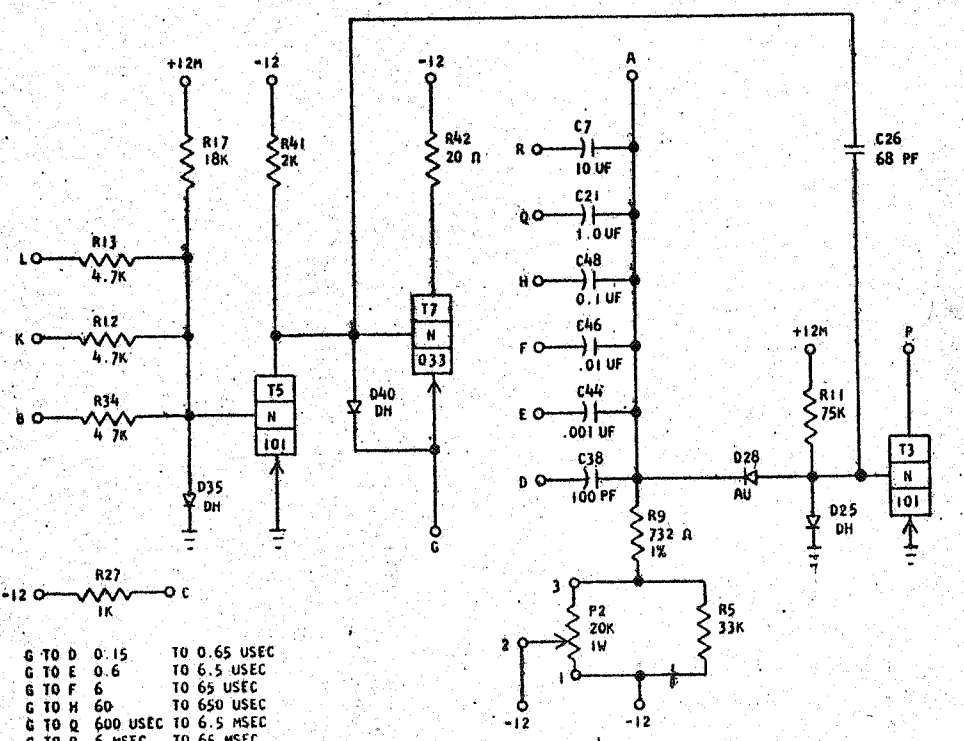
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370262

SDTRL - SINGLE SHOT

0.15 USEC TO 65 MSEC



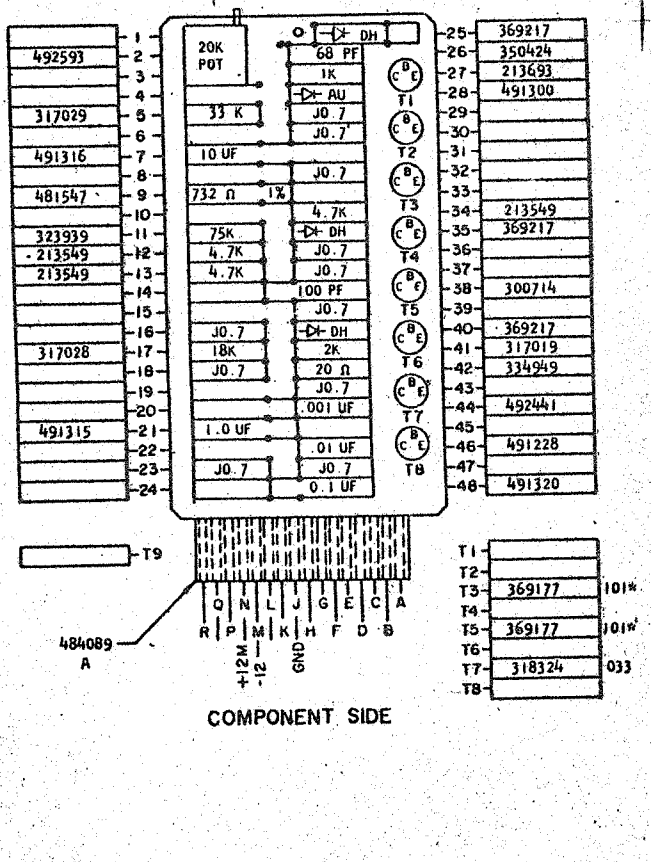


G TO D	0.15	TO 0.65 USEC
G TO E	0.6	TO 6.5 USEC
G TO F	6	TO 65 USEC
G TO H	60	TO 650 USEC
G TO Q	600 USEC	TO 6.5 MSEC
G TO R	6 MSEC	TO 65 MSEC

SEQUENCE OF OPERATION

1. PIN P TIED TO C FOR COLLECTOR LOAD, AND TO ANY INPUT IF INPUT PULSE IS NARROWER THAN REQUIRED OUTPUT PULSE. G IS TIED TO REQUIRED TIME CONSTANT INPUT
2. ALL INPUTS UP T5 OFF, T3 ON, OUTPUT UP
3. DOWN INPUT T5 ON, T3 OFF, OUTPUT DOWN
4. T3 TURNED BACK ON AT END OF TIME CONSTANT

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
L	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
K	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
B	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
P	Y	OUTPUT		UP	-0.6	-0.1
				DOWN	-6.87	-10.5
T3 BASE		SWITCH LEVEL				



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARDS	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL-SINGLE SHOT					6-19-62	115599					
DESIGN			MODEL	SMS								
DETAIL	RO	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRD			CHECK									

729924

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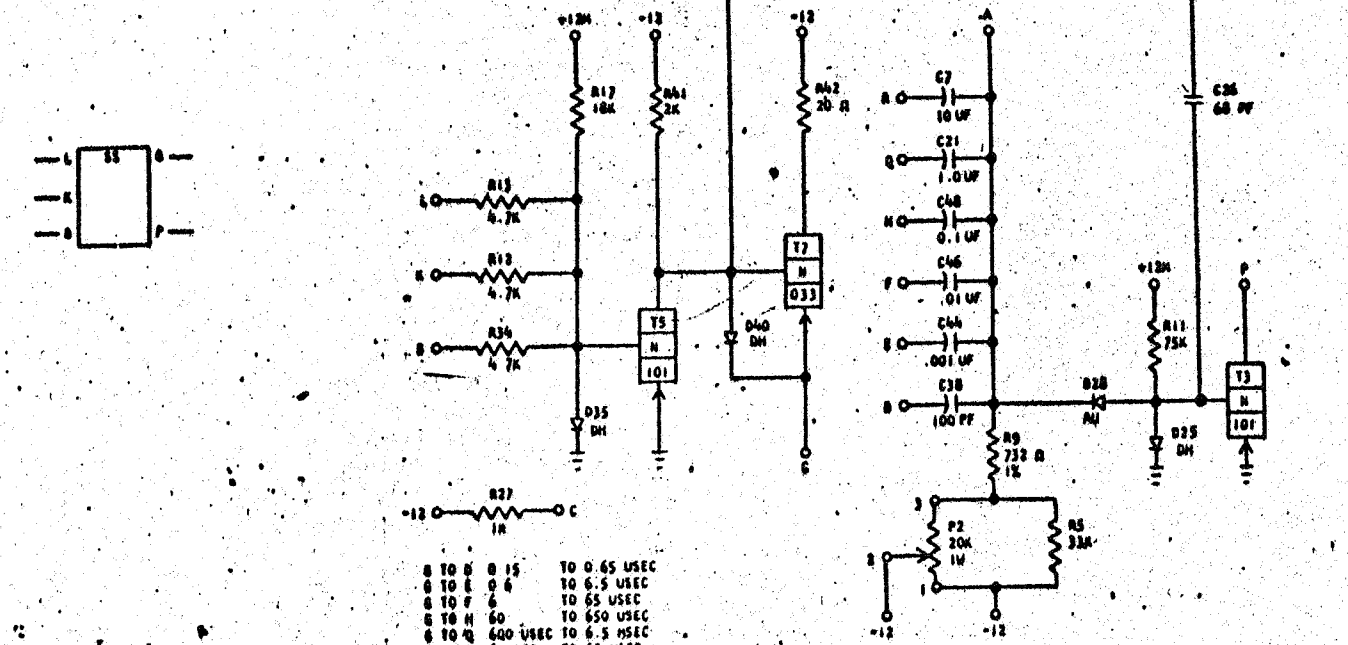
REFERENCE DRAWING

SEE PRODUCTION DRAWING 570262

SDTRL - SINGLE SHOT

0.15 USEC TO 65 MSEC

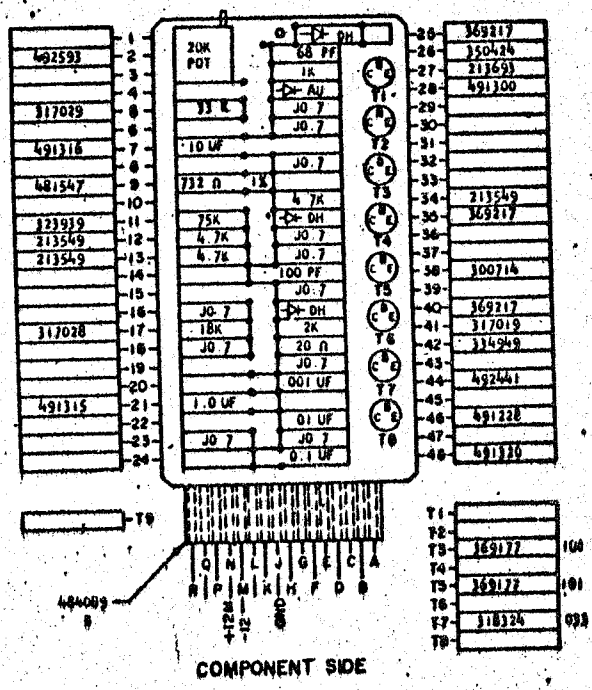


B TO B	0.15	TO 0.65 USEC
B TO E	0.6	TO 6.5 USEC
B TO F	6	TO 65 USEC
B TO H	60	TO 650 USEC
B TO Q	600 USEC	TO 6.5 MSEC
B TO R	6 MSEC	TO 65 MSEC

SEQUENCE OF OPERATION

1. PIN P TIED TO C FOR COLLECTOR LOAD, AND TO ANY INPUT IF INPUT PULSE IS NARROWER THAN REQUIRED OUTPUT PULSE. B IS TIED TO REQUIRED TIME CONSTANT INPUT
2. ALL INPUTS UP T5 OFF, T3 ON, OUTPUT UP
3. DOWN INPUT T5 ON, T3 OFF, OUTPUT DOWN
4. T3 TURNED BACK ON AT END OF TIME CONSTANT

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
L	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
K	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
B	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
P	Y	OUTPUT		UP	-0.6	-0.1
				DOWN	-6.87	-10.5
T3 BASE		SWITCH LEVEL →				



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL- SINGLE SHOT				6-29-62	115599					
			MODEL	SMS	1-3-63	EC116034					
DESIGN					30-4-63	JT B36B7					
DETAIL	RG	7-1-62	SCALE	NONE	—	—					
CHECK	WH	7-1-62	DRAW	LLG 7-17-62							
APPD			CHECK								

729924

C

4 5 6 7

729925

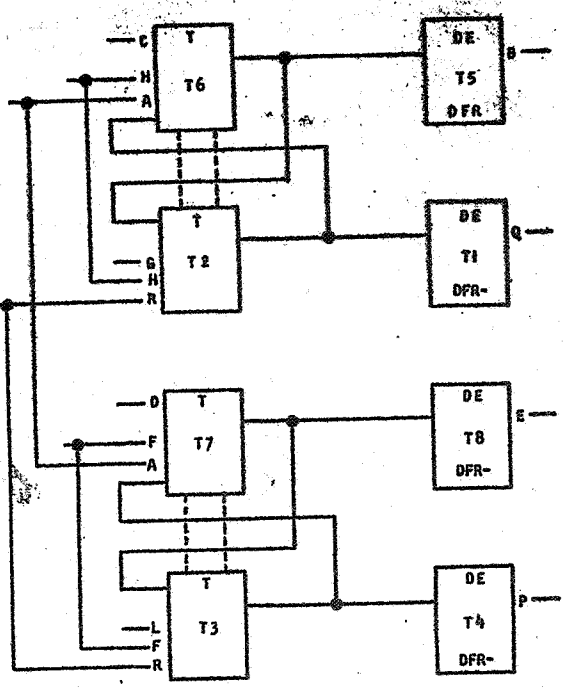
STANDARDS CODE

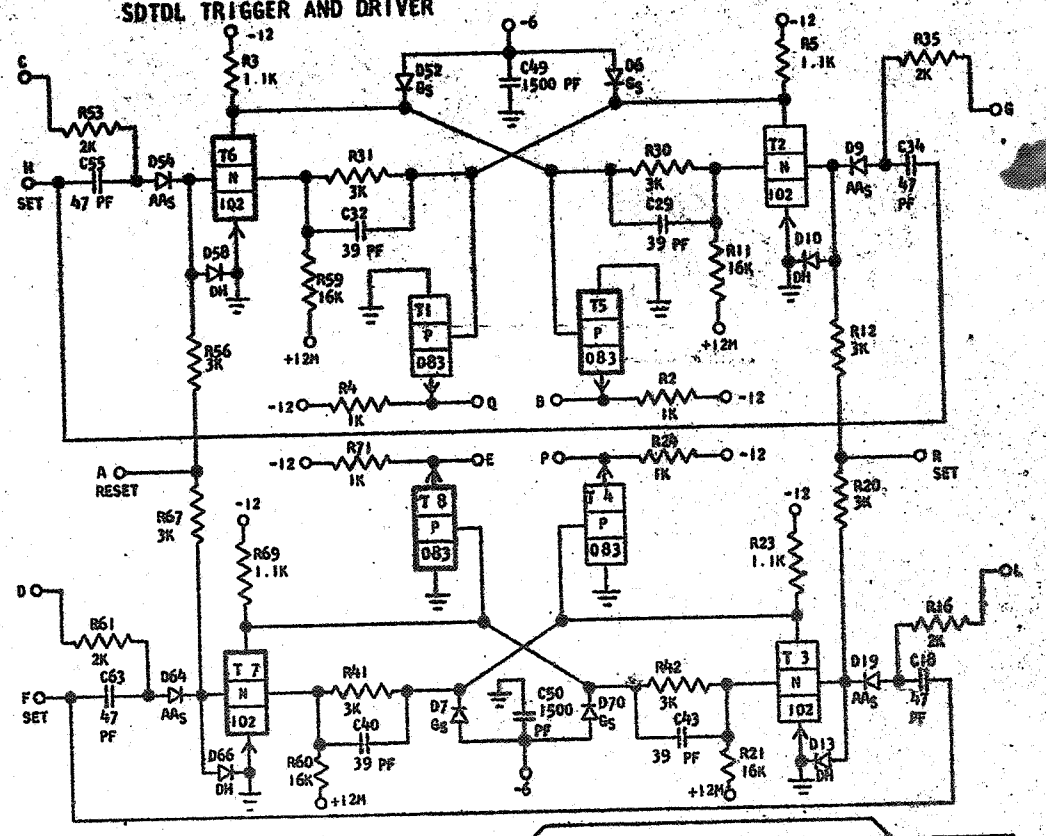
CARD CODE 729925

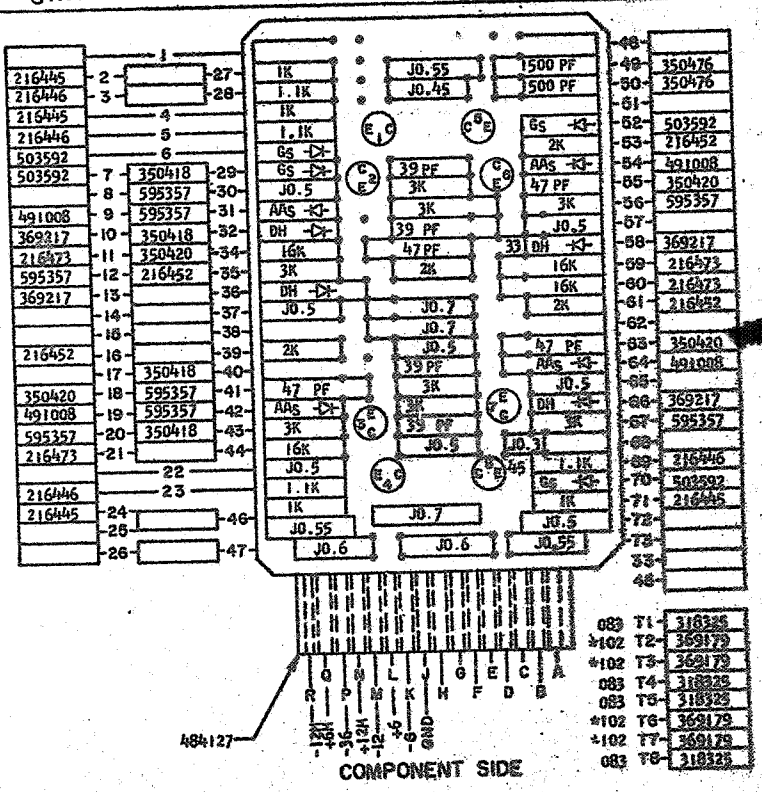
D H F -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370350







SEQUENCE OF OPERATION

THE RESET INPUT RESPONDS TO A NEGATIVE VOLTAGE LEVEL. RESETING TURNS T6, T7, T5 AND T8 ON AND THE OTHER TRANSISTORS WILL BE IN THE OPPOSITE STATE. THE GATES ARE CONDITIONED BY A POSITIVE VOLTAGE LEVEL AND THE AC SET IS RESPONSIVE TO A POSITIVE VOLTAGE LEVEL. THUS, TO SET THE TRIGGER MEANS TO TURN OFF THE TRANSISTOR WHOSE GATE AND SET ARE BOTH POSITIVE. THE DC SET RESPONDS TO A NEGATIVE VOLTAGE LEVEL. THUS WHEN THE TRIGGER IS DC SET, T2, T3, T1 AND T4 WILL BE ON.

DELAY - NSEC

	TON MAX	TON MIN	TRISE MAX	TRISE MIN	TOFF MAX	TOFF MIN	TFALL MAX	TFALL MIN
BINARY OPERATION:	123	36	63	16	240	115	200	95
GATED:	135	40	48	16	205	82	160	61

NOTE: TON IS DEFINED AS THE DELAY FROM THE TIME AN AC INPUT SIGNAL ARRIVES UNTIL THE "OFF" TRANSISTOR HAS TURNED ON COMPLETELY. THIS IS MEASURED FROM THE TIME THE AC INPUT HAS SHIFTED 10% IN THE POSITIVE DIRECTION UNTIL THE "OFF" TRANSISTOR HAS SHIFTED 90% POSITIVE.

TOFF IS MEASURED FROM THE TIME AN AC INPUT HAS SHIFTED 10% POSITIVE UNTIL THE OUTPUT OF THE "ON" TRANSISTOR HAS SHIFTED 90% NEGATIVE.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C,D	Y	GATE		UP	-.65	-.1
				DOWN	-5.81	-7.64
H,F	Y	AC SET		UP	-.65	-.1
				DOWN	-5.81	-7.64
R	Y	DC SET		UP	-.65	-.1
				DOWN	-5.81	-7.64
A	Y	RESET		UP	-.65	-.1
				DOWN	-5.81	-7.64
Q,P	Y	OUTPUT		UP	-1.1	-.22
				DOWN	-5.83	-7.3
B,E	Y	OUTPUT		UP	-1.1	-.22
				DOWN	-5.83	-7.3
G,L	Y	GATE		UP	-.65	-.1
				DOWN	-5.81	-7.64

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL TRIGGER AND DRIVER				4-19-62	115599					729925
DESIGN			MODEL	SMS							
DETAIL	RD	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

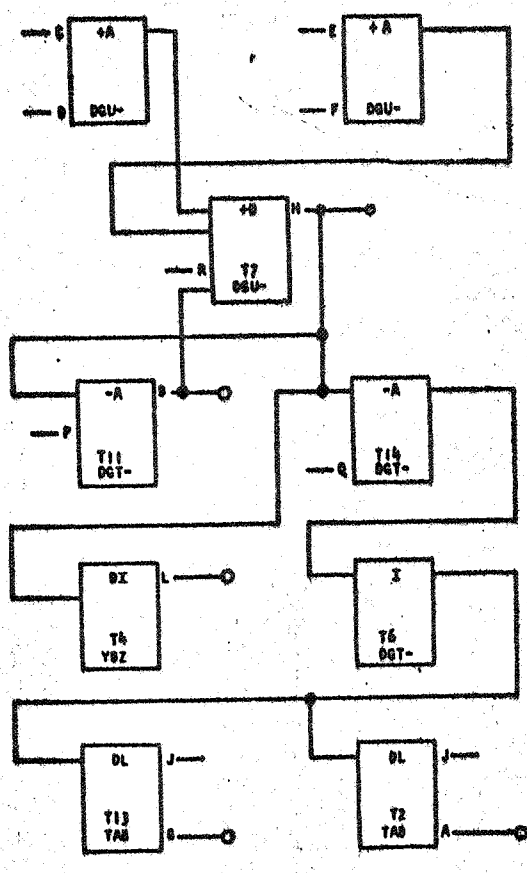
STANDARD CODE 729926

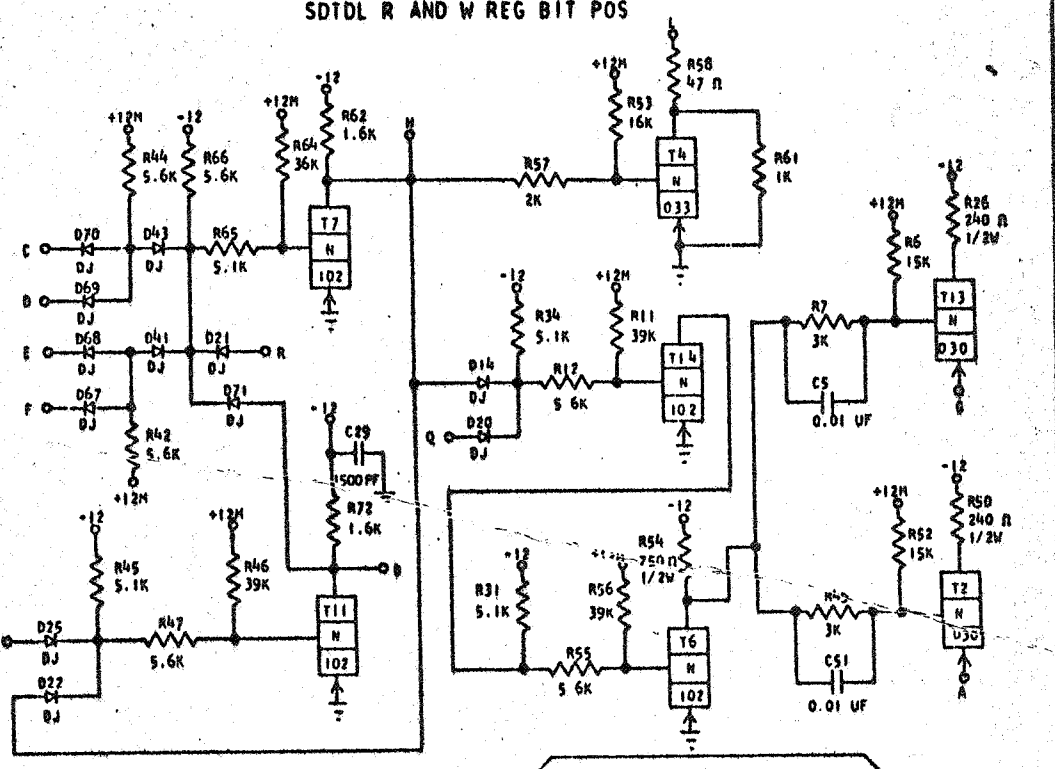
CARD CODE 729926
D H G -

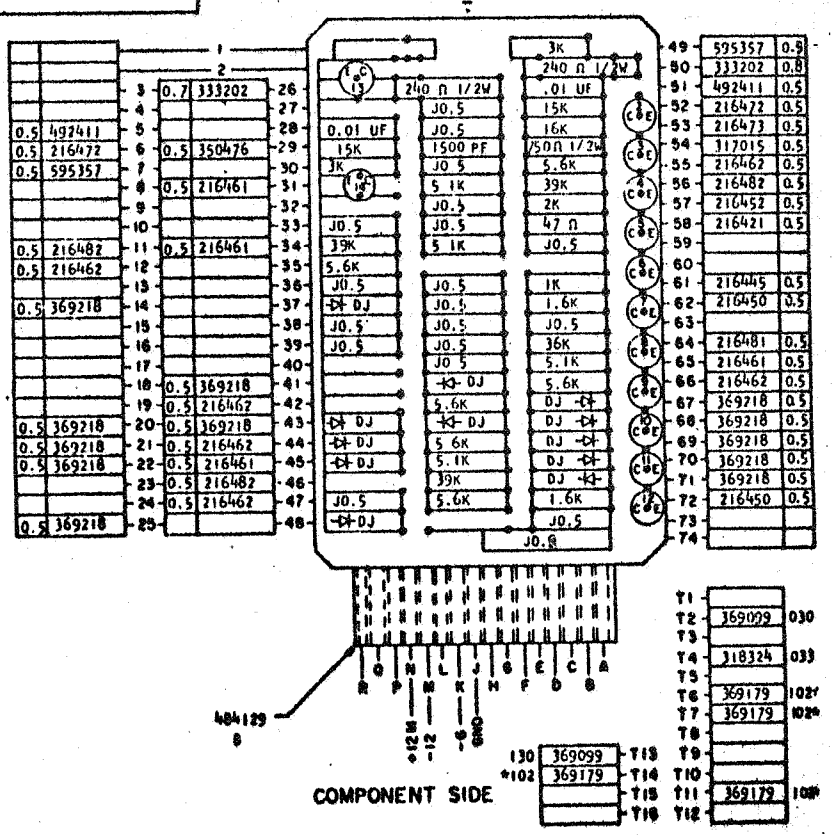
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370351

SDTDL R AND W REG BIT POS







SEQUENCE OF OPERATION

1. PINS CD OR EF OR R OR S IN UP LEVEL GIVES DOWN LEVEL AT PIN H. A DOWN LEVEL AT PIN H TURNS ON T4 GIVING UP LEVEL AT PIN L.
2. DOWN LEVELS ON PIN H AND Q GIVES UP LEVEL AT OUTPUT OF T14 WHICH TURNS T6 OFF AND T2 AND T13 ON GIVING VOLTAGE OUTPUT AT PINS A AND G (N LEVEL).
3. DOWN LEVEL AT PIN H WITH DOWN LEVEL AT PIN P RESULTS IN UP LEVEL AT PIN B
4. T7 AND T11 ACT AS A LATCH WITH GATE IN CONTROLS. THE LATCH BACK IS PERFORMED BY THE OUTPUT OF T11 BEING FED TO T7
5. T2 AND T13 ARE TRANSMISSION LINE DRIVERS CONVERTING S LEVEL INPUT TO A VOLTAGE SIGNAL FOR TRANSMISSION OVER A 93 OHM COAXIAL LINE
6. THE INPUTS ARE Y LINE LEVELS. FOR WAVEFORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS
7. DELAY - NSEC

		MIN.	MAX.
PINS C, D, E, F, R TO PIN H:	TURN ON	80	258
	TURN OFF	100	465
PINS C, D, E, F, R TO PIN B:	TURN ON	120	458
	TURN OFF	175	465
PIN P TO PIN B:	TURN ON	75	100
	TURN OFF	40	200
PIN Q TO PIN G OR A:	TURN ON	125	340
	TURN OFF	115	310
PINS C, D, E, F, R TO PIN G OR A:	TURN ON	195	568
	TURN OFF	225	709

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR SDTDL R AND W REG BIT POS	4-27-62	EC 115599					
	10.4.63	ST 83687					
DESIGN	MODEL SMS						
DETAIL AQ 5-1-62	SCALE NONE						
CHECK WR 5-1-63	DRAW LIG 5-17-62						
APPRD	CHECK						

729926

729926

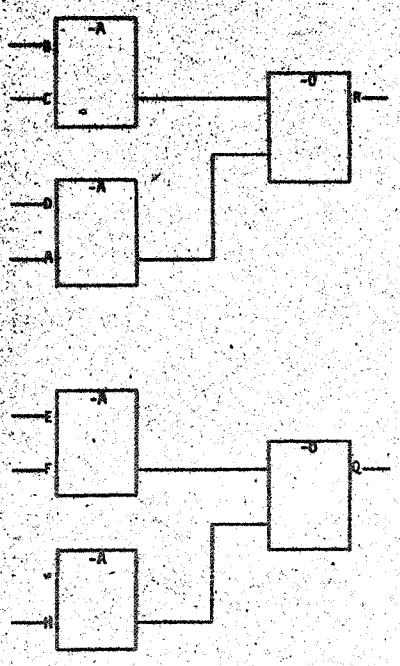
C

STANDARDS CODE 729927

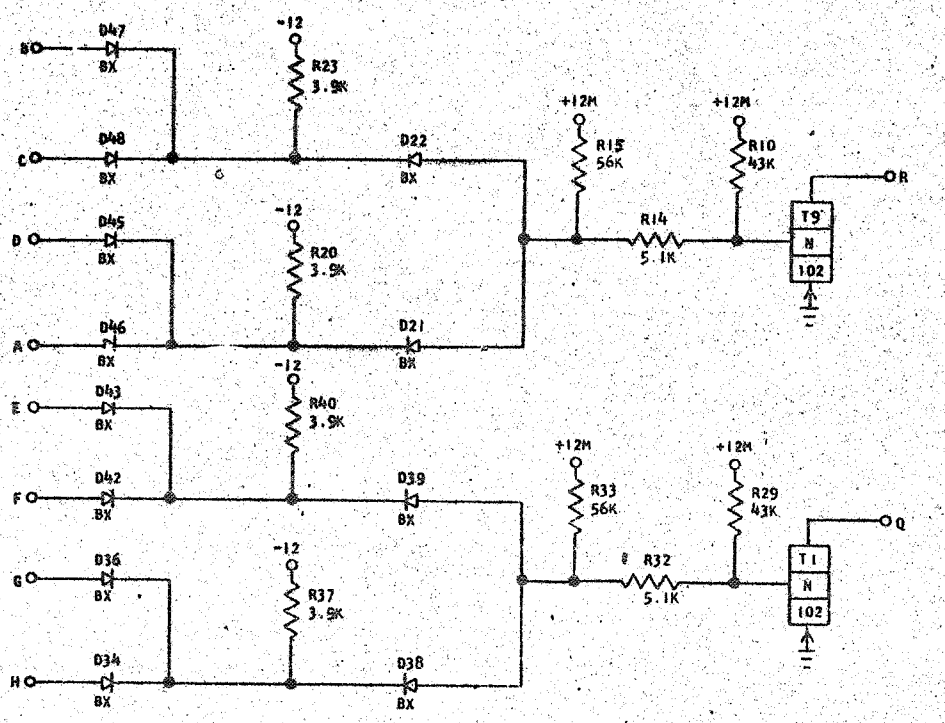
CARD CODE 729927
D H H -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370358



SDTDL DOUBLE LEVEL LOGIC BLOCK #2A LOW SPEED, WO LOADS



SEQUENCE OF OPERATION

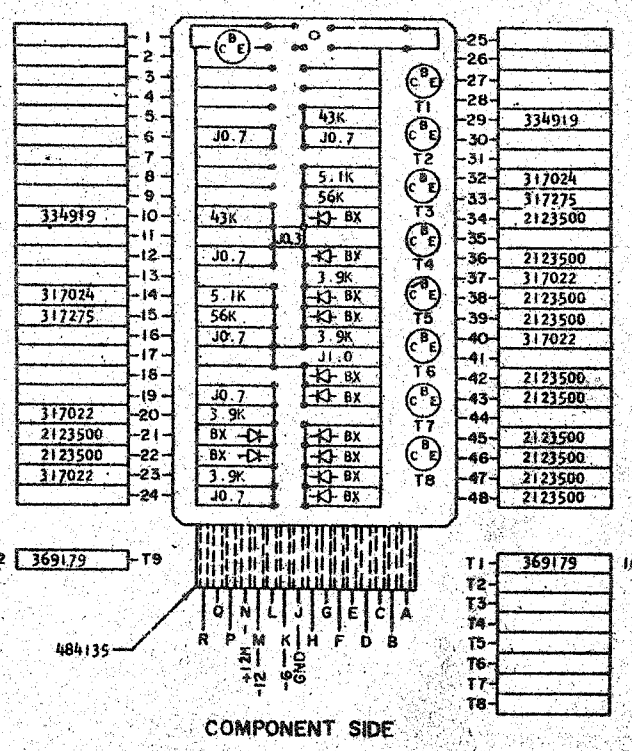
1. PINS B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D22
2. PINS D AND A MUST BE DOWN TO HAVE A DOWN LEVEL AT D21
3. EITHER LEVEL DOWN AT D21 OR D22 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP
4. EITHER B OR C UP WILL CAUSE AN UP LEVEL AT D22
5. EITHER D OR A WILL CAUSE AN UP LEVEL AT D21
6. BOTH LEVELS AT D21 AND D22 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN
7. T1 AND T9 MUST BE COLLECTOR LOADED

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
B,C D,A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	OUTPUTS		UP	-.65	.1
				DOWN	-5.81	-8.8
E,F G,H	Y	INPUTS		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	W	OUTPUTS		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY - NSEC

	MIN.	MAX
TURN ON	70	240
TURN OFF	110	515

NOTE: MAXIMUM DELAY MAY INCREASE FOR A 6.2K COLLECTOR RESISTOR.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME CARD ASM TSTR-SDTDL-DOUBLE LEVEL LG #2A LOW SPEED, WO LOADS					-62	115599						729927
DESIGN			MODEL	SMS								
DETAIL	RO	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRO			CHECK									

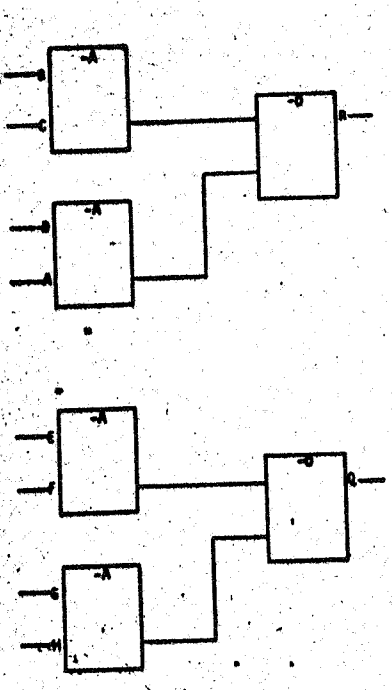
729927

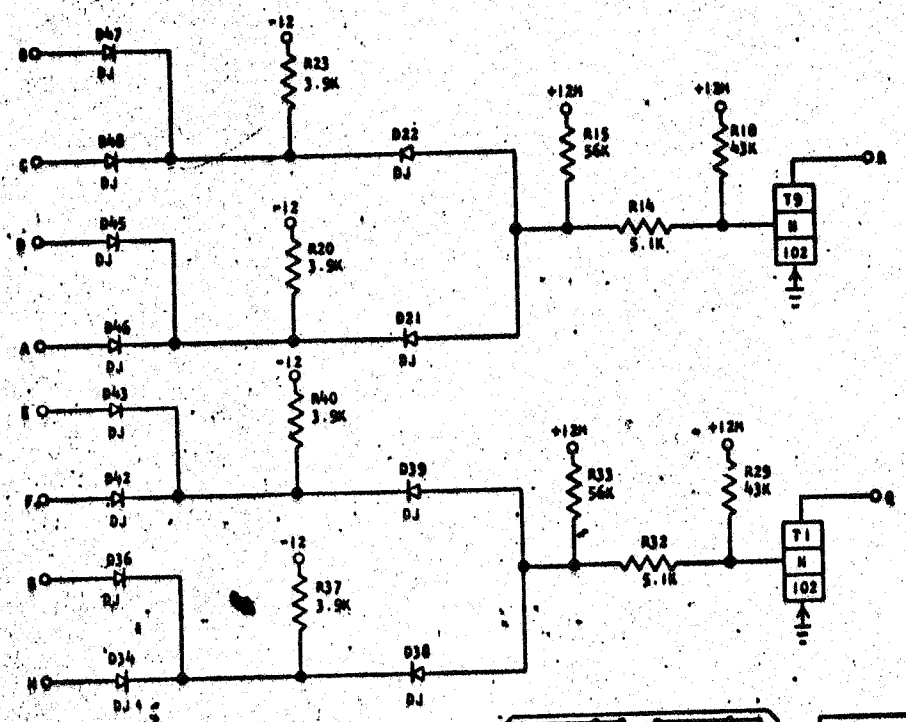
DHH-

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370358

SDTDL DOUBLE LEVEL LOGIC BLOCK #2A LOW SPEED, WO LOADS





SEQUENCE OF OPERATION

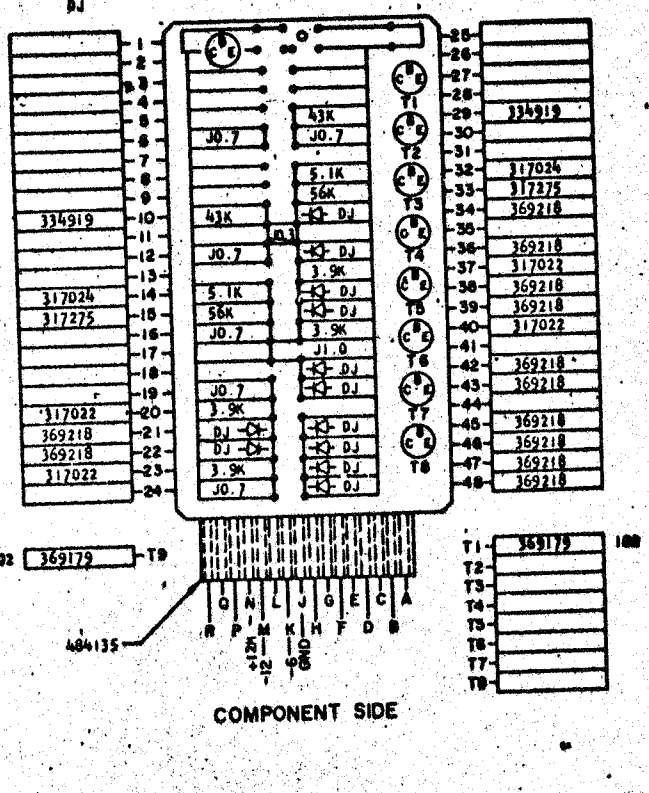
1. PINS B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D22
2. PINS D AND A MUST BE DOWN TO HAVE A DOWN LEVEL AT D21
3. EITHER LEVEL DOWN AT D21 OR D22 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP
4. EITHER B OR C UP WILL CAUSE AN UP LEVEL AT D22
5. EITHER D OR A WILL CAUSE AN UP LEVEL AT D21
6. BOTH LEVELS AT D21 AND D22 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN
7. T1 AND T9 MUST BE COLLECTOR LOADED

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,C D,A	Y	INPUT		UP	+.65	-.1
				DOWN	-5.81	-8.8
R	Y	OUTPUTS		UP	-.65	.1
				DOWN	-5.81	-8.8
E,F G,H	Y	INPUTS		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	OUTPUTS		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY - NSEC

	MIN.	MAX
TURN ON	70	240
TURN OFF	110	515

NOTE: MAXIMUM DELAY MAY INCREASE FOR A 6.2K COLLECTOR RESISTOR.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL-DOUBLE LEVEL LB #2A LOW SPEED, WO LOADS				2-11-62	115599					729927
DESIGN			MODEL	SMS	1-3-63	EC 116034					
DETAIL	RQ	3-1-62	SCALE	NONE	30-4-63	JT 83687					
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

729927

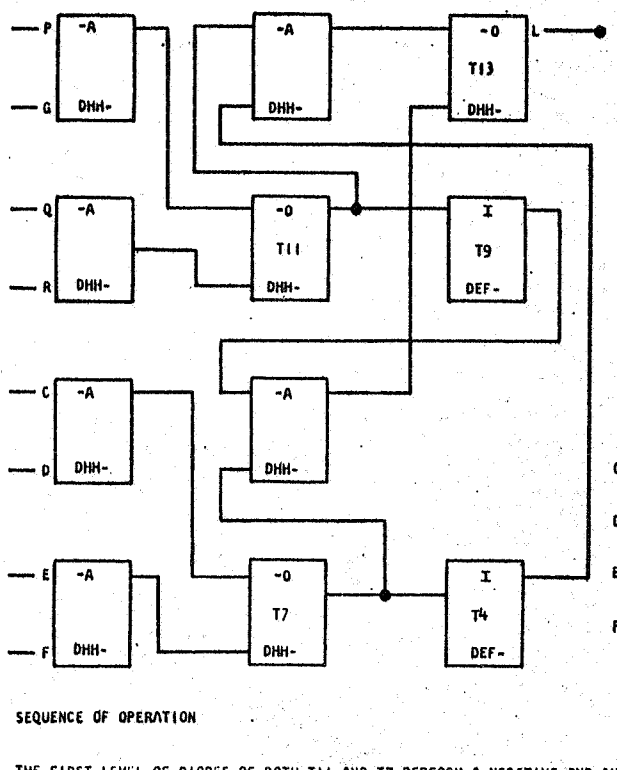
STANDARDS CODE 729928

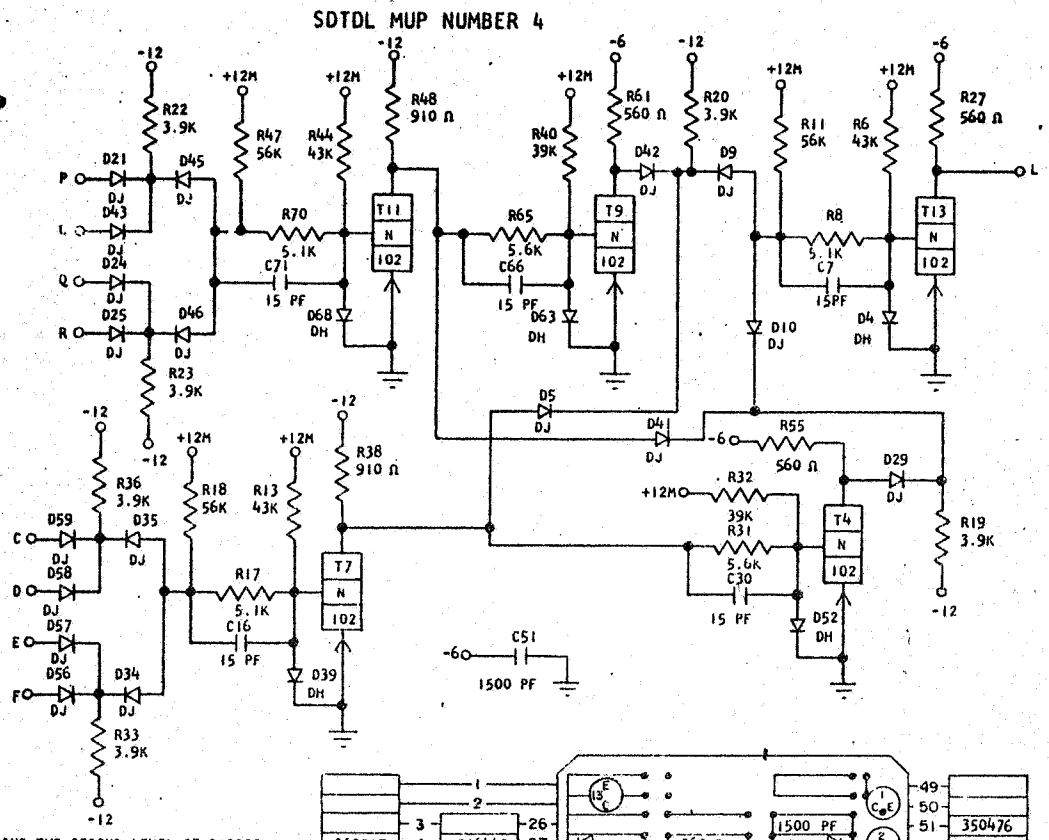
CARD CODE D H J - 729928

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370352

SDTDL MUP NUMBER 4





SEQUENCE OF OPERATION

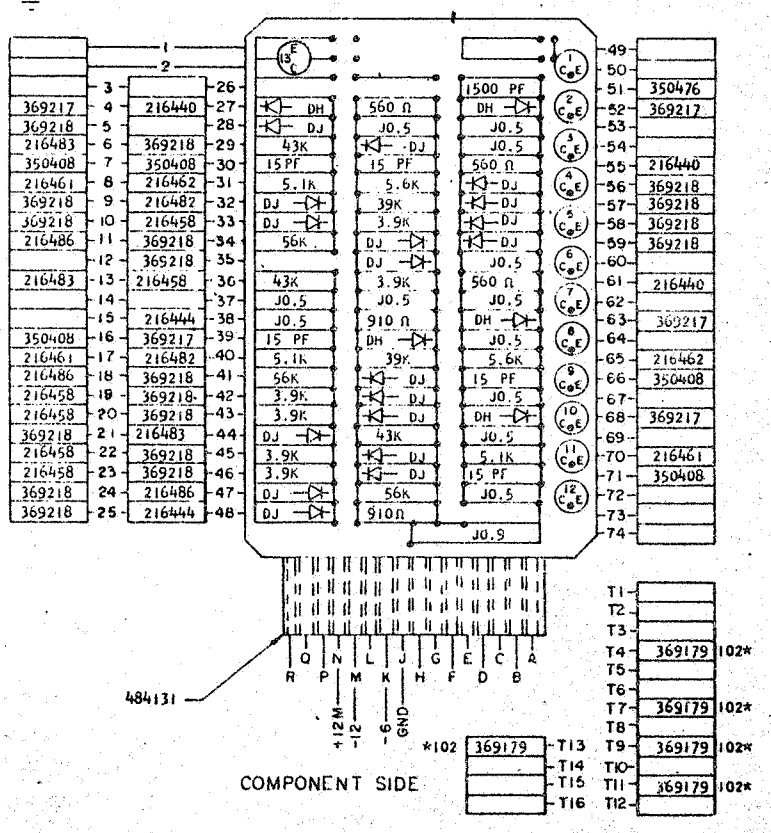
1. THE FIRST LEVEL OF DIODES OF BOTH T11 AND T7 PERFORM A NEGATIVE AND AND THE SECOND LEVEL OF DIODES A NEGATIVE OR FUNCTION. T9 AND T4 ARE HIGH SPEED INVERTERS THAT ACCEPT NEGATIVE INPUTS TO PERFORM A NEGATIVE AND INVERT FUNCTION. THESE TRANSISTORS ARE DRIVEN BY T11 AND T7 RESPECTIVELY. THE OUTPUTS OF T11, T7, T9 AND T4 ARE FED INTO T13 WHOSE FIRST LEVEL OF DIODES PERFORM A NEGATIVE AND AND WHOSE SECOND LEVEL PERFORM A NEGATIVE OR FUNCTION. THIS CIRCUIT IS USED TO CHECK FOR ODD PARITY OF A TAPE CHARACTER. T11 AND T7 ARE EXCLUSIVE OR'S THAT EACH DETERMINE IF TWO BITS ARE ODD OR EVEN PARITY AND THEN T13, ANOTHER EXCLUSIVE OR COMPARES THE OUTPUTS OF T11 AND 17 TO DETERMINE IF ALL FOUR BITS ARE ODD OR EVEN PARITY.

2. THE CARD CODES SHOWN IN THE BLOCKS REFER TO INDIVIDUAL CARDS SIMILAR TO THAT PORTION OF CIRCUITRY.

3. DELAY - NSEC

INPUTS TO OUTPUT:	MIN.	MAX.
TURN ON	32	263
TURN OFF	27	213

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
P R, C,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,Q, D,E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SDTDL					-62	115599					729928
	MUP NUMBER 4											
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

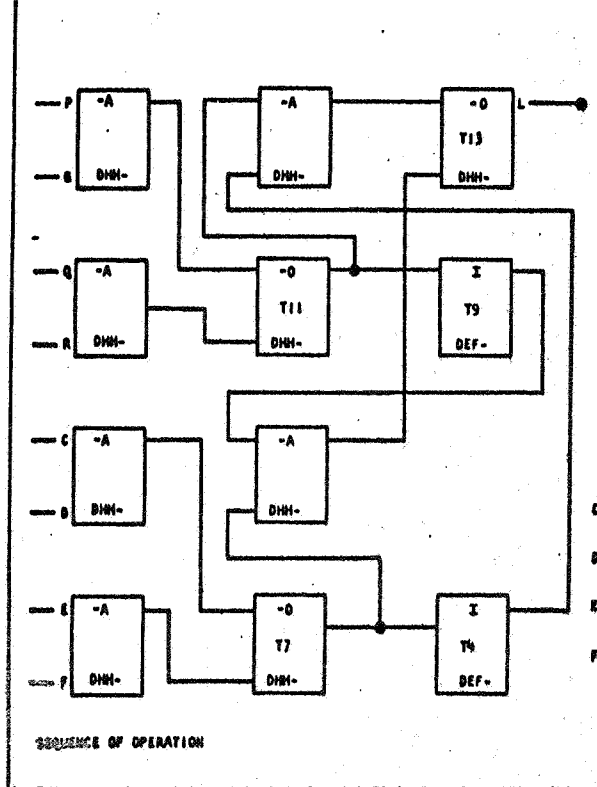
C

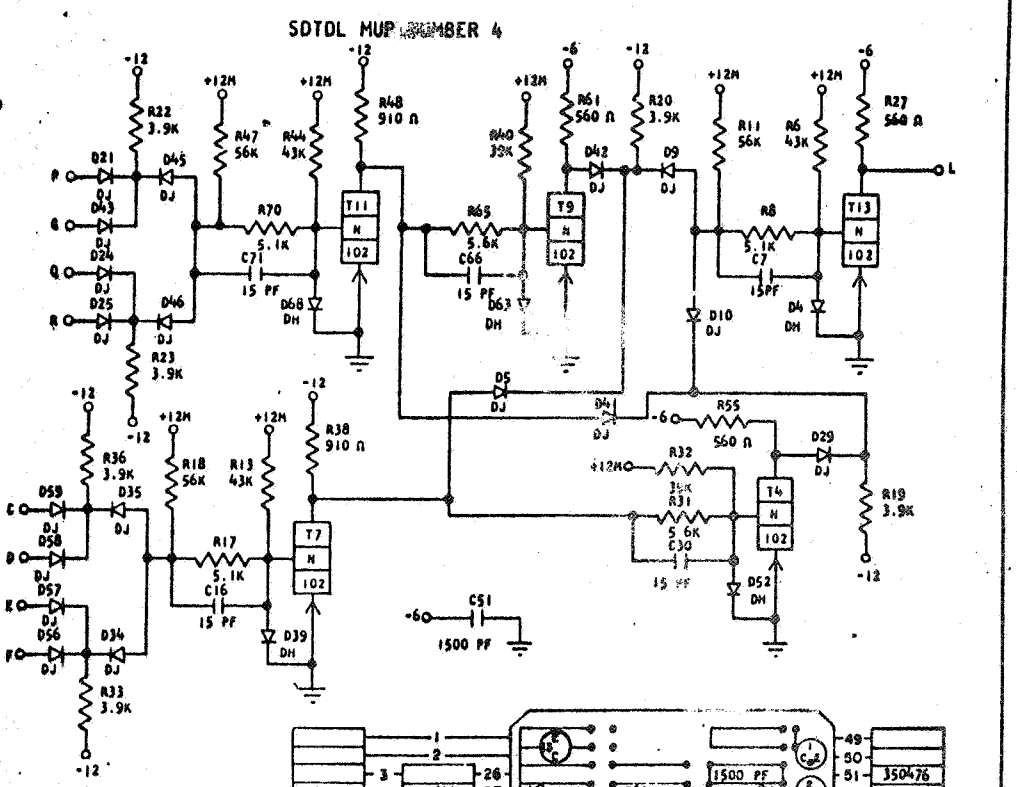
729928 STANDARDS CODE

CARD CODE 729928
D H J -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370352





SEQUENCE OF OPERATION

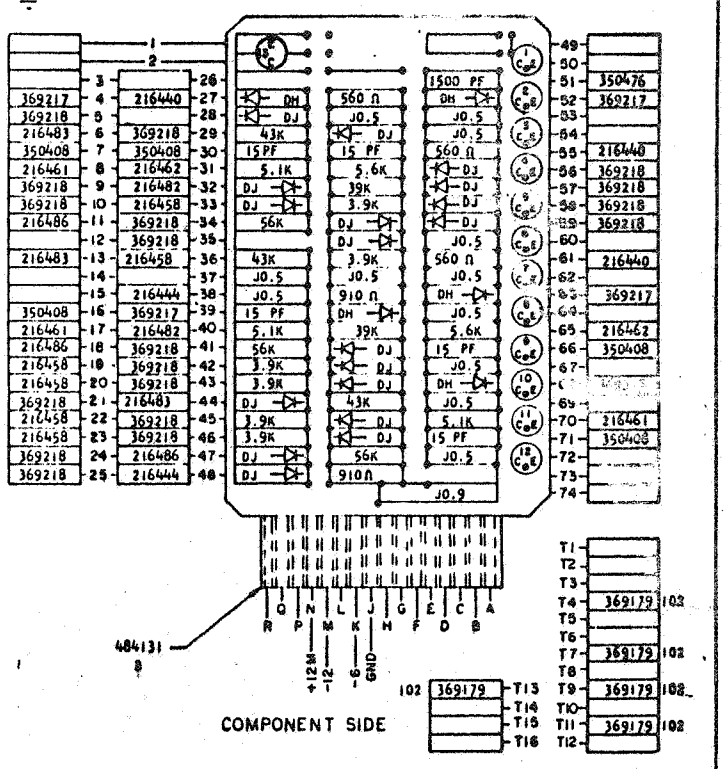
1. THE FIRST LEVEL OF DIODES OF BOTH T11 AND T7 PERFORM A NEGATIVE AND AND THE SECOND LEVEL OF DIODES A NEGATIVE OR FUNCTION. T9 AND T4 ARE HIGH SPEED INVERTERS THAT ACCEPT NEGATIVE INPUTS TO PERFORM A NEGATIVE AND INVERT FUNCTION. THESE TRANSISTORS ARE DRIVEN BY T11 AND T7 RESPECTIVELY. THE OUTPUTS OF T11, T7, T9 AND T4 ARE FED INTO T13 WHOSE FIRST LEVEL OF DIODES PERFORM A NEGATIVE AND AND WHOSE SECOND LEVEL PERFORM A NEGATIVE OR FUNCTION. THIS CIRCUIT IS USED TO CHECK FOR ODD PARITY OF A TAPE CHARACTER. T11 AND T7 ARE EXCLUSIVE OR'S THAT EACH DETERMINE IF TWO BITS ARE ODD OR EVEN PARITY AND THEN T13, ANOTHER EXCLUSIVE OR COMPARES THE OUTPUTS OF T11 AND T7 TO DETERMINE IF ALL FOUR BITS ARE ODD OR EVEN PARITY.

2. THE CARD CODES SHOWN IN THE BLOCKS REFER TO INDIVIDUAL CARDS SIMILAR TO THAT PORTION OF CIRCUITRY.

3. DELAY - NSEC

INPUTS TO OUTPUT:	MIN.	MAX.
TURN ON	32	263
TURN OFF	27	213

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
P,R, C,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
S,Q, D,E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
	Y			UP	-.65	-.1
				DOWN	-5.81	-8.8



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729928
NAME	CARD ASM TSTR - SDTDL MUP NUMBER 4				-/-/-62	115599						
DESIGN			MODEL	SMS	12-18-62	EC116055						
DETAIL	RQ	3-1-62	SCALE	NONE	30.4.63	JT83687						
CHECK	WH	3-1-62	DRAW CHECK	LIG 3-7-62								
APPROV												

C

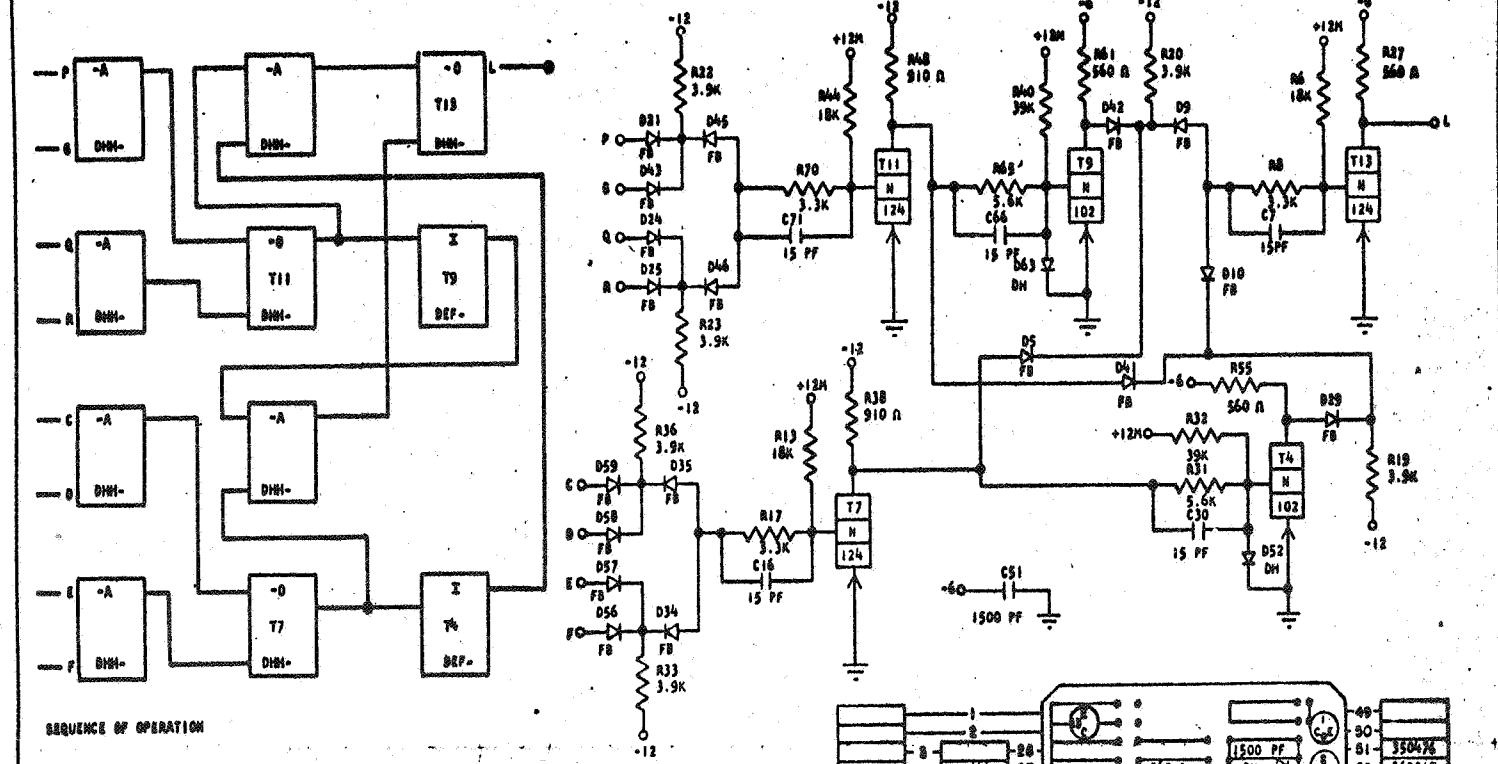
729928 | STANDARDS CODE

CARD CODE 729928 | D H J -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370352

SDTDL MUP NUMBER 4



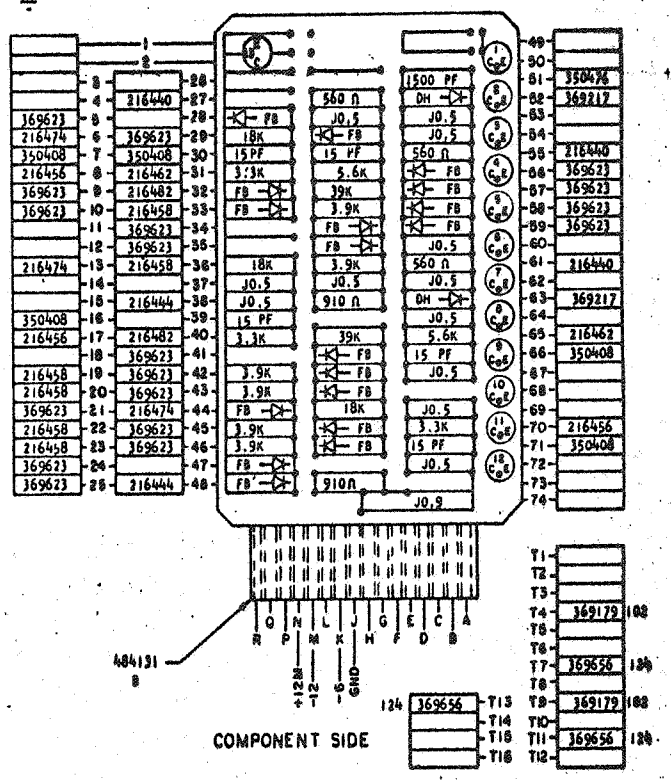
1. THE FIRST LEVEL OF DIODES OF BOTH T11 AND T7 PERFORM A NEGATIVE AND AND THE SECOND LEVEL OF DIODES A NEGATIVE OR FUNCTION. T9 AND T4 ARE HIGH SPEED INVERTERS THAT ACCEPT NEGATIVE INPUTS TO PERFORM A NEGATIVE AND INVERT FUNCTION. THESE TRANSISTORS ARE DRIVEN BY T11 AND T7 RESPECTIVELY. THE OUTPUTS OF T11, T7, T9 AND T4 ARE FED INTO T13 WHOSE FIRST LEVEL OF DIODES PERFORM A NEGATIVE AND AND WHOSE SECOND LEVEL PERFORM A NEGATIVE OR FUNCTION. THIS CIRCUIT IS USED TO CHECK FOR ODD PARITY OF A TAPE CHARACTER. T11 AND T7 ARE EXCLUSIVE OR'S THAT EACH DETERMINE IF TWO BITS ARE ODD OR EVEN PARITY AND THEN T13, ANOTHER EXCLUSIVE OR COMPARES THE OUTPUTS OF T11 AND T7 TO DETERMINE IF ALL FOUR BITS ARE ODD OR EVEN PARITY.

2. THE CARD CODES SHOWN IN THE BLOCKS REFER TO INDIVIDUAL CARDS SIMILAR TO THAT PORTION OF CIRCUITRY.

3. DELAY = NSEC

INPUTS TO OUTPUT:	MIN.	MAX.
TURN ON	32	263
TURN OFF	27	213

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
P,R, C,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,Q, B,E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SDTDL MUP NUMBER 4					6-29-62	115599					729928
DESIGN			MODEL	SMS		12-18-62	116055					
DETAIL	RQ	3-1-62	SCALE	NONE		4-10-63	116155					
CHECK	WH	3-1-62	DRAW	LIG	3-7-62							
APPRO			CHK'R									

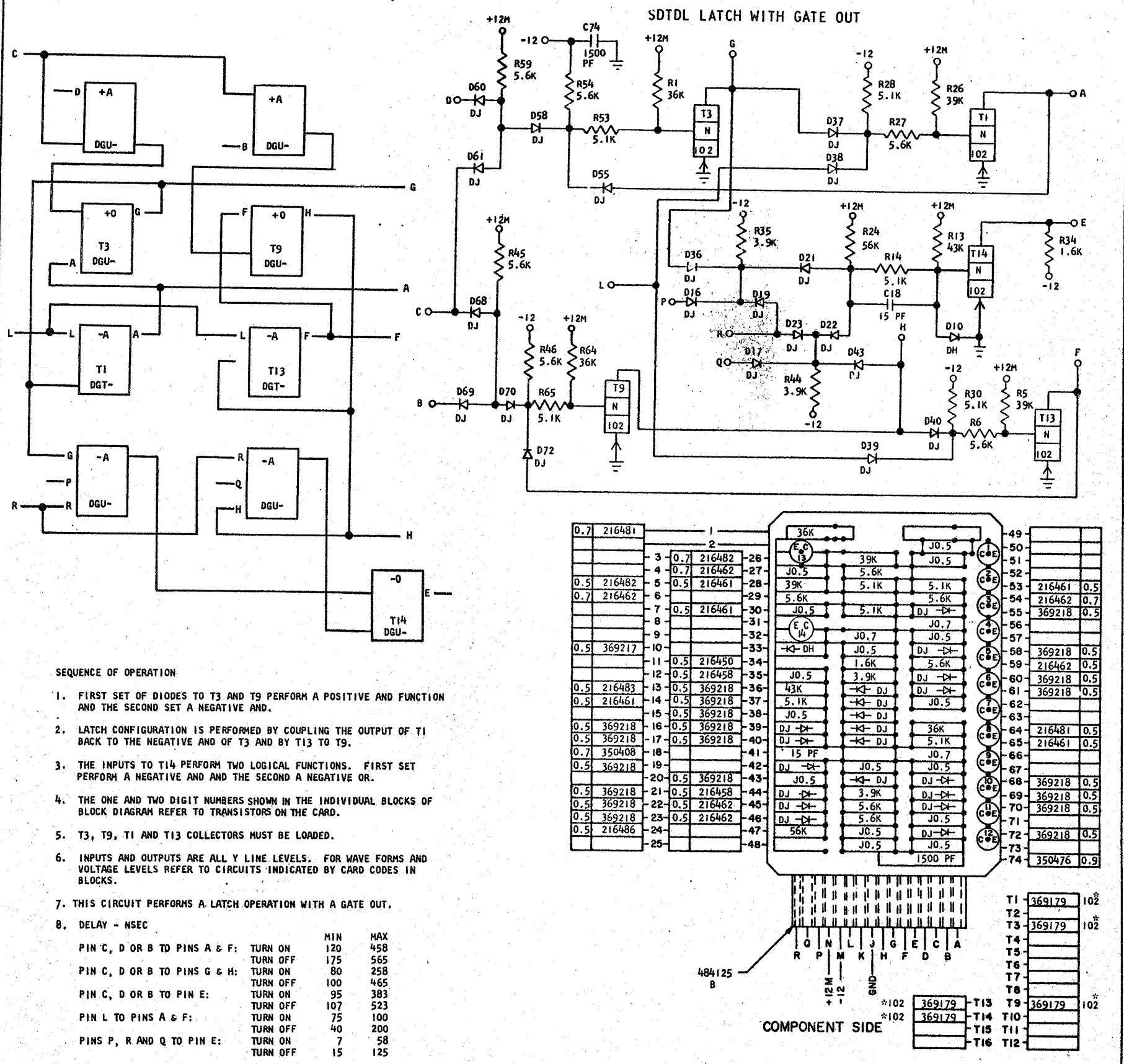
C

729929 | STANDARDS CODE

CARD CODE 729929
DHK-

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370349



SEQUENCE OF OPERATION

1. FIRST SET OF DIODES TO T3 AND T9 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
2. LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF TI BACK TO THE NEGATIVE AND OF T3 AND BY T13 TO T9.
3. THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
4. THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
5. T3, T9, TI AND T13 COLLECTORS MUST BE LOADED.
6. INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
7. THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
8. DELAY - NSEC

		MIN	MAX
PIN C, D OR B TO PINS A & F:	TURN ON	120	458
	TURN OFF	175	565
PIN C, D OR B TO PINS G & H:	TURN ON	80	258
	TURN OFF	100	465
PIN C, D OR B TO PIN E:	TURN ON	95	383
	TURN OFF	107	523
PIN L TO PINS A & F:	TURN ON	75	100
	TURN OFF	40	200
PINS P, R AND Q TO PIN E:	TURN ON	7	58
	TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL LATCH WITH GATE OUT				2-27-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729929

C

729929

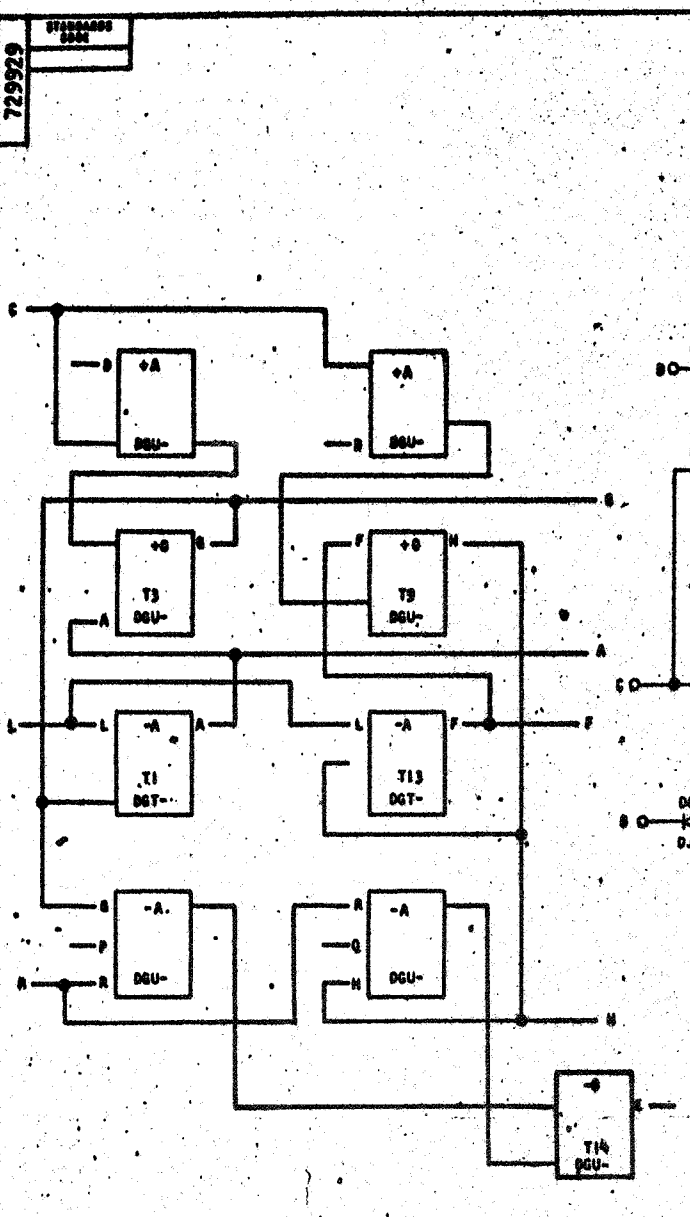
729929

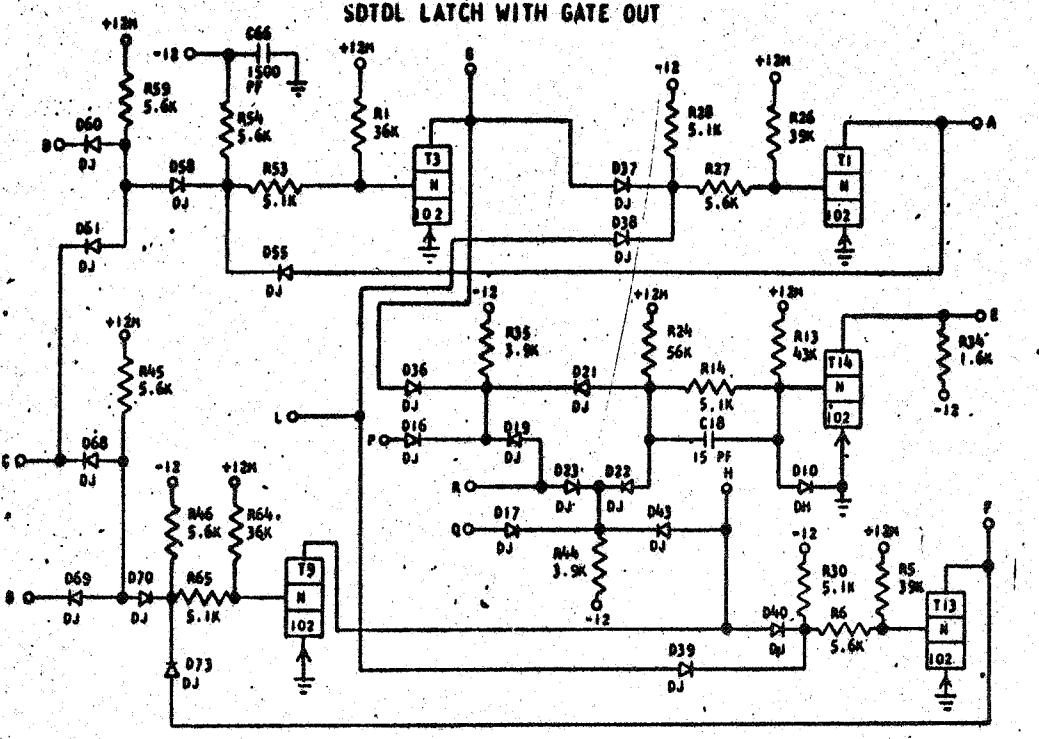
DHK -

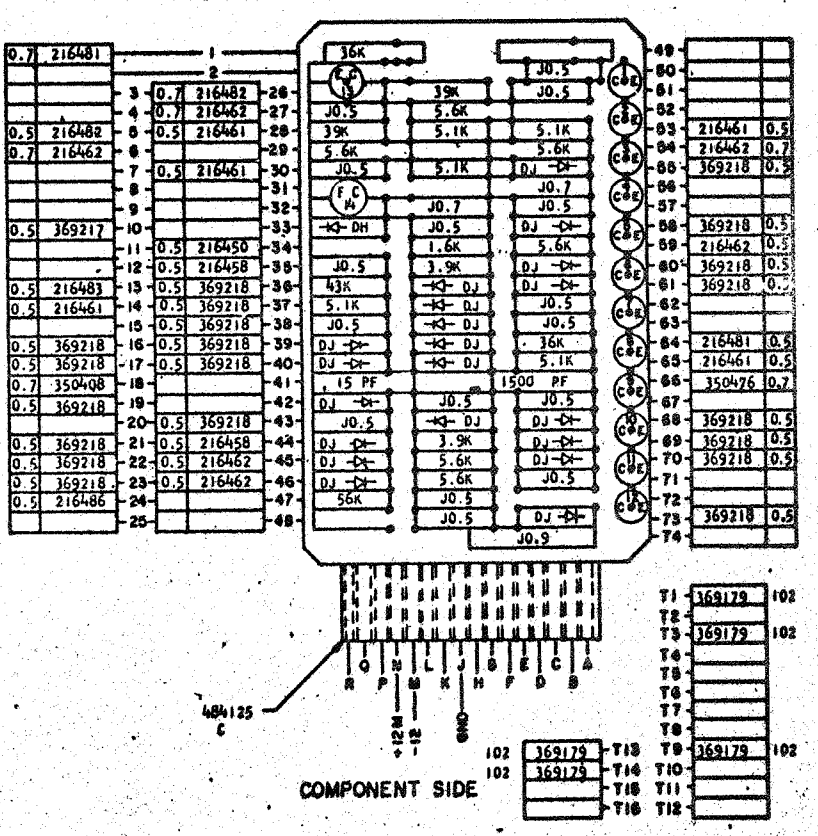
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370349

SDTDL LATCH WITH GATE OUT







SEQUENCE OF OPERATION

1. FIRST SET OF DIODES TO T3 AND T9 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
2. LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF T1 BACK TO THE NEGATIVE AND OF T3 AND BY T13 TO T9.
3. THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
4. THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
5. T3, T9, T1 AND T13 COLLECTORS MUST BE LOADED.
6. INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
7. THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
8. DELAY - NSEC

		MIN	MAX
PIN C, B OR B TO PINS A & F:	TURN ON	120	458
	TURN OFF	175	565
PIN C, B OR B TO PINS G & H:	TURN ON	80	258
	TURN OFF	100	465
PIN C, B OR B TO PIN E:	TURN ON	95	383
	TURN OFF	107	523
PIN L TO PINS A & F:	TURN ON	75	100
	TURN OFF	40	200
PINS P, R AND Q TO PIN E:	TURN ON	7	58
	TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729929
NAME	CARD ASM TSTR-SDTDL LATCH WITH GATE OUT					2-19-62	115599						
				MODEL	SMS	1-3-63	EC 116034						
DESIGN				SCALE	NONE	30-4-63	JT 83687						
DETAIL	RQ	3-1-62		DRAW	LIG 3-17-62								
CHECK	WH	3-1-62		CHECK									
APPRD													

C

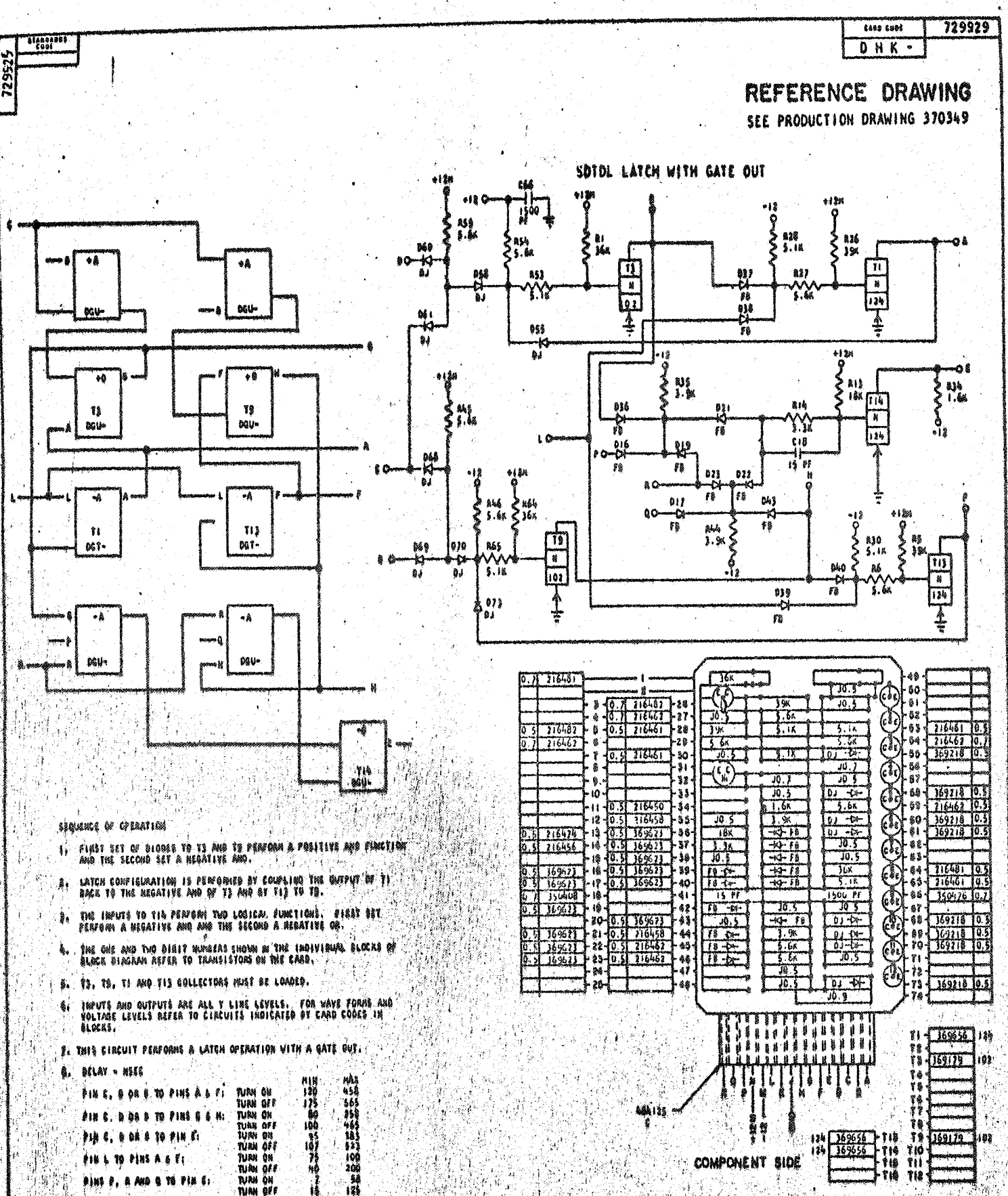
729525

CARD CODE 729929

DHK -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370349



SEQUENCE OF OPERATION

1. FIRST SET OF BLOCKS TO T3 AND T8 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
2. LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF T1 BACK TO THE NEGATIVE AND OF T3 AND BY T13 TO T8.
3. THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
4. THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
5. T3, T8, T1 AND T13 COLLECTORS MUST BE LOADED.
6. INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORM AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
7. THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
8. DELAY - NSEC

		MIN	MAX
PIN E, B OR B TO PINS A & F:	TURN ON	120	458
	TURN OFF	175	565
PIN G, B OR B TO PINS G & H:	TURN ON	80	358
	TURN OFF	100	465
PIN G, B OR B TO PIN F:	TURN ON	95	183
	TURN OFF	167	523
PIN L TO PINS A & F:	TURN ON	75	100
	TURN OFF	90	200
PINS P, R AND Q TO PIN G:	TURN ON	2	58
	TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVED	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME KAMS ASM TSTG-SDTDL LATCH WITH GATE OUT	7-19-62	115599					
	8-3-63	116034					
DESIGN RG 7-1-62	8-10-63	116186					
CHECK WS 7-1-62							
APPD							

729929

C

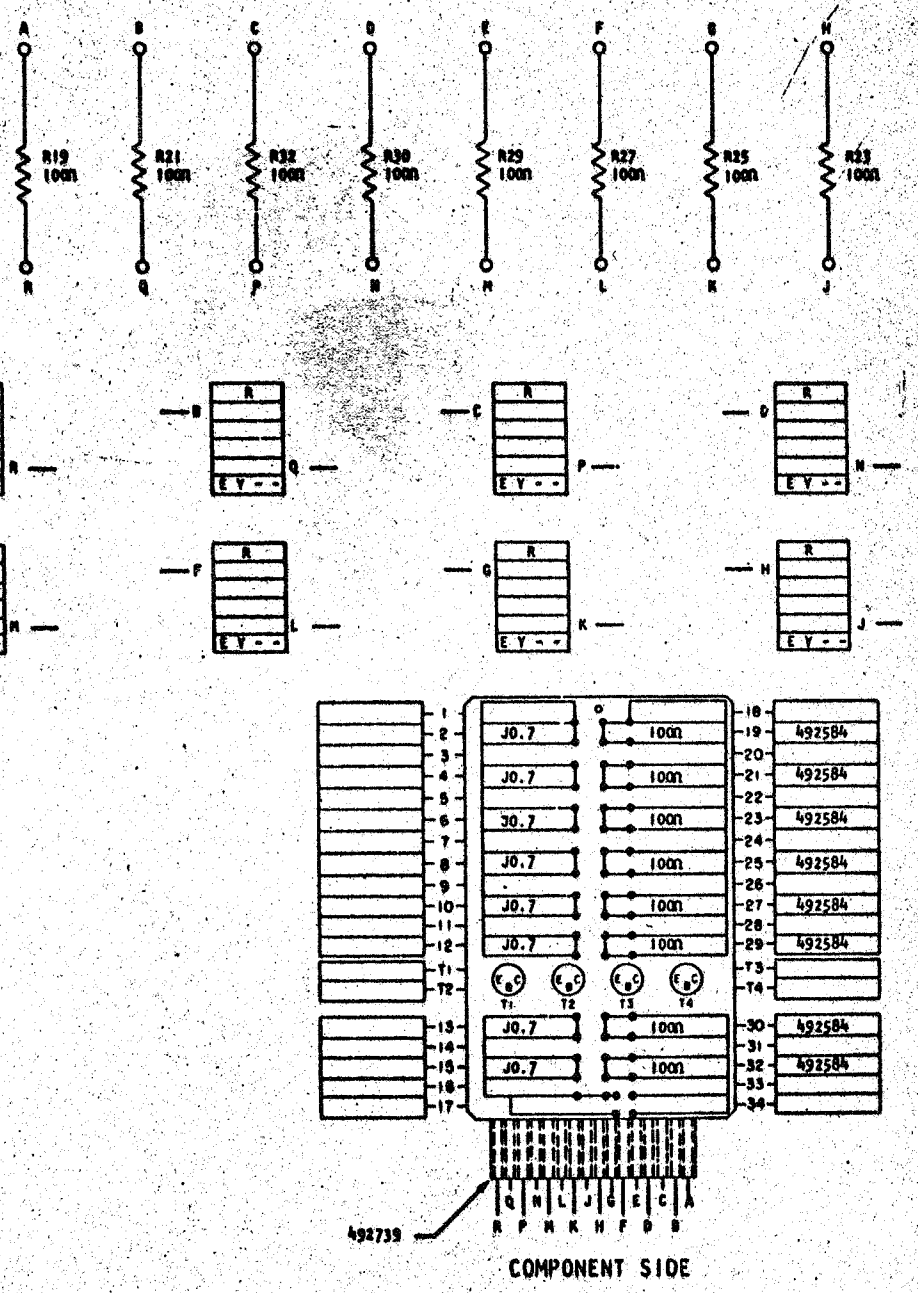
729930 | STANDARDS CODE

CARD CODE 729930
EY --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371199

DRIFT-DRIVER, RESISTOR



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - DRIFT-DRIVER, RESISTOR		MODEL	SMS	4-27-62	EC 115599					
DESIGN					10.4.63	JT 83687					
DETAIL	RO	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729930

C

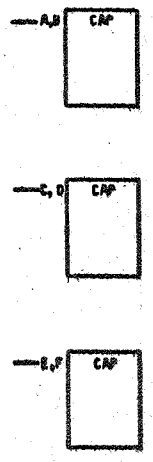
729931 | STANDARDS CODE

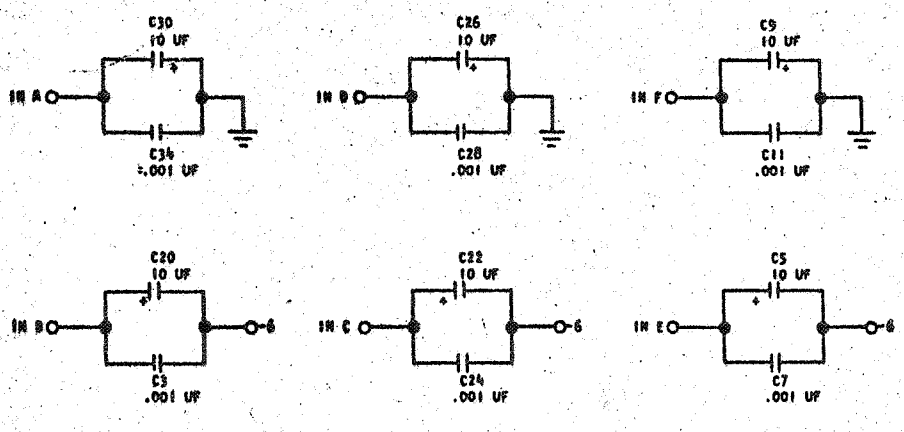
CARD CODE 729931
GK --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371533

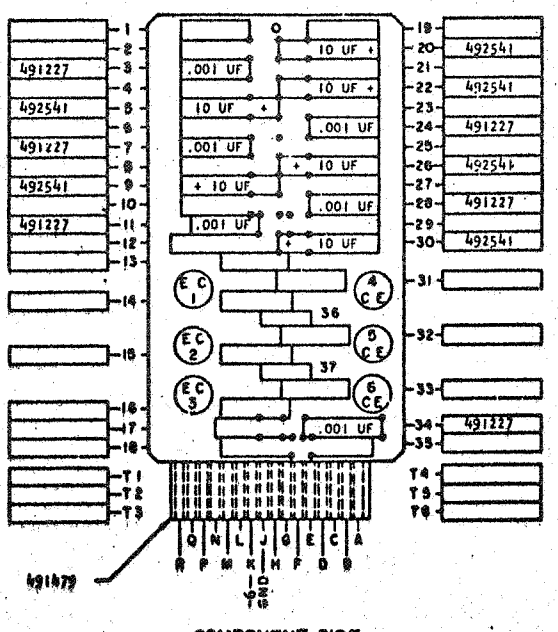
CABLE DE COUPLE CARD





SEQUENCE OF OPERATION

1. CARD DECOUPLES THE NEUTRAL WIRE OF A TWISTED PAIR OR THE SHIELD OF A COAXIAL CABLE



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CABLE DE COUPLE CARD				6-19-63	EC 115599					729931
DESIGN			MODEL	SMS	30.4.63	JT 83687					
DETAIL	AQ	5-1-62	SCALE	NONE							
CHECK	WH	5-1-62	DRAW	LIB 5-17-62							
APPRD			CHECK								

C

STANDARDS CODE 729932

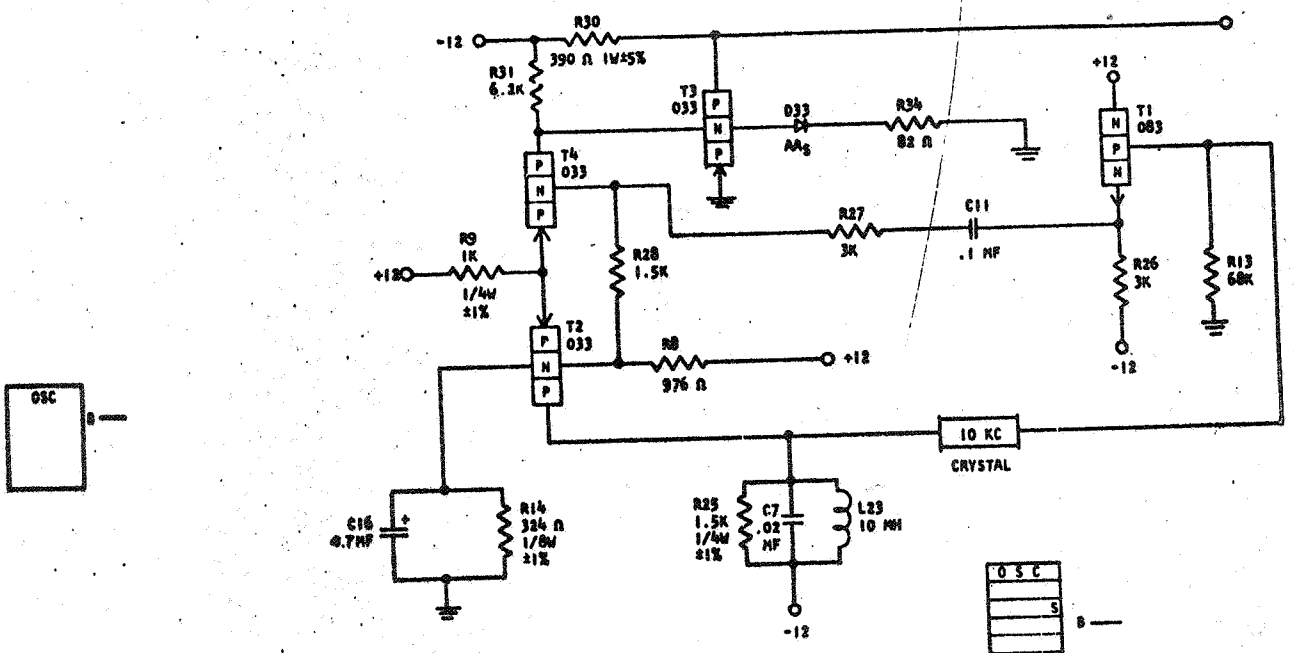
CARD CODE 729932

JB --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371245

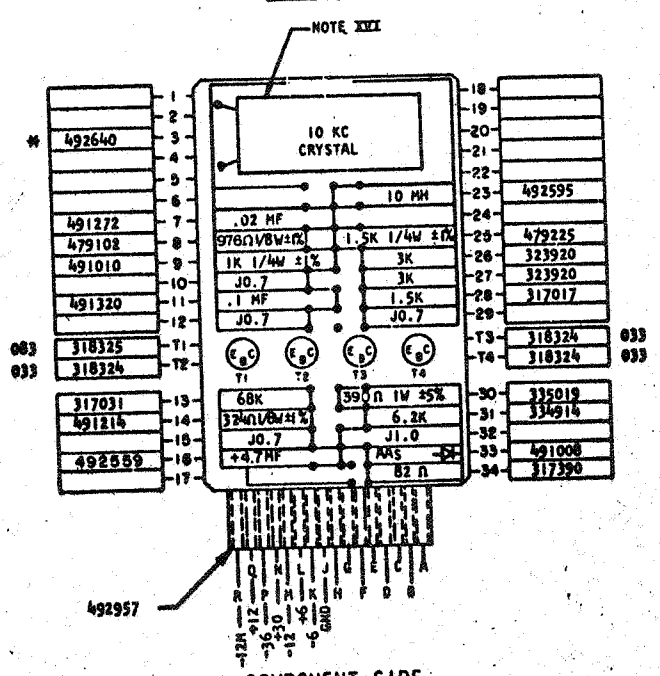
CTRL-OSCILLATOR, 10 KC FREE RUNNING (CRYSTAL)



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, OSCILLATOR TURNS ON

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B	S	OUTPUT	10 KC	UP	0	-.2
				DOWN	-11.8	-12.12



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - CTRL OSC. 10KC FREE RUNNING CRYSTAL					6-27-62	EC 115599					
			MODEL	SMS	10.4.63	JT 83687					
DESIGN			SCALE	NONE							
DETAIL RQ	3-1-62		DRAW	LIG 3-17-62							
CHECK WH	3-1-62		CHECK								
APPRO											

729932

C

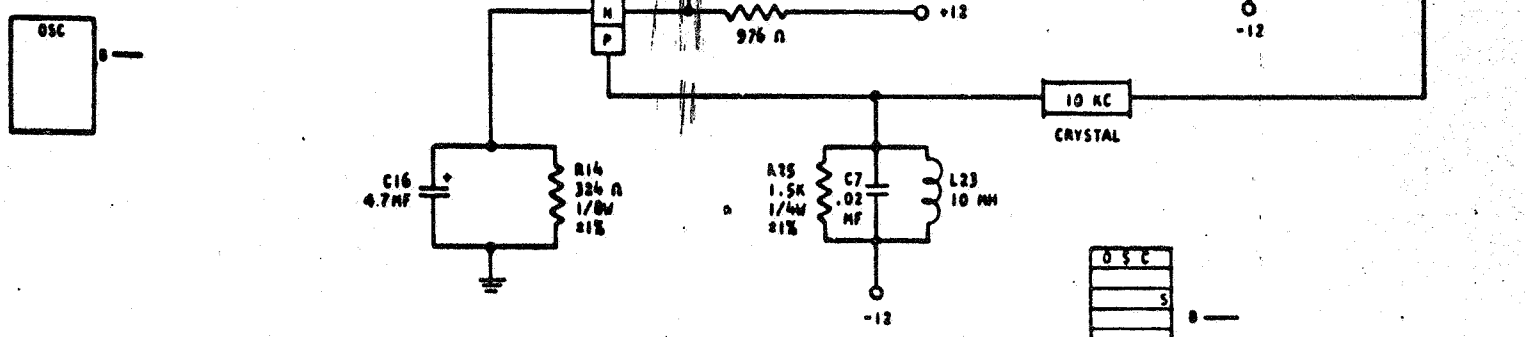
729932 | STANDARDS CODE

CARD CODE	729932
JB - -	

REFERENCE DRAWING

SLT PRODUCTION DRAWING 371245

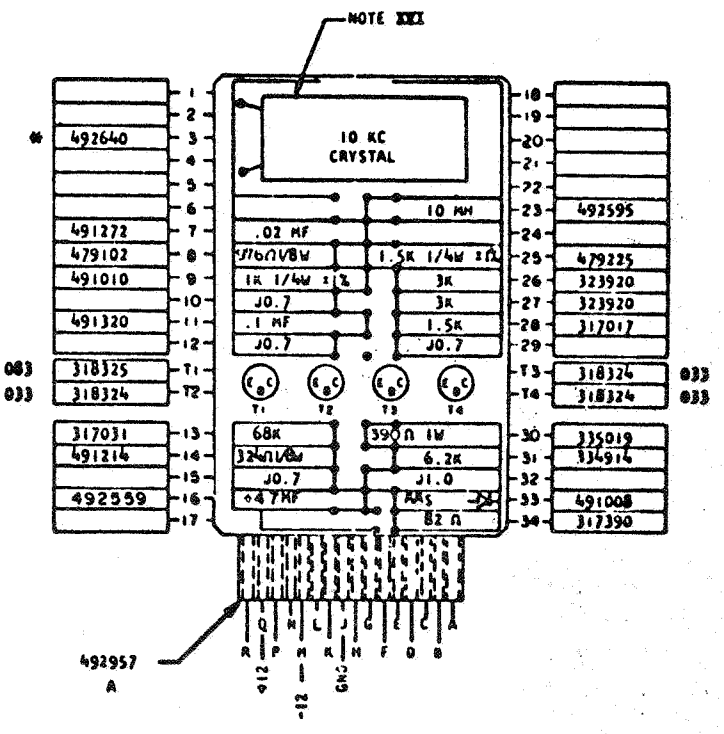
CTRL-OSCILLATOR, 10 KC FREE RUNNING (CRYSTAL)



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, OSCILLATOR TURNS ON

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B	S	OUTPUT	10 KC	UP	0	-.2
				DOWN	-11.8	-12.12



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO
NAME	CARD ASM TSTR - CTRL OSC, 10KC FREE RUNNING CRYSTAL		MODEL	SMS	6-7-62	115599					
DESIGN					8-28-63	117802					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WM	3-1-62	DRAW	LIG 3-17-62							
APPRD			CHECK								

C

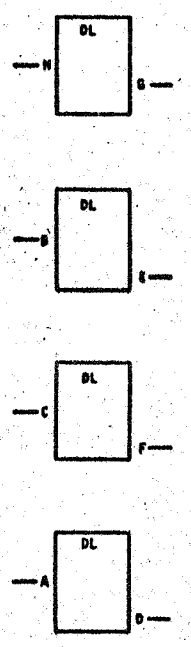
729933 | STANDARDS CODE

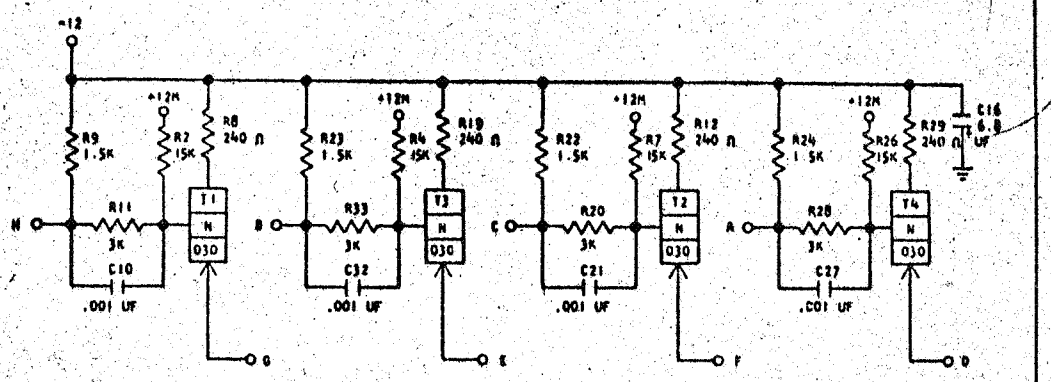
CARD CODE 729933
TAB -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370066

SDTRL 93Ω COAX LINE DRIVER-DISPERSED LOADS





SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT DOWN
2. INPUT UP TRANSISTOR OFF OUTPUT UP

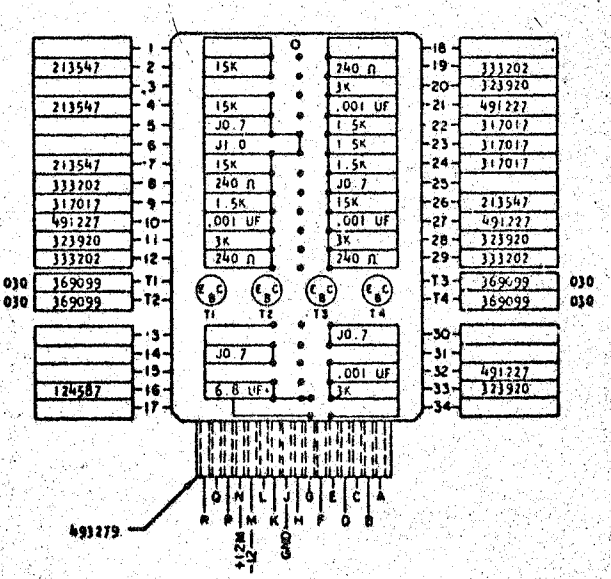
PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
H,B, C,A	S	INPUT		UP	-.6	0
				DOWN	-1.14	-8.15
G,E, F,D	N	OUTPUT		UP	+0.8	
				DOWN	-0.8	
G,E, F,D	R	OUTPUT		UP	12.	
				DOWN	0.0	

DELAY - NSEC - DISPERSED LOADS:

	MINIMUM	MAXIMUM
TURN ON	10	40
TURN OFF	0	10

DELAY - NSEC - "DOT-ORING"

	MINIMUM	MAXIMUM
TURN ON	16	52
TURN OFF	0	10



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL 93 Ω					6 Jy -62	EC 115599					
	COAX LINE DRIVER-DISPERSED LOADS					30.4.63	TT 83687					
DESIGN				MODEL	SMS							
DETAIL	RG	3-1-62		SCALE	NONE							
CHECK	WH	3-1-62		DRAW	LIG	3-17-62						
APPRO				CHECK								

729933

C

83687

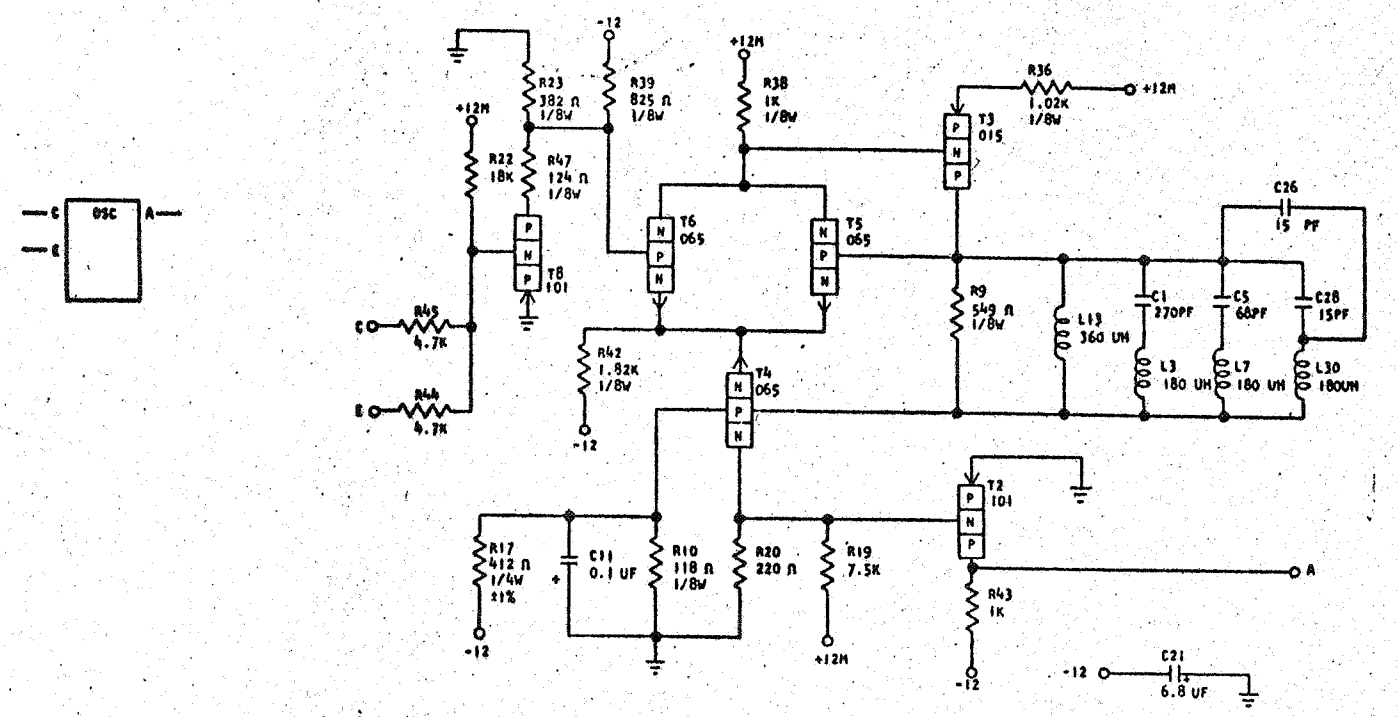
729934 STANDARDS CODE

CARD CODE 729934
T B G -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370296

SDTRL - OSCILLATOR, 320 KC S LINE GATED



SEQUENCE OF OPERATION

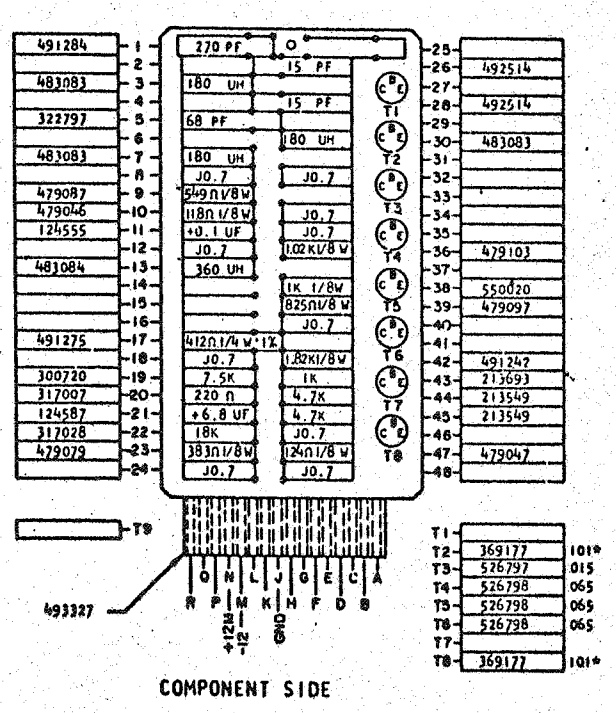
1. WHEN C AND E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E ARE DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	100
TURN OFF*	160	200
RISE TIME	52	66
FALL TIME	42	60

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-SDTRL OSC 320 KC S LINE GATED				6-11-62	EC 115599						729934
DESIGN			MODEL	SMS	30.4.63	JT 83687						
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WM	3-1-62	DRAW	LIG 3-17-62								
APPRO			CHECK									

C

729935 STANDARDS CODE

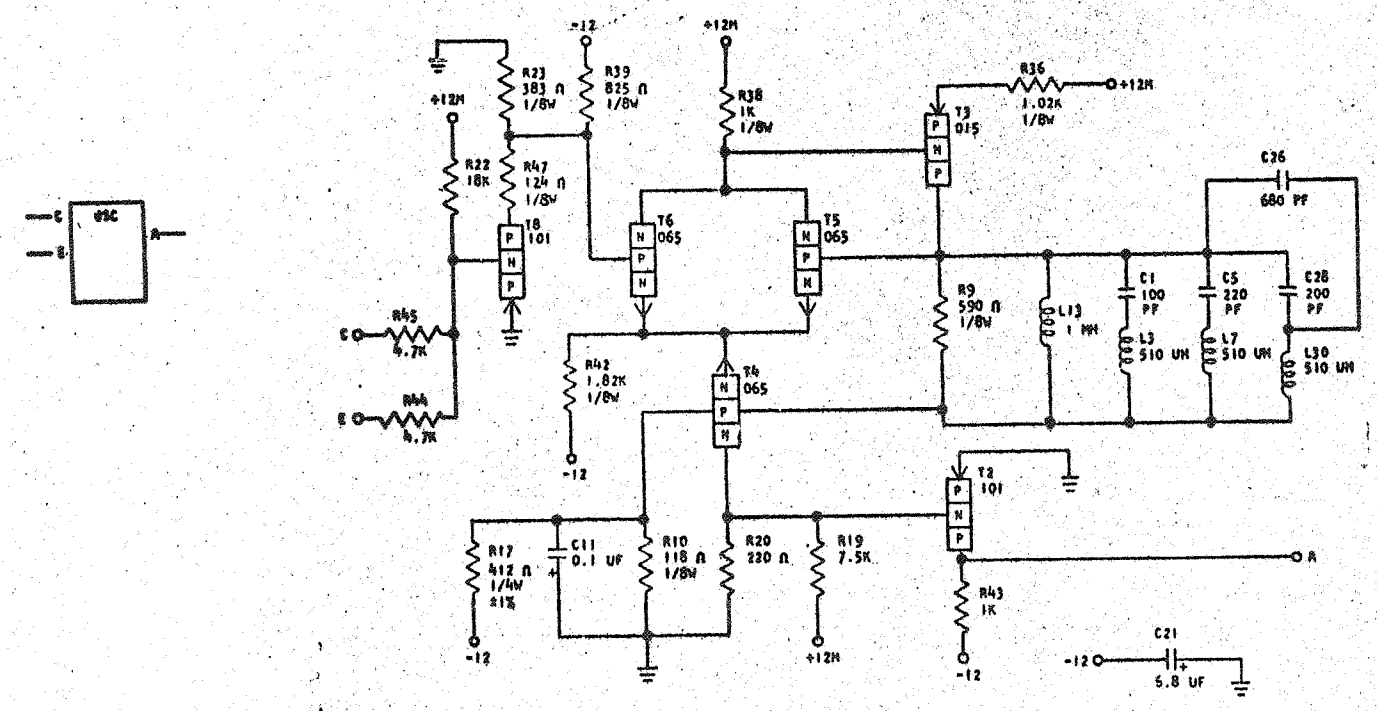
CARD CODE 729935

T B Q -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370295

SDTRL - OSCILLATOR, 115 KC S LINE GATED



SEQUENCE OF OPERATION

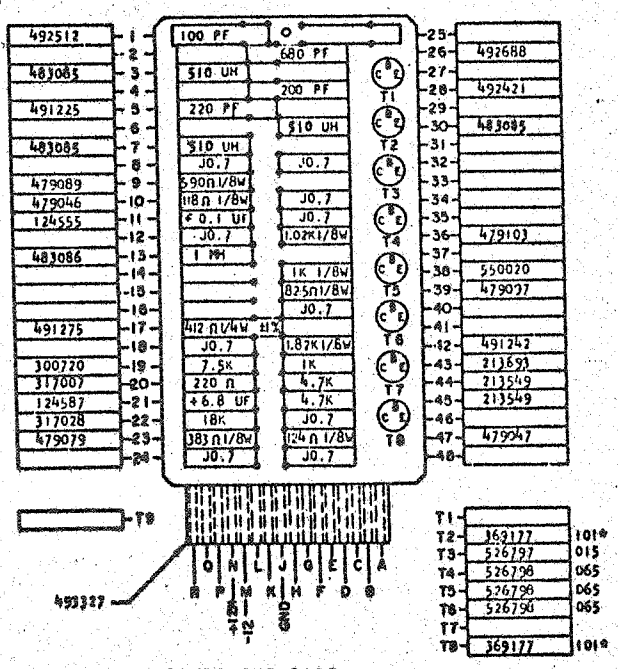
1. WHEN C AND E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	115 KC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	60	130
TURN OFF*	110	190
RISE TIME	28	82
FALL TIME	21	58

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL-OSC, 115 KC S LINE GATED				4-27-62	EC 115599					
DESIGN			MODEL	SMS	30.4.63	TT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRD			CHECK								

729935

C

729935

STANDARDS CODE 729936

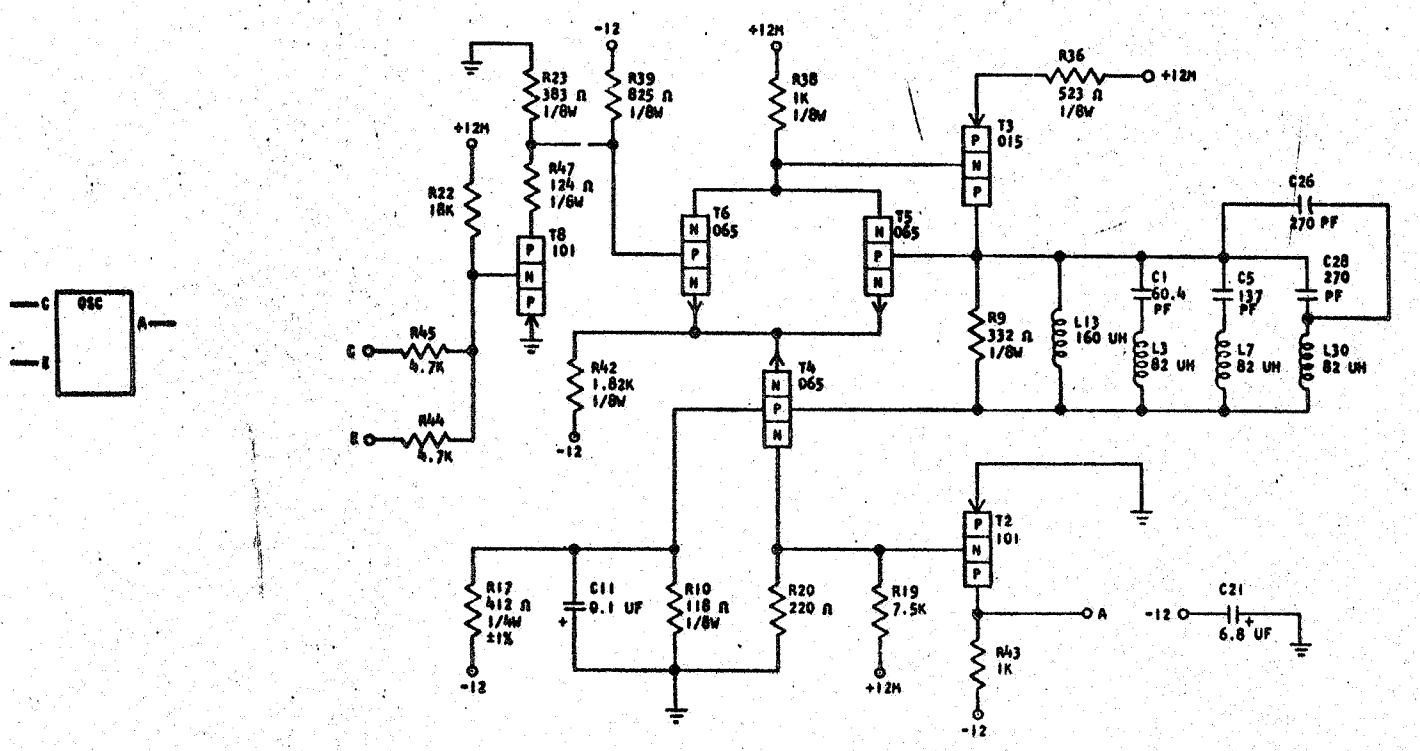
CARD CODE 729936

T B R -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370297

SDTRL - OSCILLATOR, 360 KC S LINE GATED



SEQUENCE OF OPERATION

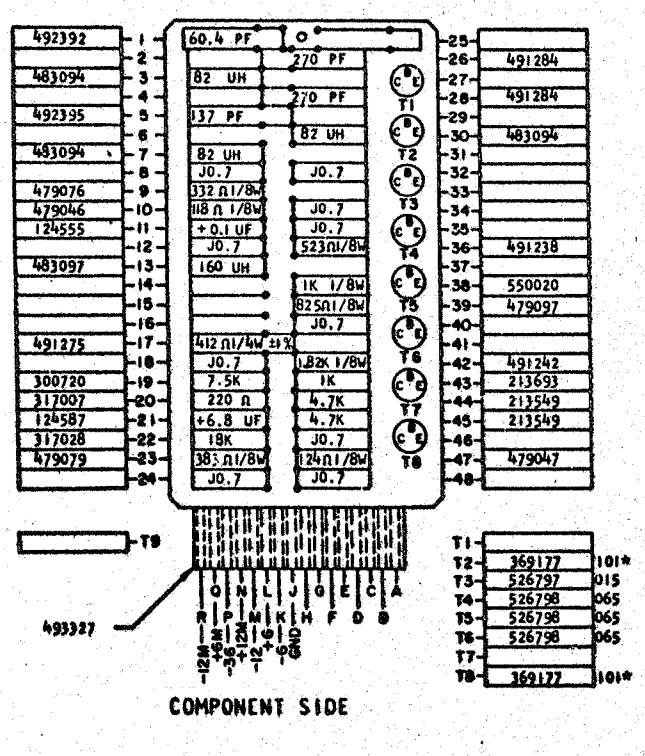
1. WHEN C AND E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	360 KC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	110
TURN OFF*	160	200
RISE TIME	28	52
FALL TIME	46	54

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL-OSC. 360 KC S LINE GATED					6-29-62	EC 115599					
				MODEL	SMS	30.4.63	JT 83697					
DESIGN												
DETAIL	RO	3-1-62	SCALE	NONE								
CHECK	WHS	3-1-62	DRAW	LJG	3-17-62							
APPRO			CHECK									

729936

C

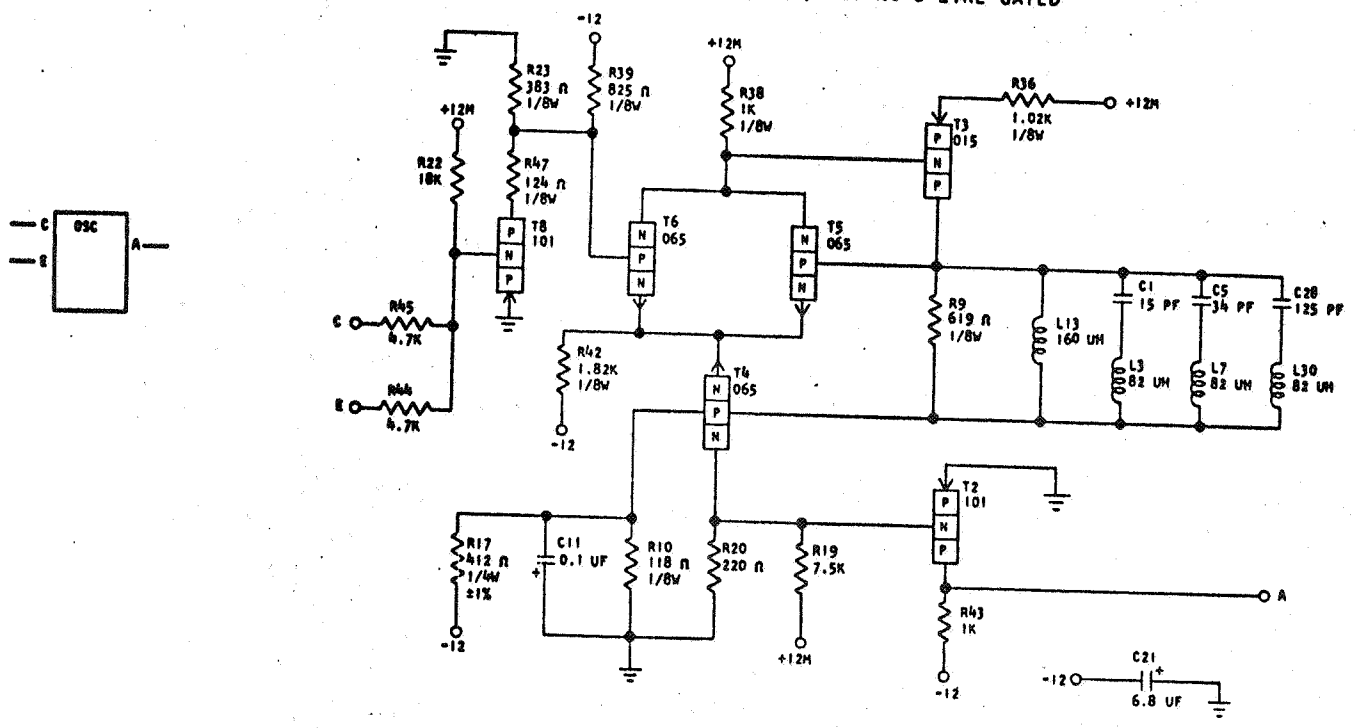
729937 | STANDARDS CODE

CARD CODE | 729937
T B S -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370298

SDTRL - OSCILLATOR, 667 KC S LINE GATED



SEQUENCE OF OPERATION

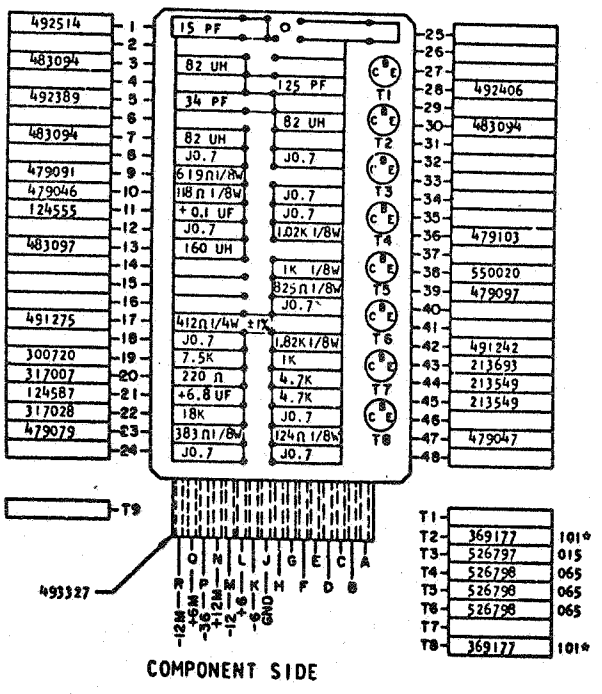
1. WHEN C AND E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	667 KC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	110
TURN OFF*	160	200
RISE TIME	36	52
FALL TIME	48	62

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL-OSC, 667 KC S LINE GATED				6-29-62	EC 115599					
DESIGN			MODEL	SMS	30.4.63	JT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WN	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

729937

729938 STANDARD COST

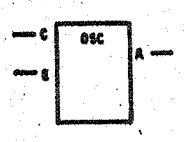
CARD CODE 729938

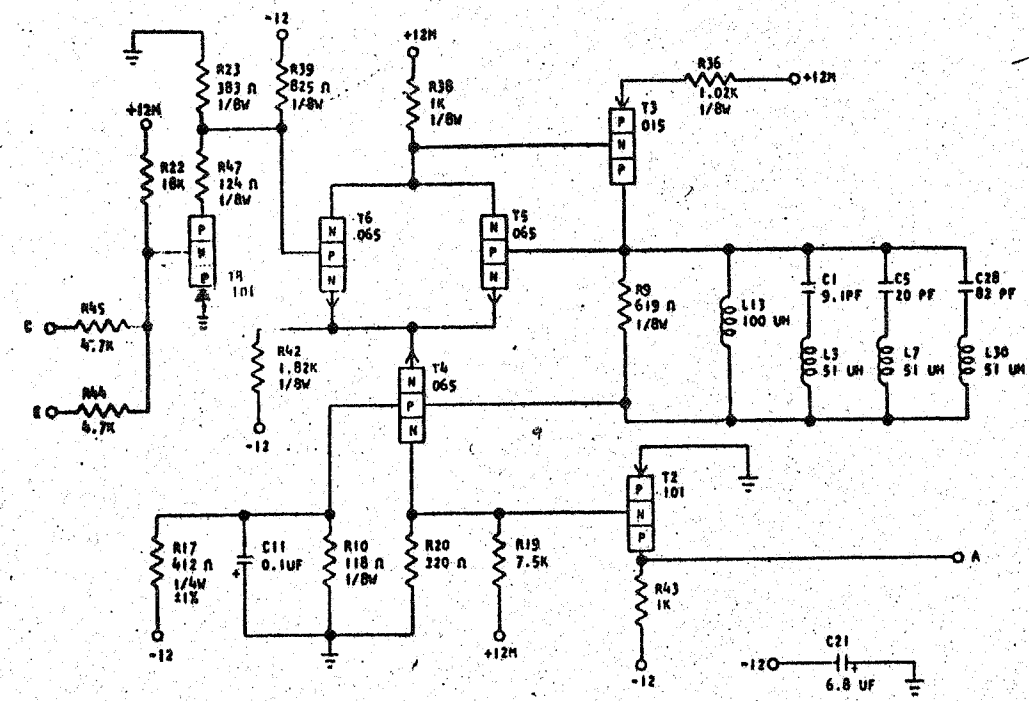
T B V -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370299

SDTRL - OSCILLATOR, I MC S LINE GATED





SEQUENCE OF OPERATION

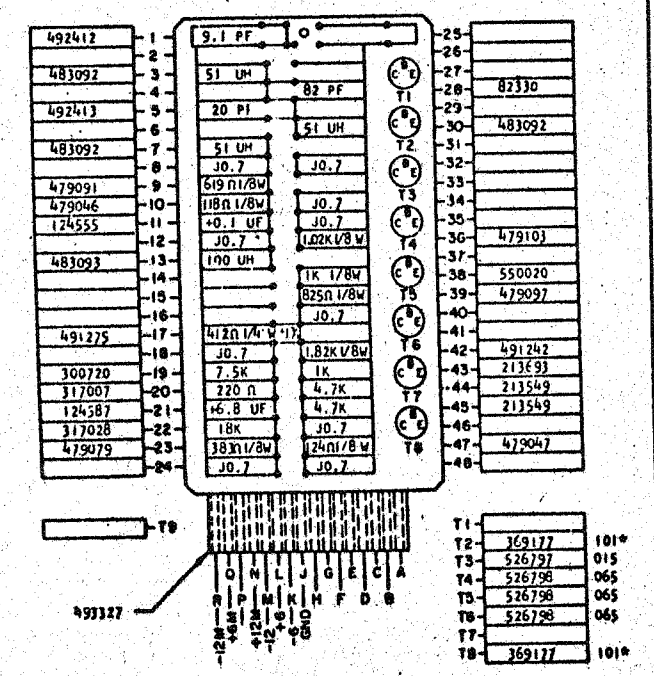
1. WHEN C & E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	1MC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	120
TURN OFF*	80	200
RISE TIME	52	110
FALL TIME	42	220

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC.	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD [illegible] DIFL-BSC.	4-29-62	EC 185329					729938
I MC S LINE	30.4.63	ET 83687					
DESIGN							
DETAIL RO 3-1							
CHECK WH 3-1-62 APPD							
APPRD CHECK							

C

729938

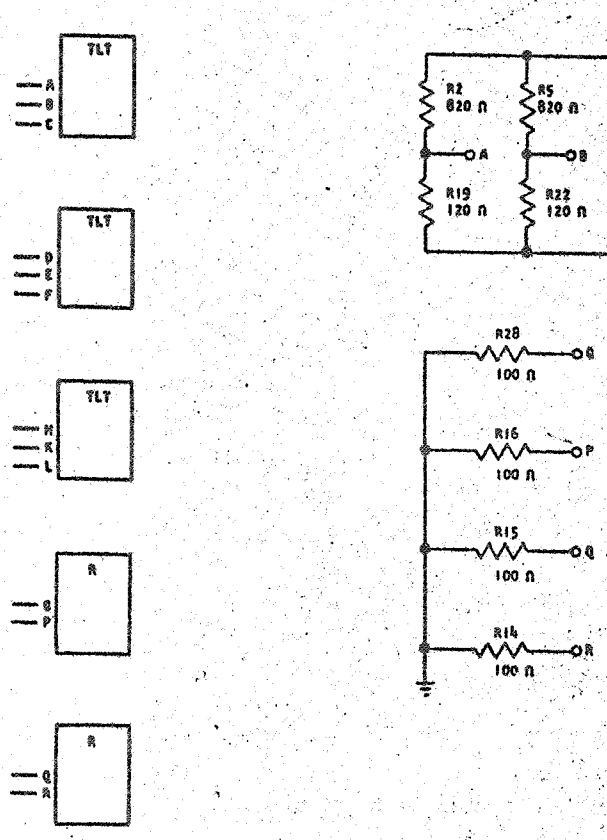
729939 STANDARDS CODE

CARD CODE 729939
T C K -

REFERENCE DRAWING

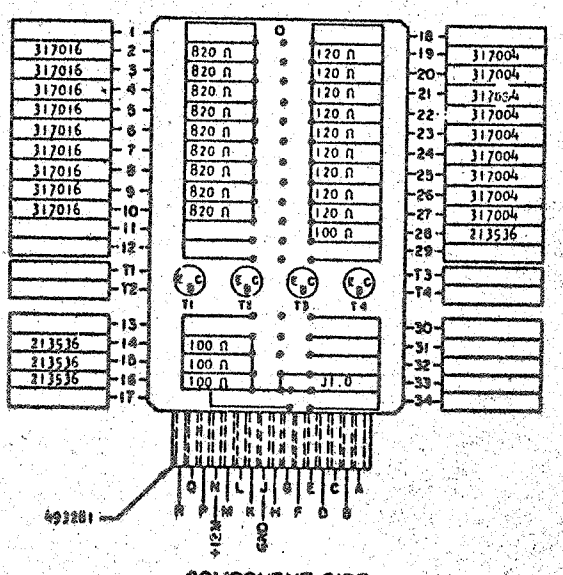
SEE PRODUCTION DRAWING 370334

SDTRL - END OF LINE TERMINATORS



APPLICATION

1. 100Ω RESISTOR USED TO TERMINATE A SDTRL TRANSMISSION LINE
2. 820Ω AND 120Ω RESISTOR FORM COUPLING NETWORK WHICH ACTS AS A SPECIAL END OF LINE TERMINATOR FOR SDTRL COAXIAL LINE AND WITH ITS' INPUT PIN FORMS A SEPARATE CIRCUIT
3. EACH PIN REPRESENTS A SEPARATE NETWORK OR RESISTOR



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARDS	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SDTRL - END OF LINE TERMINATORS					4-29-63	EC 115599					
DESIGN			MODEL	SMS		5.8.63	JT 83687					
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729939

C

729939

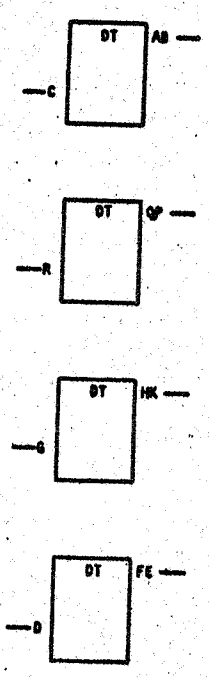
729940 STANDARDS CODE

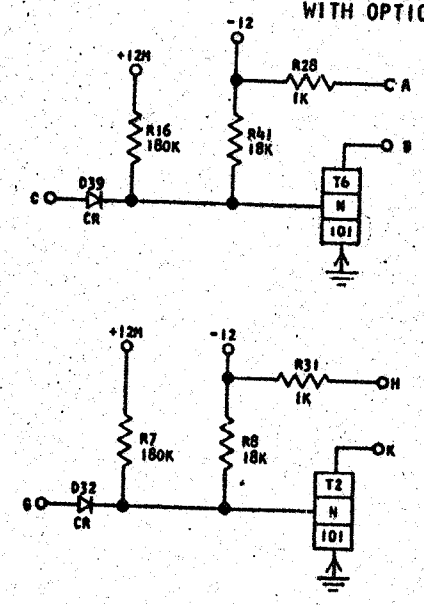
CARD CODE 729940
T D B -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370389

SDTRL-DISTRIBUTED LINE TERMINATOR
WITH OPTIONAL LOAD RESISTORS





SEQUENCE OF OPERATION

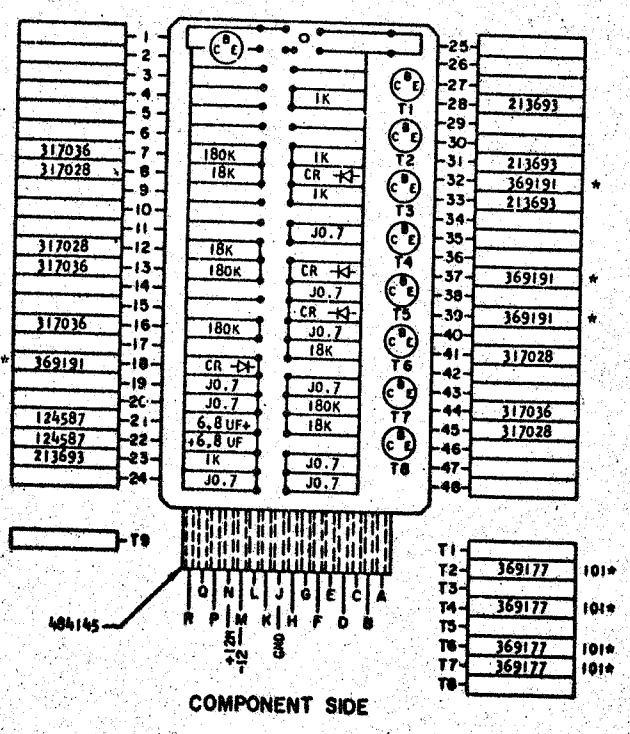
1. DOWN INPUT TRANSISTOR ON OUTPUT UP
2. UP INPUT TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C,R, G,D	N	INPUT		UP	+.65	
				DOWN	-.7	
B,P, K,E	Y	OUTPUT		UP	-.1	-.5
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	106	120*
TURN OFF	108	126*

*FOR 100 FT OF CABLE.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SDTRL- DISTRIBUTED LINE TERMINATOR					6-29-62	EC 115599					
DESIGN			MODEL	SMS		30.4.63	JT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WR	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

C

729940

729940

729941

STANDARDS CODE

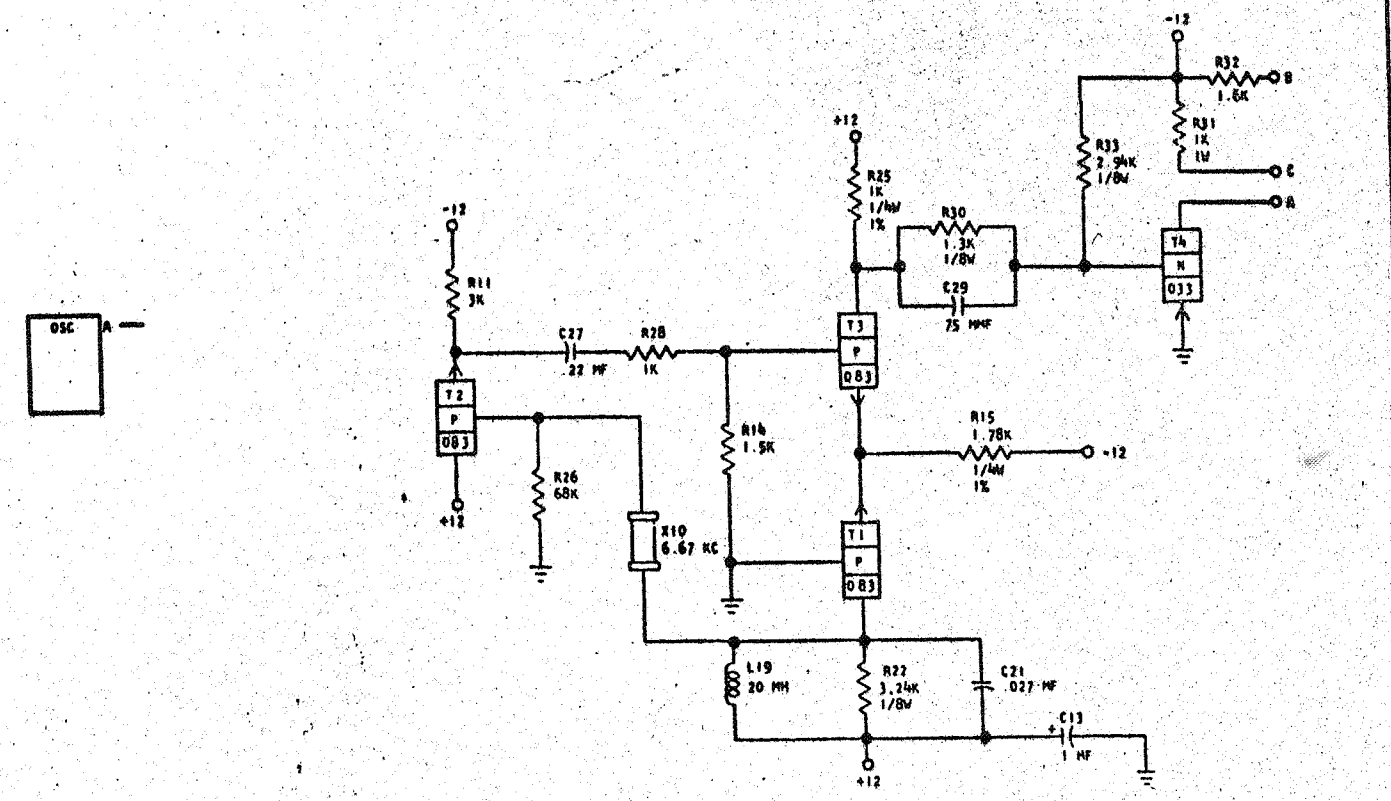
CARD CODE 729941

T-D-C -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370401

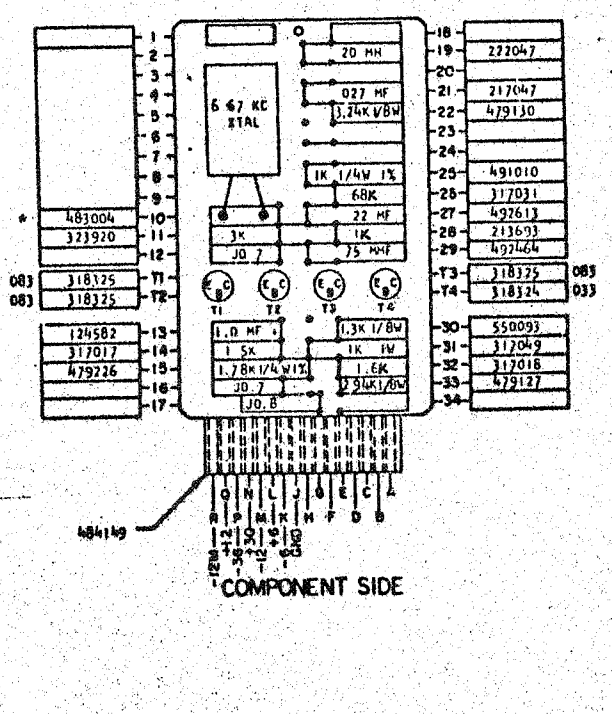
SDTDL-SDTRL - 6.67 KC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON THE CURRENT REQUIREMENTS.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A	S	OUTPUT	6.67KC	UP	-.5	-.1
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP						DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTL SDTRL-6.67 KC OSCILLATOR					3-27-62	EC 115599					
						30.4.63	JT 83687					
DESIGN				MODEL	SMS							
DETAIL	RG	3-1-62		SCALE	NONE							
CHECK	WH	3-1-62		DRAW	LIG	3-17-62						
APPRO				CHECK								

729941

C

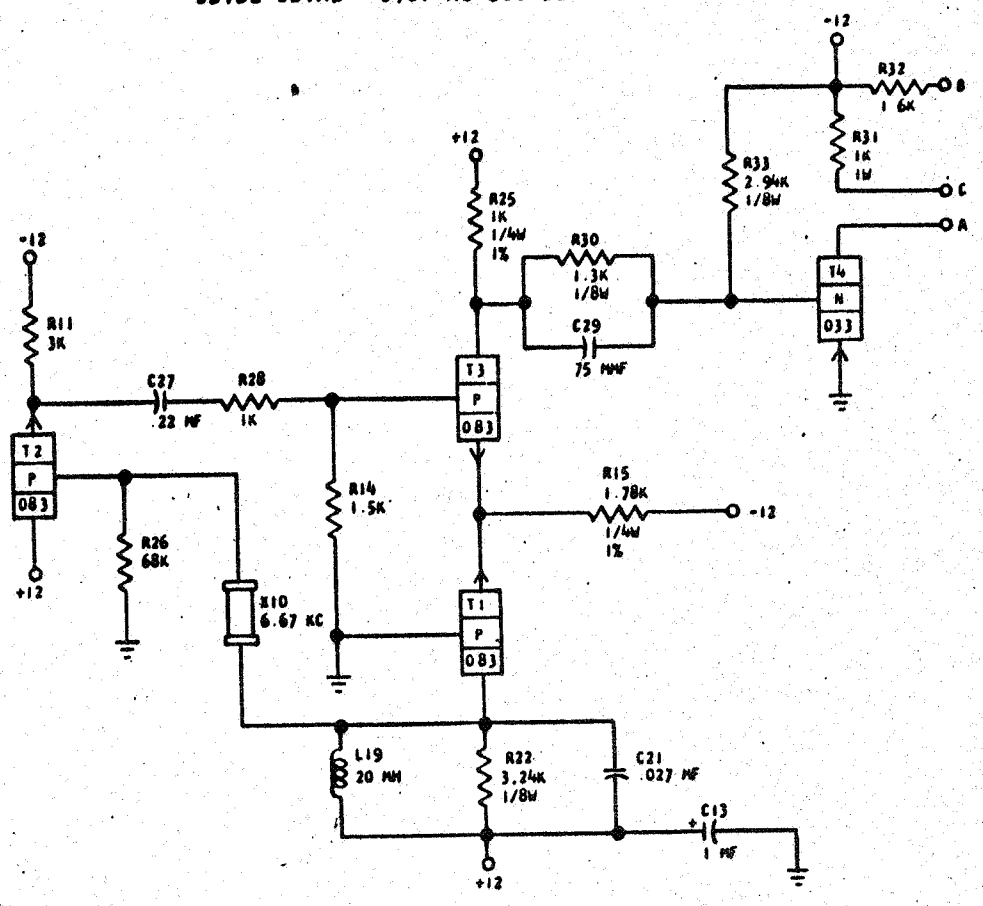
STANDARDS CODE 729941

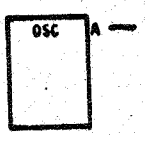
CARD CODE T D C - 729941

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370401

SDTDL-SDTRL - 6.67 KC OSCILLATOR

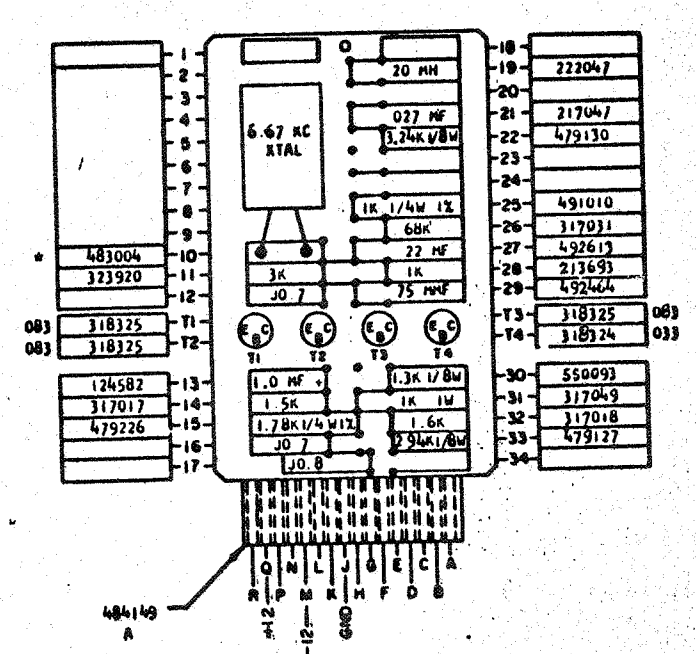




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON THE CURRENT REQUIREMENTS.

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
A	S	OUTPUT	6.67KC	UP	-.5	-.1
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARDS	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.	729941
NAME	CARD ASM TSTR-SDTL SDTRL-6.67 KC OSCILLATOR					2-27-62	115599						
DESIGN			MODEL	SMS		8-28-63	117802						
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRD			CHECK										

C

729941

729942

STANDARDS CODE

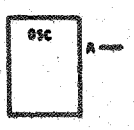
CARD CODE 729942

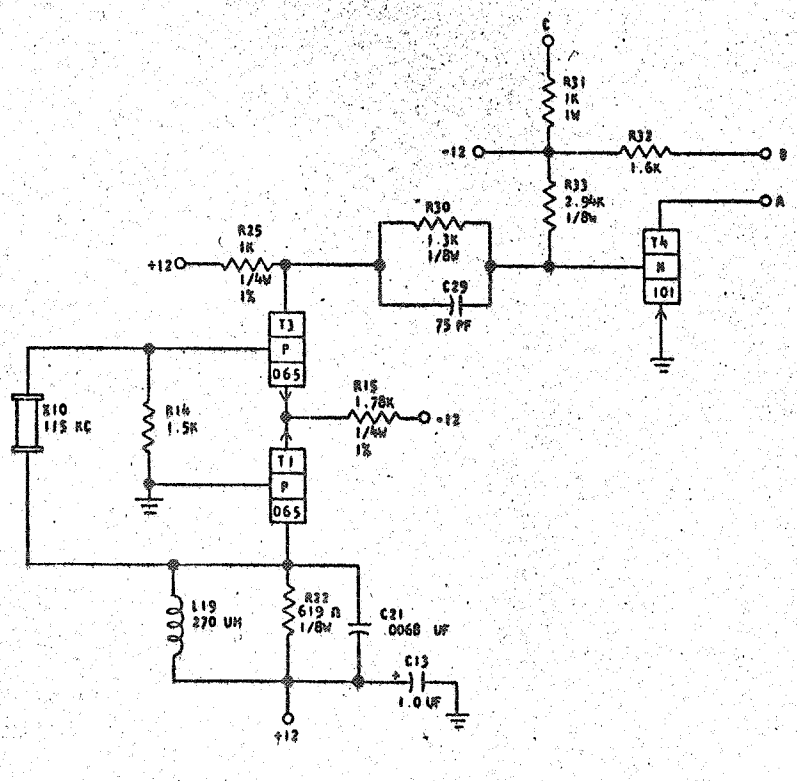
T D D -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370400

SDTDL-SDTRL - 115 KC OSCILLATOR

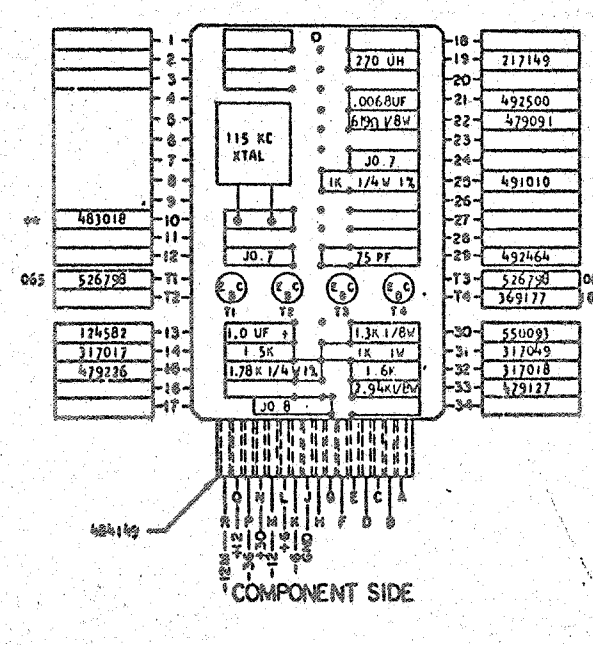




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
A	S	OUTPUT	115KC	UP	-.45 +	-.05
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SDTDL				6-11-62	EC115599					
	SDTRL-115 KC OSCILLATOR				30-4-63	TT83687					
DESIGN			MODEL	SMS							
DESIGN	RG	5-1-62	SCALE	NONE							
CHECK	WH	5-1-62	DRAW	LIG 5-17-62							
APPRO			CHECK								

C

729942

729942

STANDARDS CODE

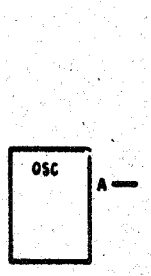
CARD CODE 729942

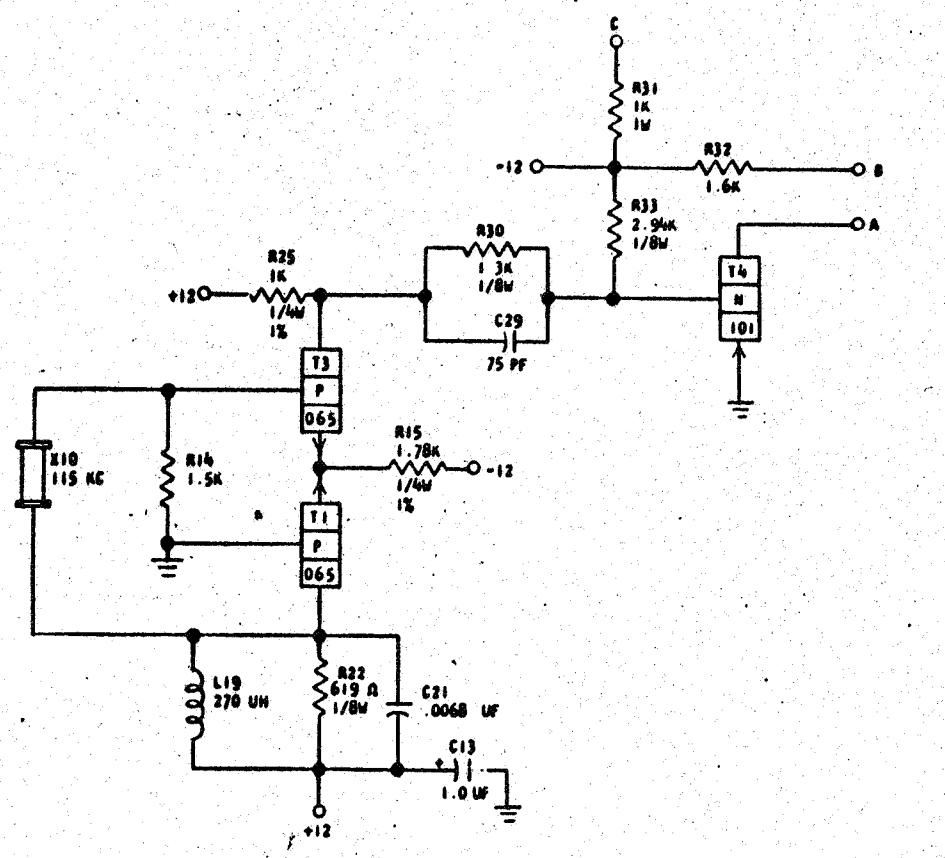
T D D -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370400

SDTDL-SDTRL - 115 KC OSCILLATOR

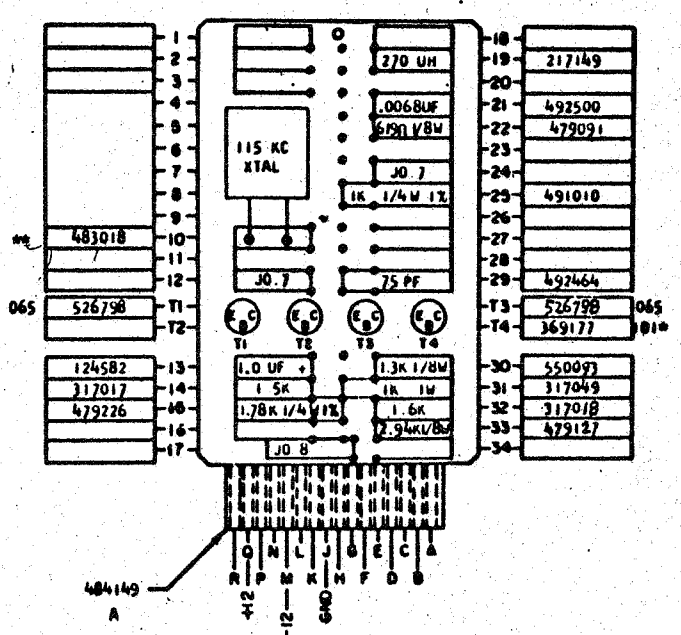




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	S	OUTPUT	115KC	UP	-.45	-.05
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.	729942
NAME	CARD ASM TSTR- SDTDL					6-27-62	115599						
	SDTRL-115 KC OSCILLATOR					8-28-63	117802						
DESIGN			MODEL	SMS									
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRO			CHECK										

C

729942

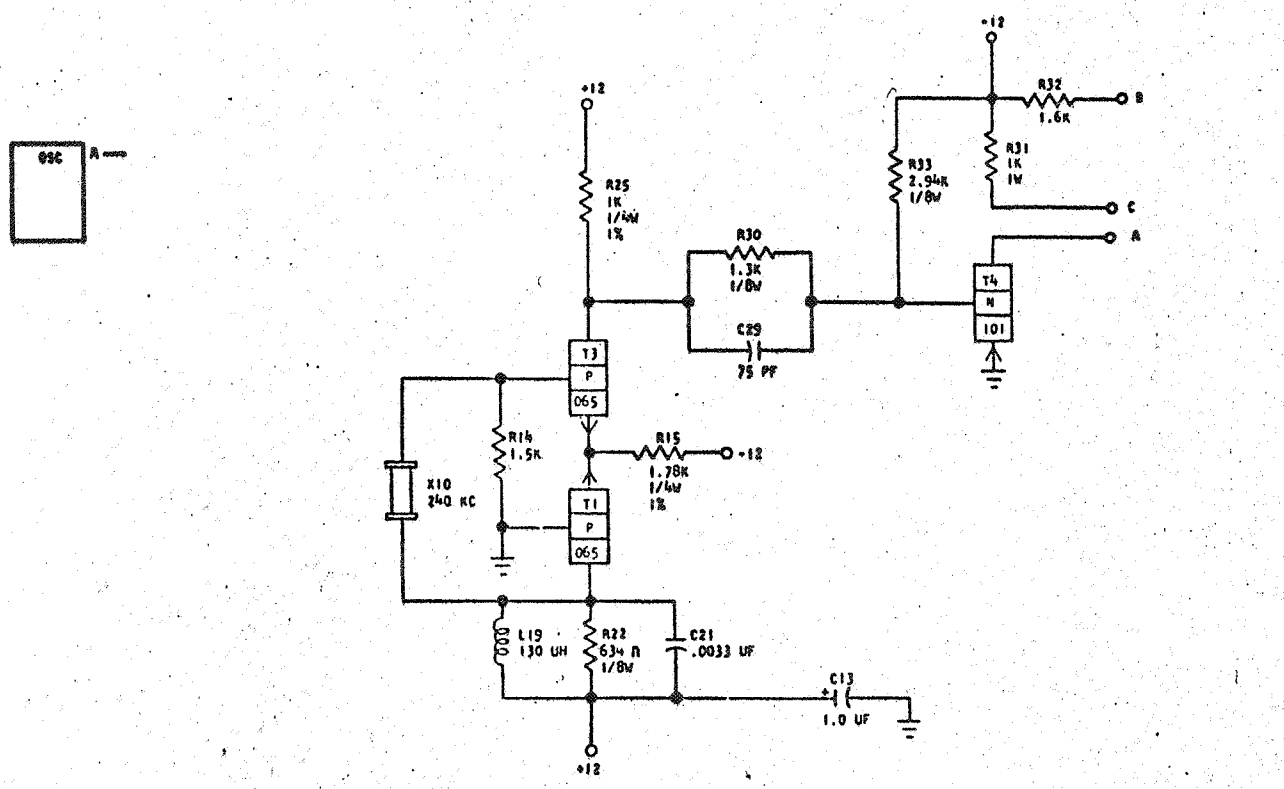
729943 | STANDARDS CODE

CARD CODE 729943
T D E -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370399

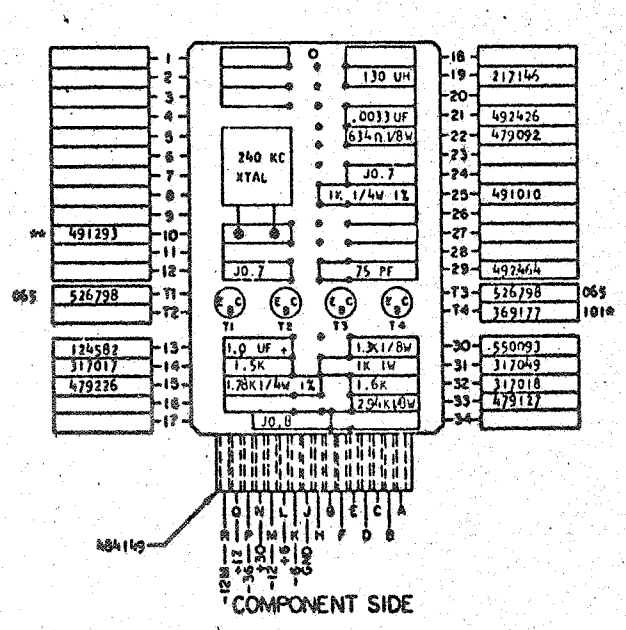
SDTDL-SDTRL-240 KC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CIRCUIT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MAX	MIN
A	B	OUTPUT	240 KC	UP	-.45	-.05
				DOWN	-.05	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHARGE NO.	APPROVAL	DATE	CHARGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL SDTRL-240 KC OSCILLATOR				6-19-62	EC 115599					
			MODEL	SMS	30.4.63	TT83687					
DESIGN											
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729943

C

3-6-63

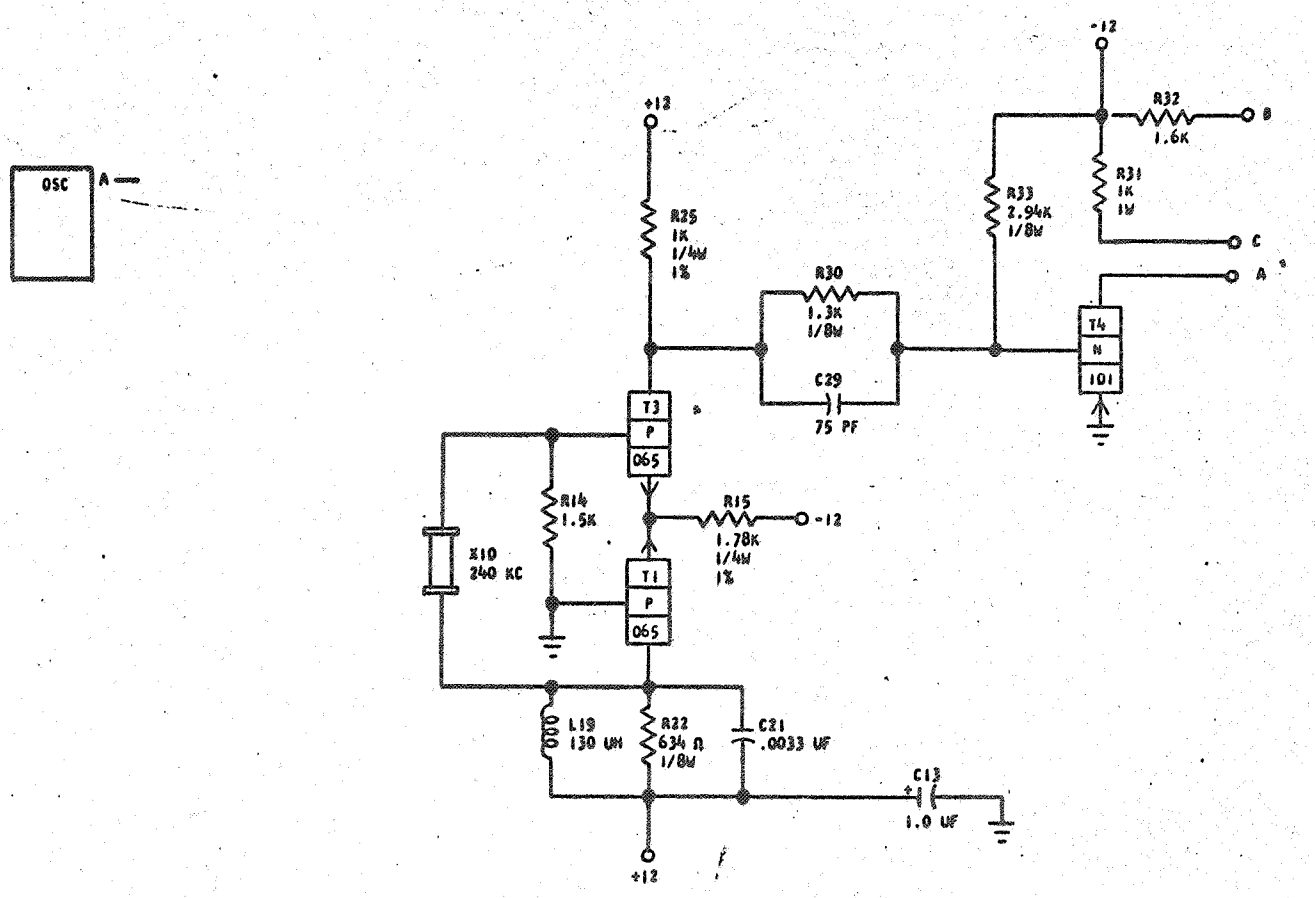
729943 | STANDARDS CODE

CARD CODE 729943
T D E -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370399

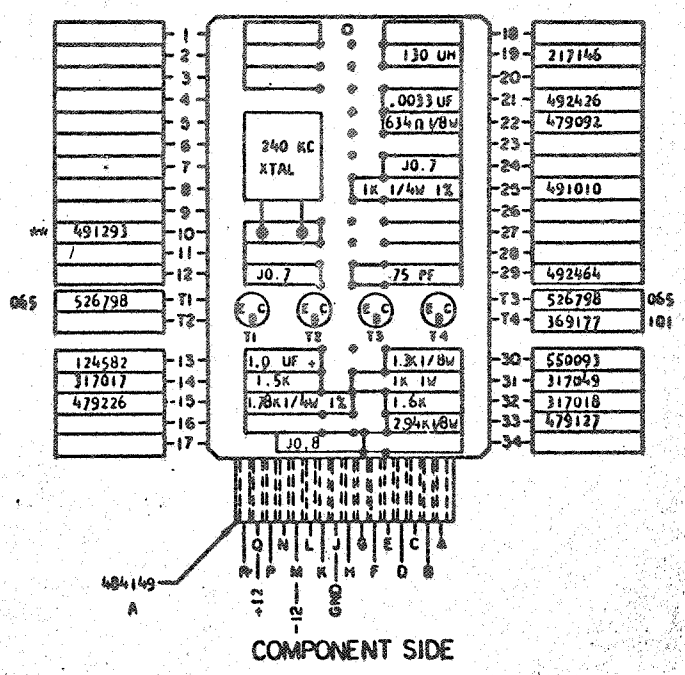
SDTDL-SDTRL-240 KC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CIRCUIT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MAX	MIN
A	S	OUTPUT	240 KC	UP	-.45	-.05
				DOWN	-.05	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO
NAME	CARD ASM TSTR-SDTDL				6-27-62	115599					
	SDTRL-240 KC OSCILLATOR				8-28-63	117802					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG	3-17-62						
APPRO			CHECK								

729943

C

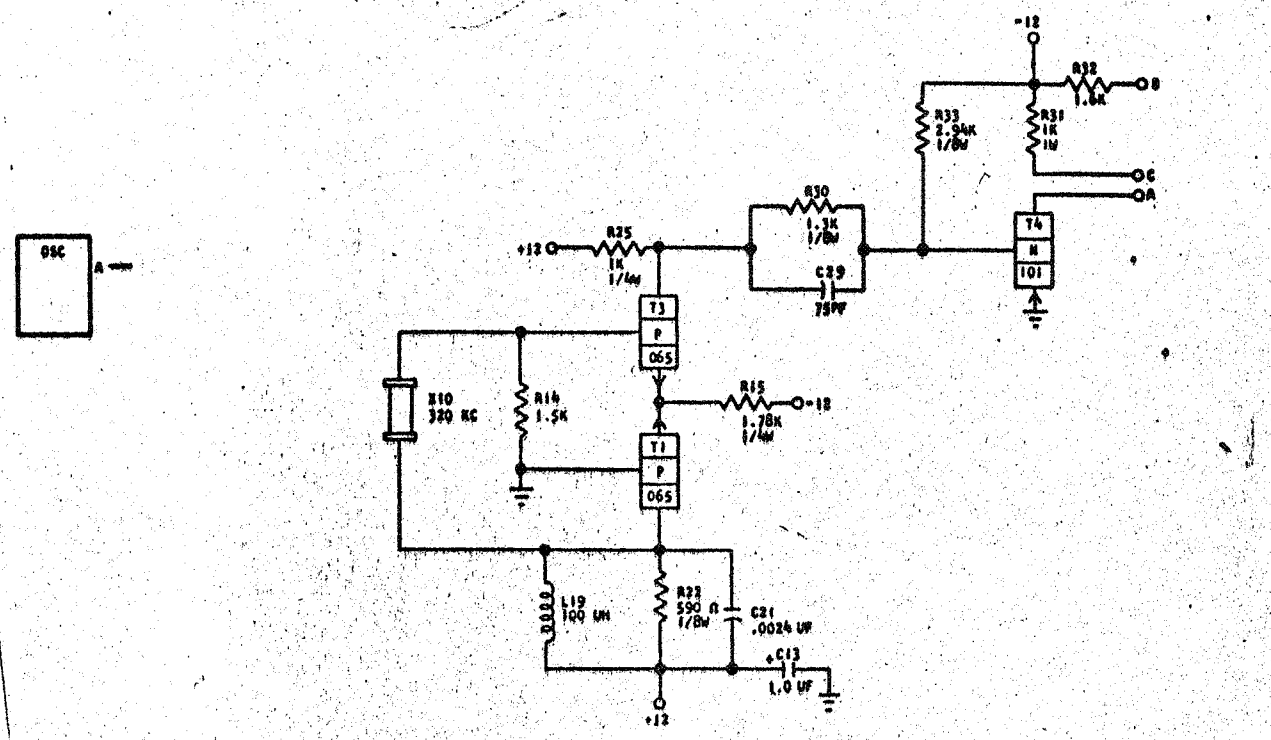
STANDARDS CODE 729944

CARD CODE 729944
T D F -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370398

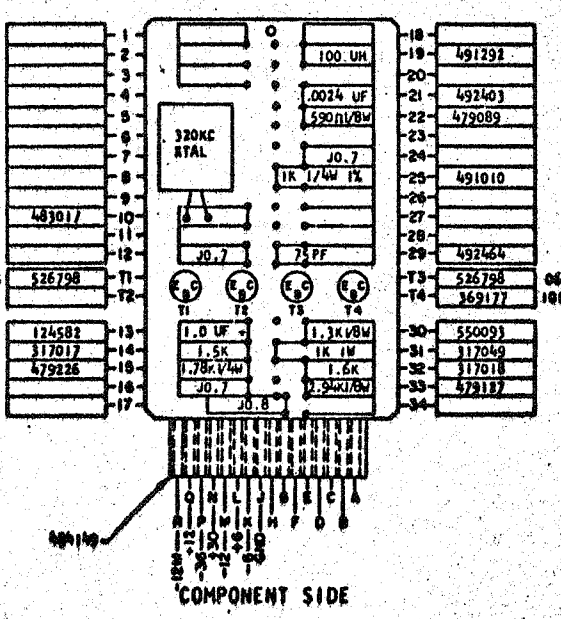
SDTDL-SDTRL-320 KC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS.

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
A	S	OUTPUT	320KC	UP	+.45	+.05
				DOWN	+5.8	-12.48



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD

APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL				6-1-62	EC 115599					
	SDTRL-320 KC OSCILLATOR				10.4.63	7783687					
DESIGN			MODEL	SMS							
DETAIL	MG	3-1-62	SCALE	NONE							
CHECK	MH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729944

C

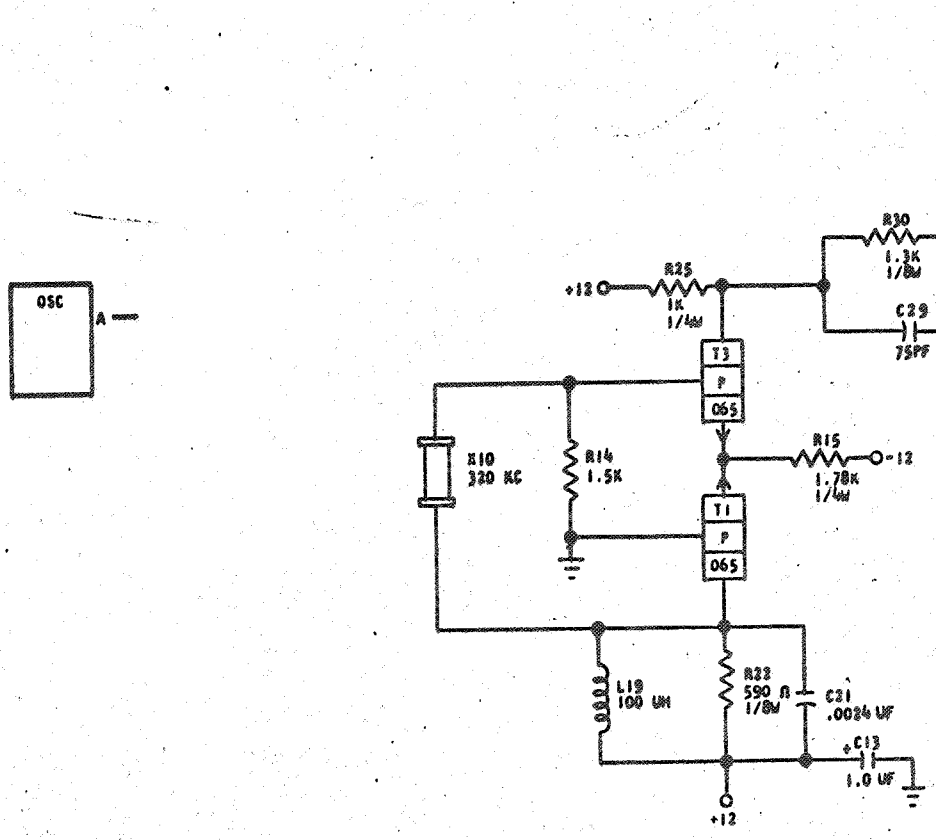
STANDARDS CODE	
729944	

CARD CODE	729944
TDF -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370398

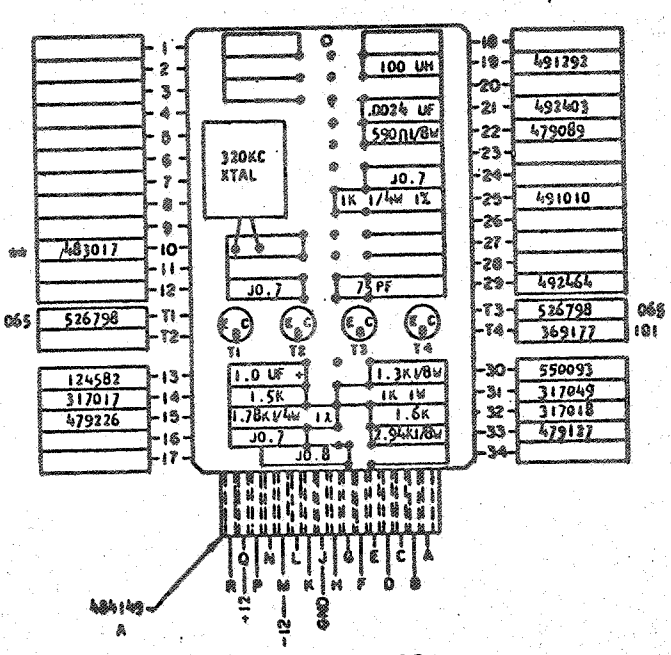
SDTDL-SDTRL-320 KC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	S	OUTPUT	320KC	UP	-.45	-.05
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-SDTDL				
	SDTRL-320 KC OSCILLATOR				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO
6-1-63	115599					
8-28-63	117802					

C

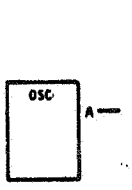
729945 | STANDARDS CODE

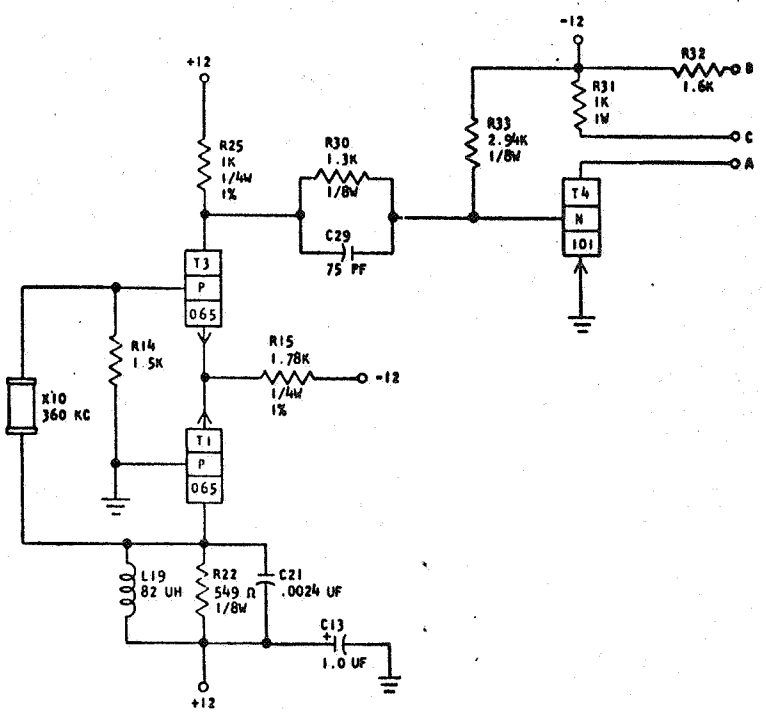
CARD CODE | 729945
T D G -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370397

SDTDL-SDTRL - 360 KC OSCILLATOR

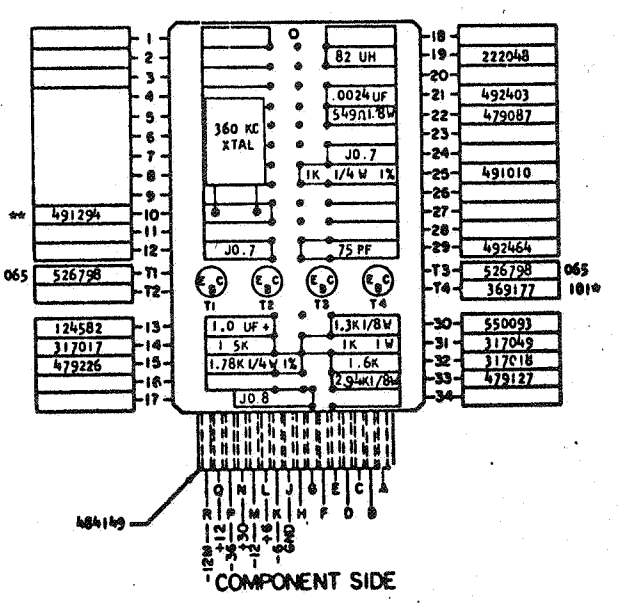




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
A	S	OUTPUT	360 KC	UP	-.45	-.05
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL					6-29-62	EC 115599					
	SDTRL - 360 KC OSCILLATOR					10.4.63	JT 83687					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WM	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729945

C

729945

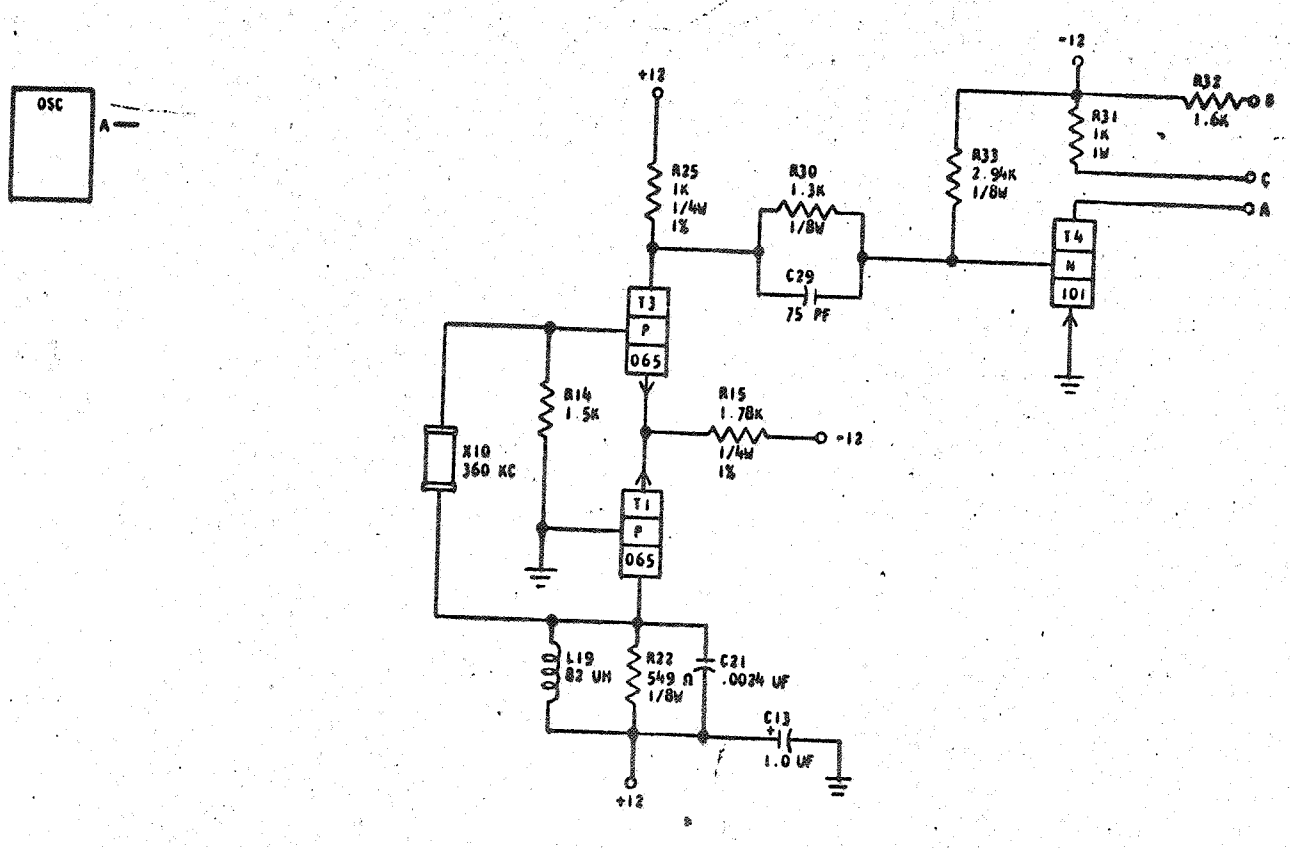
STANDARDS CODE

CARD CODE	729945
T D G -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370397

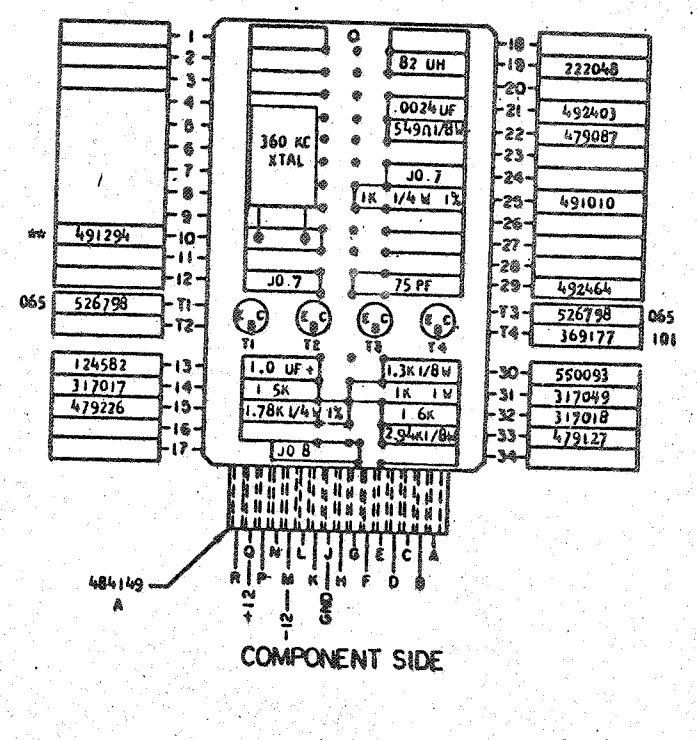
SDTDL - SDTRL - 360 KC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	S	OUTPUT	360 KC	UP	-.45	-.05
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO	
NAME	CARD ASM TSTR-SDTDL SDTRL - 360 KC OSCILLATOR					6-29-62	115599						729945
DESIGN			MODEL	SMS		8-28-63	117802						
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WN	3-1-62	DRAW	LIG	3-17-62								
APPRD			CHECK										

729945

729946

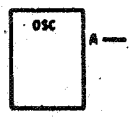
CARD CODE 729946

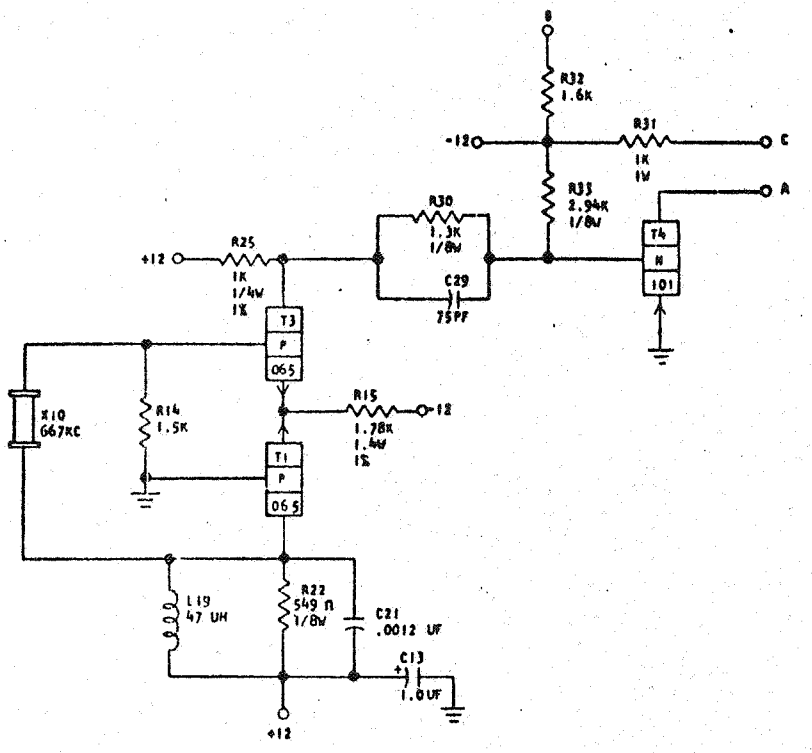
T D H -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370396

SDTOL-SDTRL-667 KC OSCILLATOR

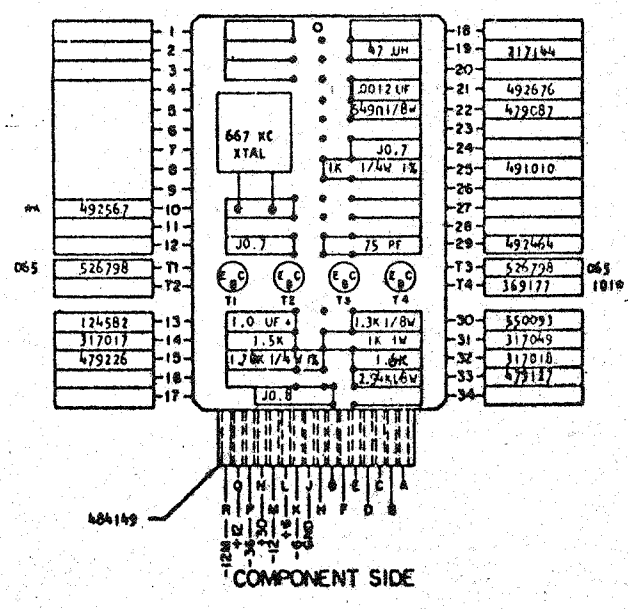




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	S	OUTPUT	667KC	UP	-.45	-.05
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729946
NAME	CARD ASM TSTR-SDTOL SDTRL-667 KC OSCILLATOR					6-27-62	EC115599						
DESIGN				MODEL	SMS	30.4.65	FI83687						
DETAIL	RG	3-1-62		SCALE	NONE								
CHECK	MH	3-1-62		DRAW	LIB	3-17-62							
APPRO				CHECK									

C

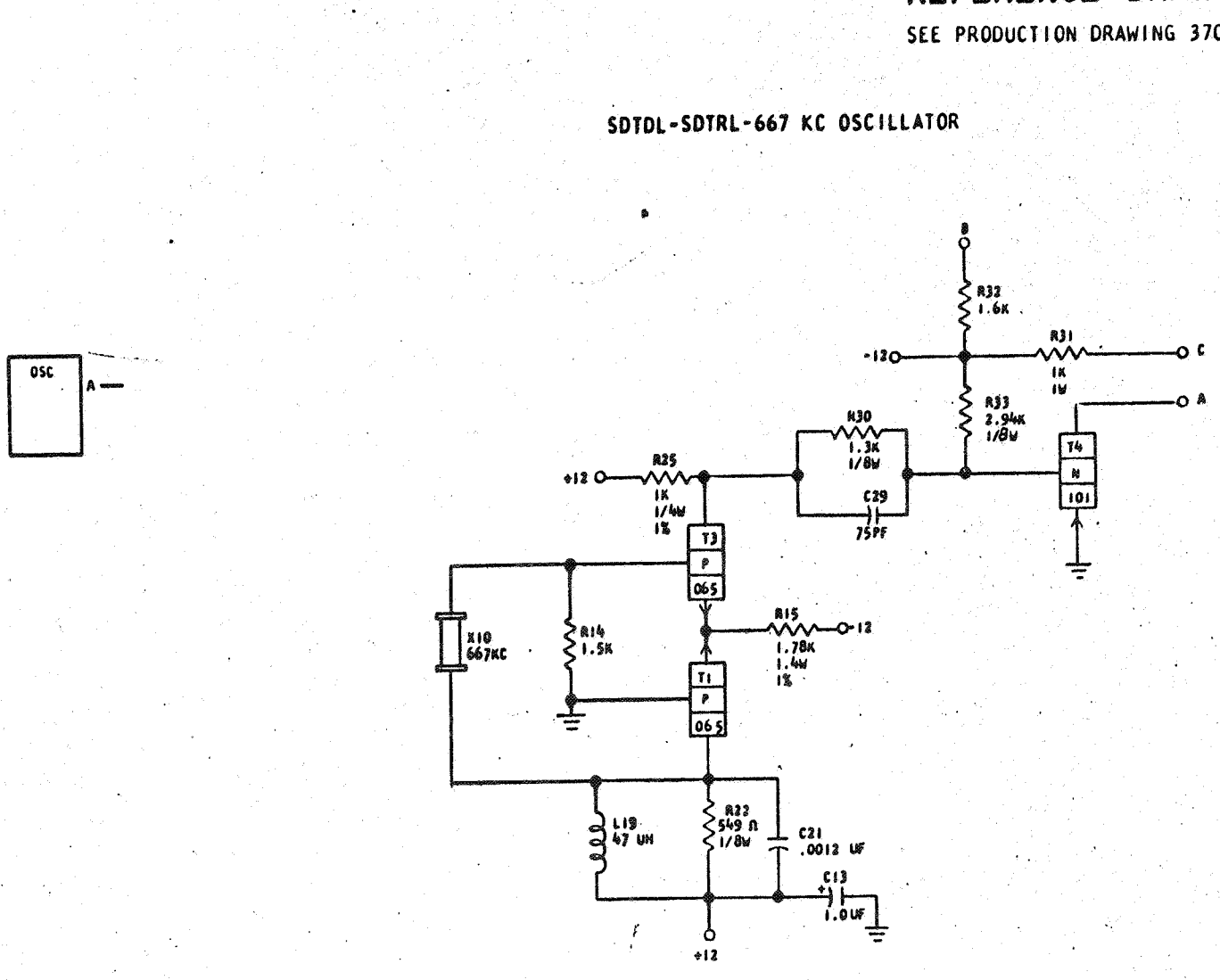
STANDARDS CODE	729946

CARD CODE	729946
T D H -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370396

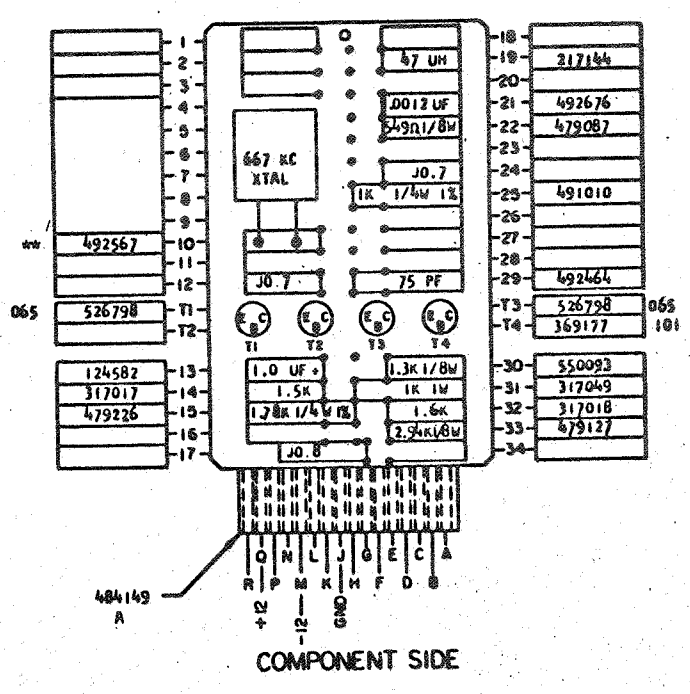
SDTDL-SDTRL-667 KC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	S	OUTPUT	667KC	UP	-.45	-.05
				DOWN	-5.8	-12.48



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.	729946
NAME	CARD ASM TSTR-SDTDL					6-11-62	115599						
	SDTRL-667 KC OSCILLATOR					8-28-63	117802						
DESIGN			MODEL	SMS									
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-63								
APPRO			CHECK										

C

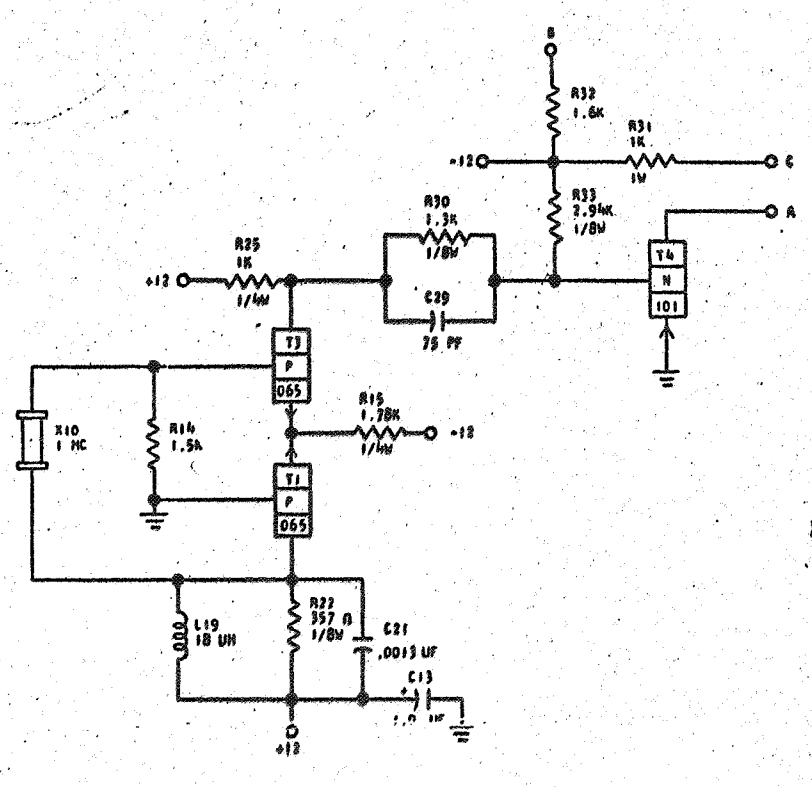
729947 STANDARDS CODE

CARD CODE 729947
TDK-

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370551

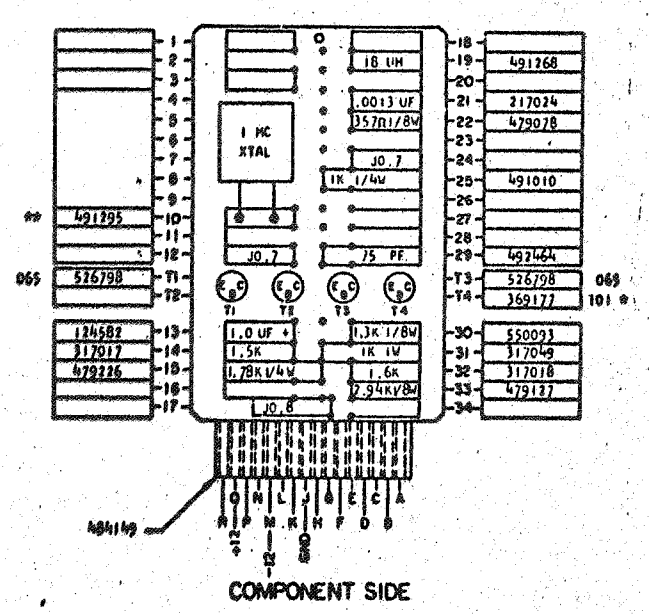
SDTDL-SDTRL - 1 MC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS DEPENDING ON CURRENT REQUIREMENTS.

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS	
					MIN	MAX
A	B	OUTPUT	1MC	UP	-.3	0
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL-SDTRL-1 MC OSCILLATOR					4-11-62	EC 119599					
DESIGN	-		MODEL	SMS		30.4.61	JT 836B7					*
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-63							
APPRO			CHECK									

729947

C

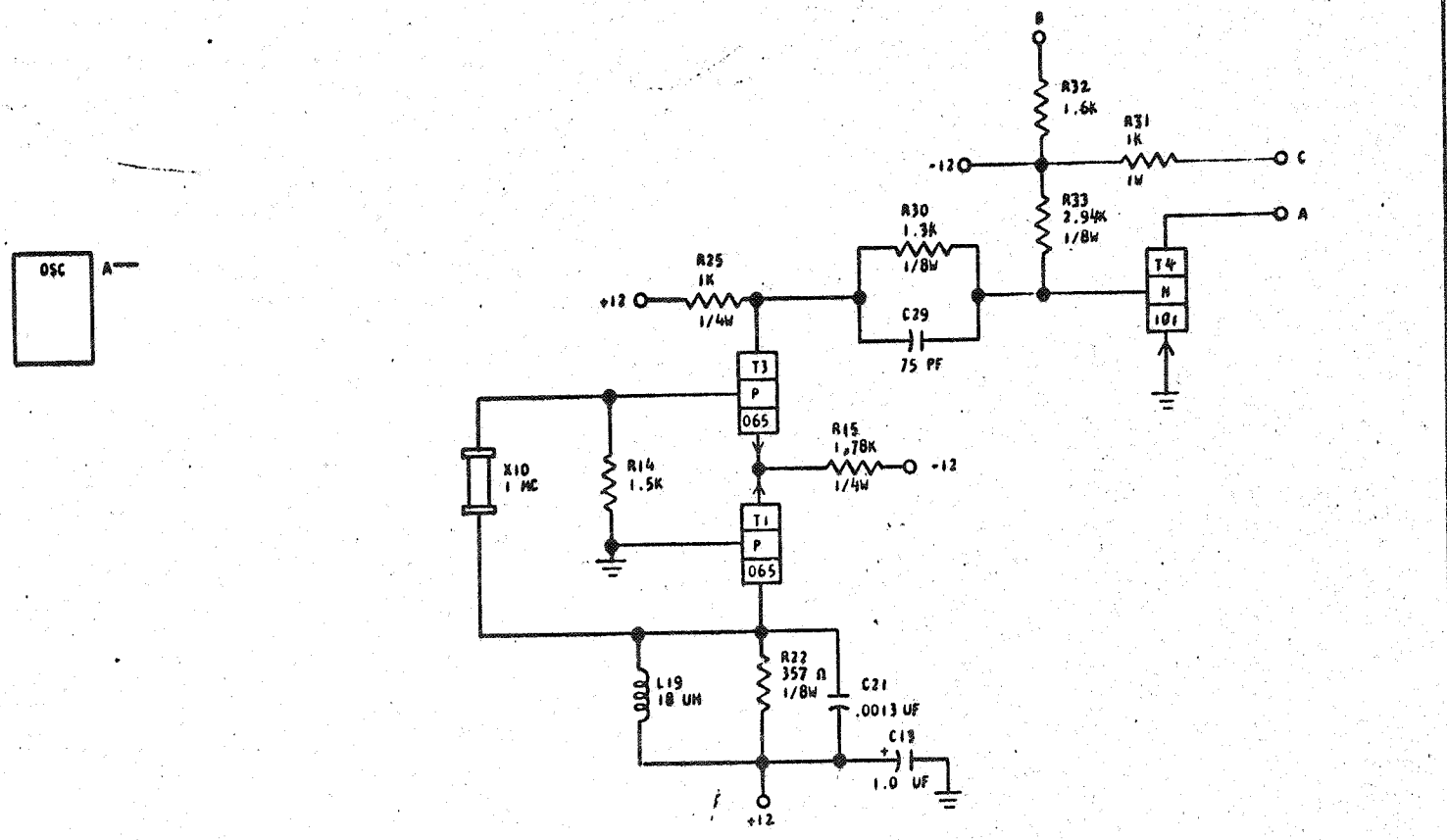
729947

STANDARDS CODE	729947
CARD CODE	729947
T D K -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370551

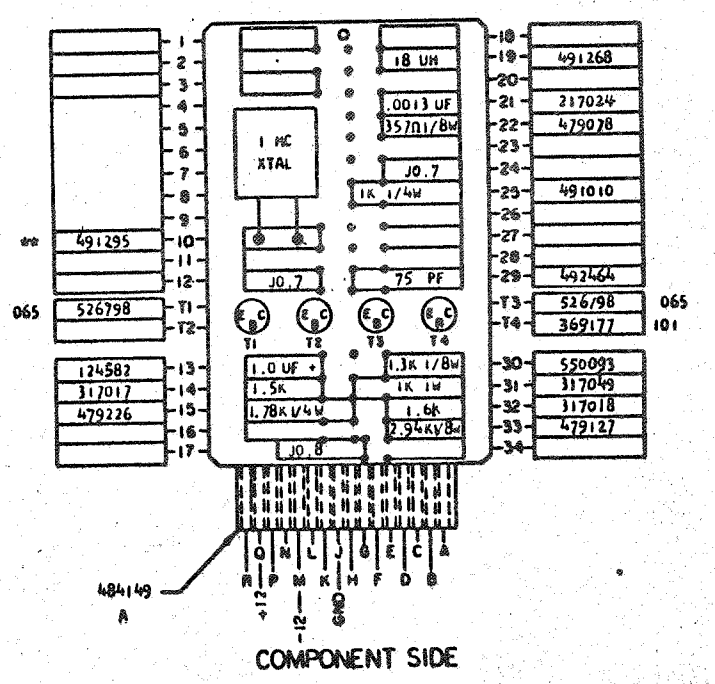
SDTDL-SDTRL - 1 MC OSCILLATOR



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS DEPENDING ON CURRENT REQUIREMENTS.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A	S	OUTPUT	1MC	UP	-.3	0
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729947
NAME	CARD ASM TSTR-SDTDL-SDTRL-1 MC OSCILLATOR					2-22-62	115599						
						8-28-63	117802						
DESIGN			MODEL	SMS									
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRO			CHECK										

C

729947

729948

CARD CODE 729948

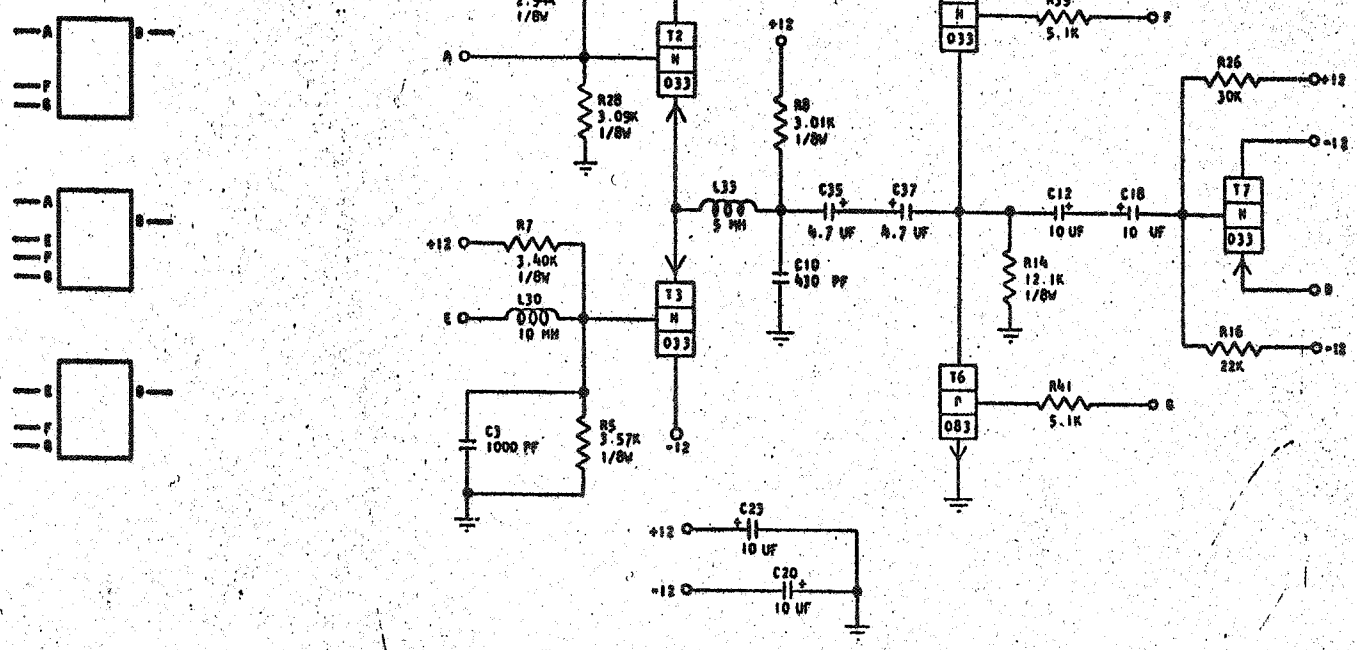
Y B Y -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370417

SENSE AMPLIFIER - INPUT FILTER AND SELECT GATE

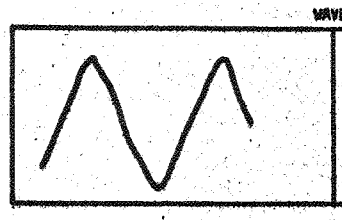
MOUNT CARD ON ONE INCH CENTERS NOTE XXX



SEQUENCE OF OPERATION

1. PIN F AT +12V AND PIN G AT -12V FROM GATE ON SIGNAL AMPL CARD
2. PIN B WAVE FORM WILL BE SAME AS INPUT WAVE FORM
3. TRANSISTOR THAT DOES NOT HAVE INPUT IS CUT OFF

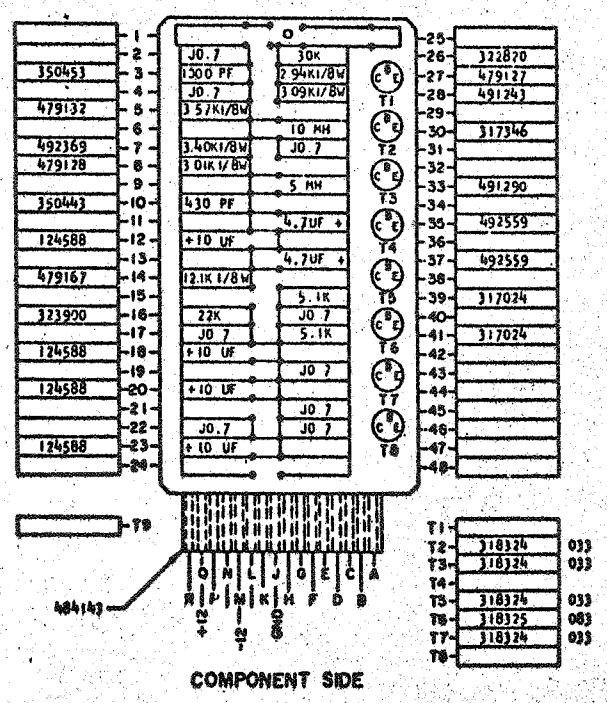
WAVE FORMS



INPUT WAVE 8V P-P — PIN A FOR 729, PIN E FOR 7330

MAX 8.8 P-P

REFERENCE LEVEL 0V +1.2 -.8



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-SENSE AMPL				6-29-62	EC 115599						729948
	INPUT FILTER AND SELECT GATE				30.469	JT 83697						
DESIGN			MODEL	SMS								
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRO			CHECK									

C

729949

STANDARDS CODE

CARD CODE 729949

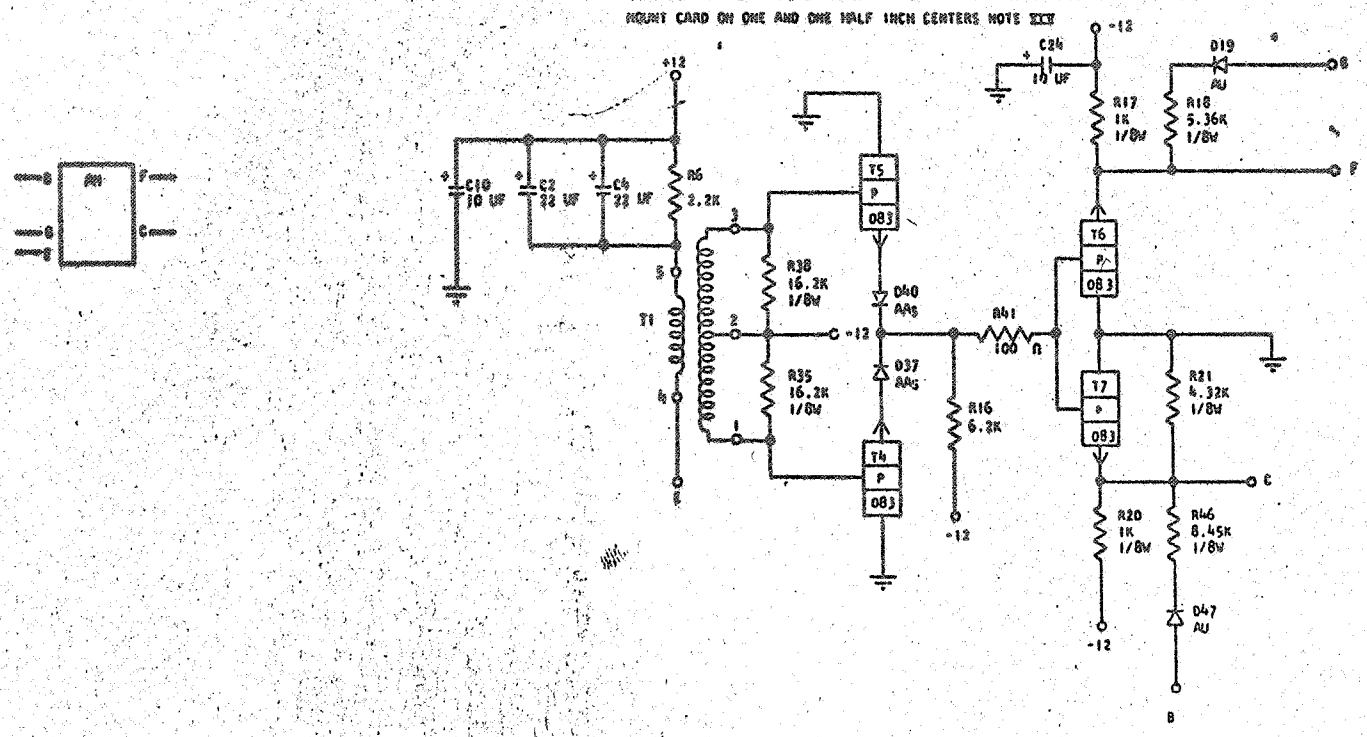
Y 8 Z -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370418

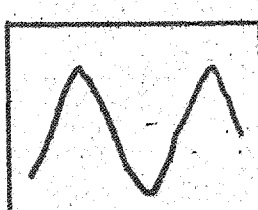
SENSE AMPLIFIER-RECTIFIER AND CLIPPER

MOUNT CARD ON ONE AND ONE HALF INCH CENTERS NOTE XXX

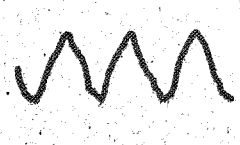


APPLICATION NOTES

VOLTAGES AT PIN B AND B FROM CLIPPING CARD

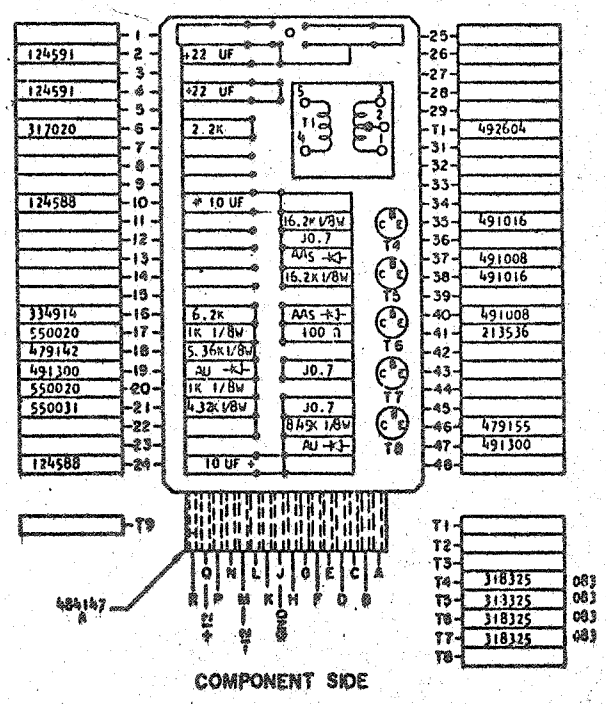


INPUT WAVE FORM AT PIN E
2.6VP-P NOMINAL FOR HIGH FREQUENCY
7.2VP-P NOMINAL FOR LOW FREQUENCY
8.4VP-P MAXIMUM
REFERENCE LEVEL +1.52V TO -3.88V



OUTPUT WAVE FORM AT PIN C

1. LOW ACCEPTANCE CHANNEL
   0V TO 9V P-P READ CONDITIONS
   0V TO 7.5 P-P READ WHILE WRITE CONDITIONS
2. HIGH ACCEPTANCE CHANNEL
   0V TO 6.85V P-P READ CONDITIONS
   0V TO 6.18V P-P READ WHILE WRITE CONDITION



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SENSE AMPLIFIER-RECTIFIER AND CLIPPER					6-28-62	EC 115599					
DESIGN			MODEL	SMS		30.4.63	JT83687					
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	MM	3-1-62	DRAW	LIC	3-17-63							
APPRO			CHECK									

729949

C

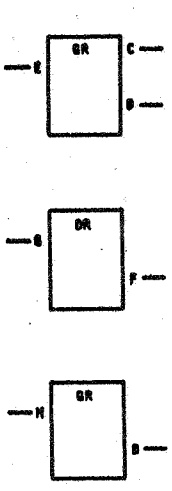
STANDARDS CODE 729950

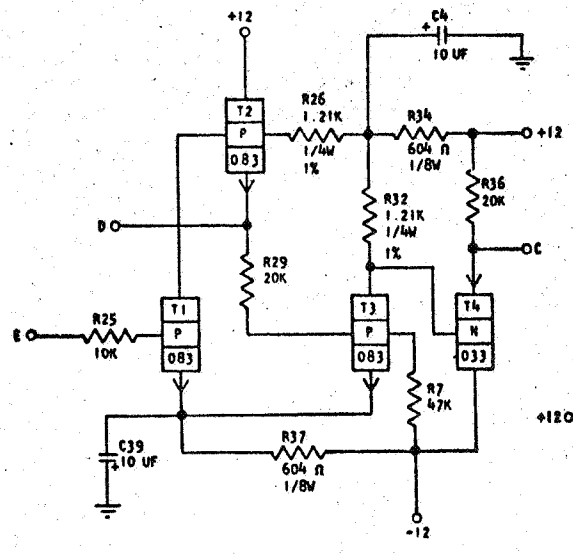
CARD CODE 729950
Y C B -

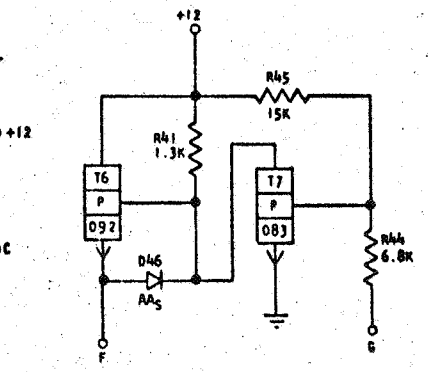
REFERENCE DRAWING

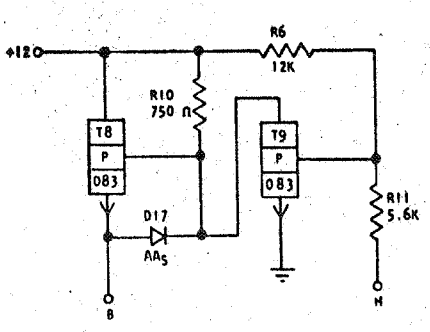
SEE PRODUCTION DRAWING 370420

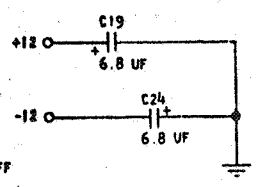
SENSE AMPLIFIER-SELECT GATE, READ GATE AND BAND PASS CTRL











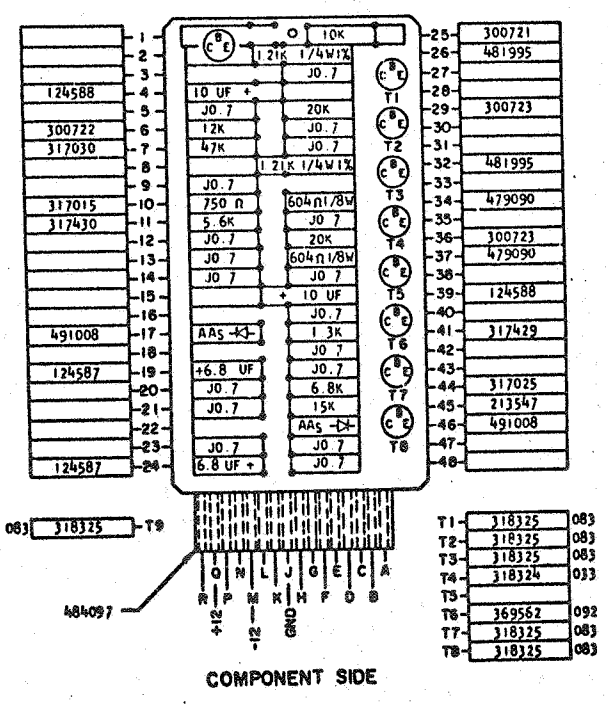
SEQUENCE OF OPERATION

A. SELECT GATE
   1. WHEN INPUT AT PIN E IS UP, T1 IS ON, T2, T3, T4, ARE OFF THE OUTPUT IS UP AT PIN C AND DOWN AT PIN D
   2. WHEN OUTPUT AT PIN E IS DOWN, T1 IS OFF, T2, T3, T4 ARE ON, THE OUTPUT IS DOWN AT PIN C AND UP AT PIN D

B. READ GATE
   1. WHEN INPUT AT PIN G IS UP, T7 TURNS ON, T6 TURNS ON AN OUTPUT AT PIN F IS DOWN
   2. WHEN INPUT AT PIN G IS DOWN, T7 IS OFF T6 IS ON, AND OUTPUT AT PIN F IS UP

C. NOISE REJECTION
   1. WHEN INPUT AT H IS UP, T9 IS ON, T8 IS ON AND OUTPUT AT B IS DOWN
   2. WHEN INPUT AT H IS DOWN, T9 IS OFF, T8 IS ON AND THE OUTPUT AT B IS UP

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E	S	SELECT GATE INPUT		UP	-.5	-.1
				DOWN	-7.42	-12.48
C	S	SELECT GATE OUTPUT #1		UP	5.14	7.23
				DOWN	-4.43	-6.64
D	S	SELECT GATE OUTPUT #2		UP	4.52	6.88
				DOWN	-4.76	-6.84
G	S	READ GATE INPUT		UP	-.5	-.1
				DOWN	-6.87	-12.48
F	S	READ GATE OUTPUT		UP	+9.39	+12.48
				DOWN	+.7	0
H	S	NOISE REJECT INPUT		UP	-.5	-.1
				DOWN	-6.87	-12.48
B	S	NOISE REJECT OUTPUT		UP	10.41	12.48
				DOWN	.7	0



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729950
NAME	CARD ASM TSTR-SEN AM-SEL				6-29-62	EC 115599						
	GT, RD GT AND BAND PASS CTRL				30.4.63	JT 83687						
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRO			CHECK									

C

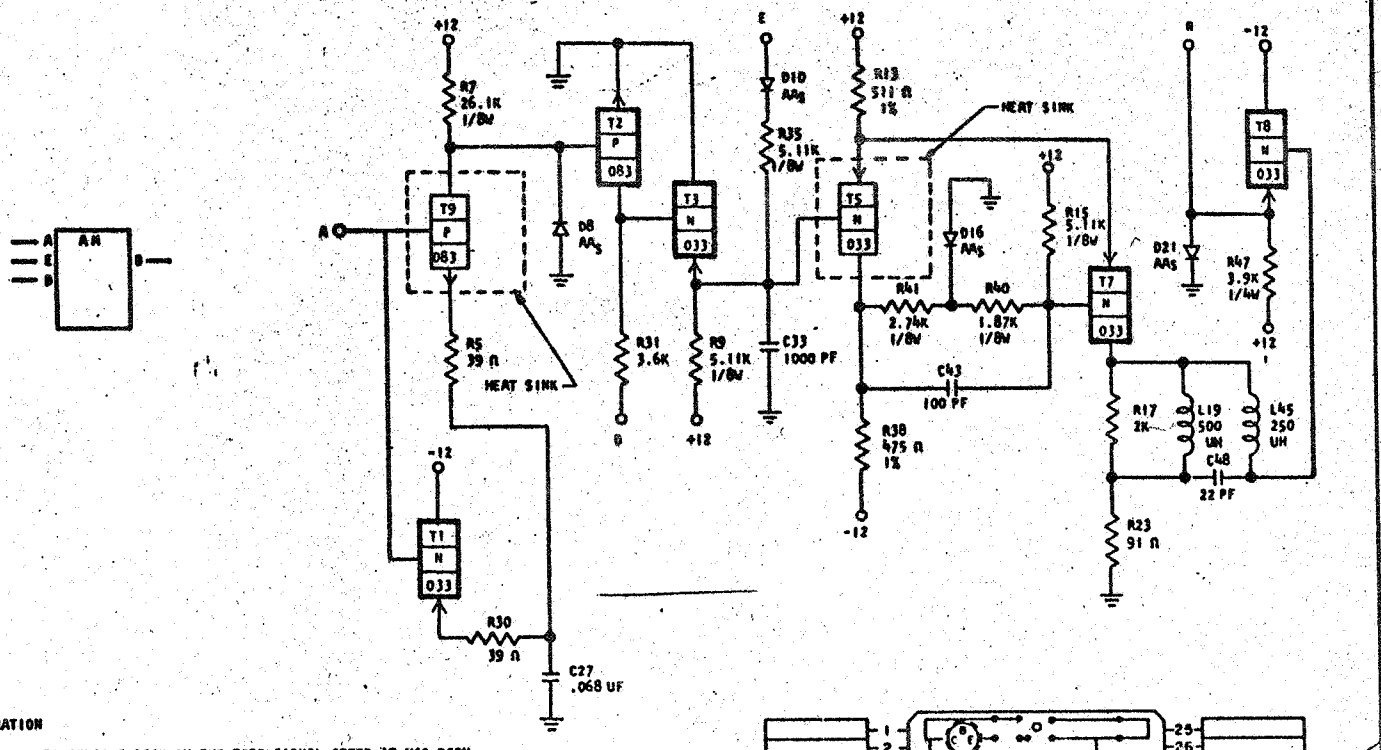
729951 STANDARDS CODE

CARD CODE 729951
Y C C -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370421

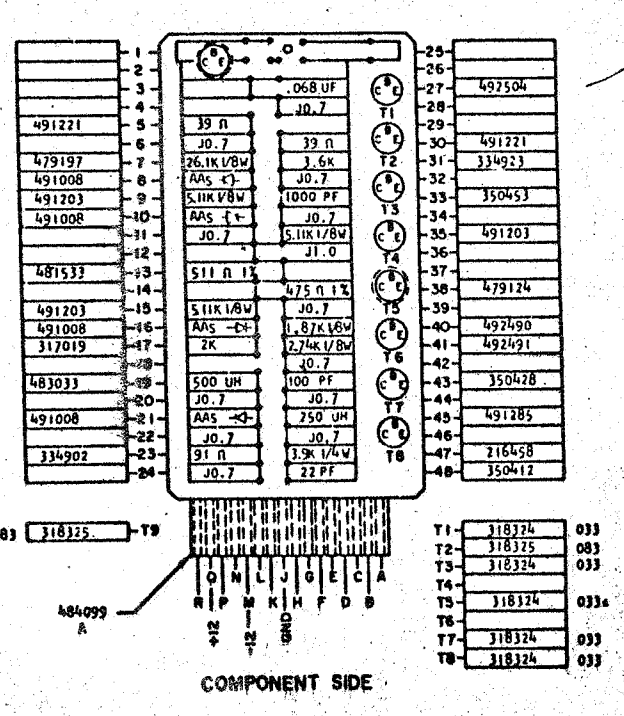
PEAK DETECTOR, INTEGRATOR & V.M. DRIVER



SEQUENCE OF OPERATION

1. THIS CIRCUIT IS USED TO SENSE A PEAK IN THE TAPE SIGNAL AFTER IT HAS BEEN AMPLIFIED BY THE TAPE PRE-AMPLIFIER. TRANSISTORS 1 AND 9 SENSE THE PEAK AND THIS SIGNAL IS AMPLIFIED BY T2 TO DRIVE T3 WHICH INTURN DRIVES THE INTEGRATOR AND THE SCHMITT TRIGGER. WHEN THE SCHMITT TRIGGER FIRES, THE FALL TRANSITION IS SHAPED INTO THE OUTPUT PULSE (-12V) AND THEN IT IS COUPLED TO THE LOAD BY T8, AN EMITTER FOLLOWER.
2. A READ CONTROL LINE IS USED TO GATE THE SIGNAL DURING SWITCHING BETWEEN READ AND READ-WHILE-WRITE CONDITIONS: PIN D. ANOTHER CONTROL LINE CHANGES THE NOISE REJECTION OF THE CIRCUIT DEPENDING UPON THE TYPE OF TAPE DRIVE WHICH IS USED: PIN E. FOR HIGH FREQUENCY OPERATION THE INPUT AT PIN E IS AT + 12 V. FOR LOW FREQUENCY OPERATION THE INPUT TO PIN E IS 0 V.
3. OUTPUT CAN DRIVE SDTDL OR SDTRL CIRCUITS.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
A		INPUT		UP		9 PEAK
				DOWN		0
E		NOISE REJECTION GATE	HIGH FREQUENCY		+10.41	+12.48
			LOW FREQUENCY		0	+.7
B	S	OUTPUT		UP	0	+.4
				DOWN	-11.5	-13
D	V	READ GATE		UP	+9.39	+12.48
				DOWN	0	+.7



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - PEAK DETECTOR INTEGRATOR & V.M. DRIVER					6-29-62	EC 115599					
DESIGN			MODEL	SMS		30.4.63	JT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WM	3-1-62	DRAW	LEG	3-17-62							
APPRO			CHECK									

729951

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729952

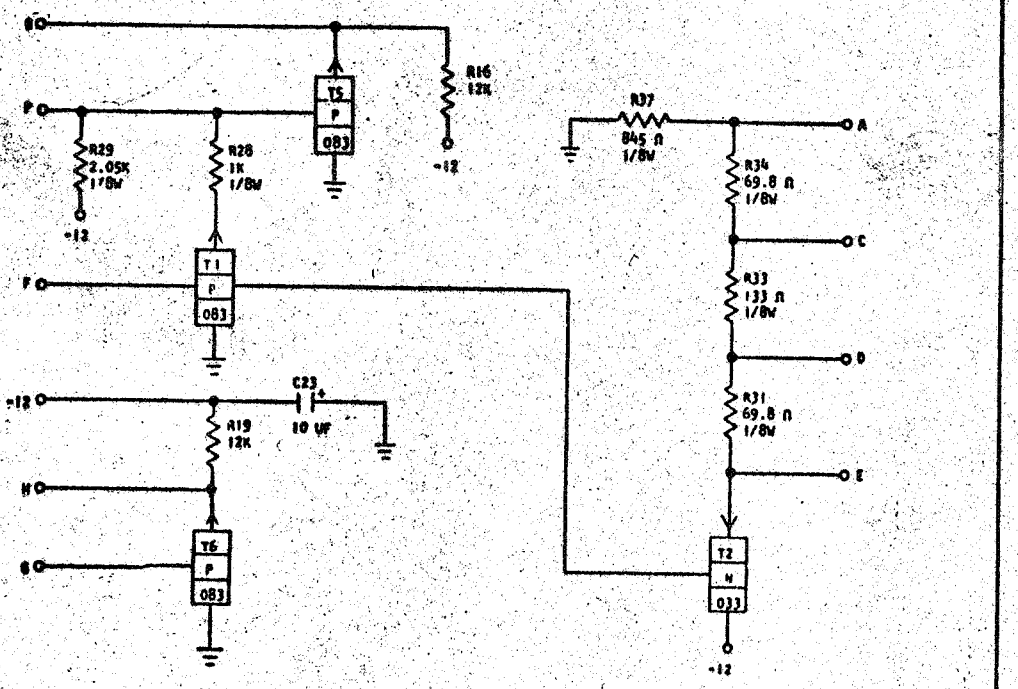
STANDARDS CODE

CARD CODE Y D M - 729952

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370501

SENSE AMPLIFIER-CLIPPING LEVEL CONTROL



APPLICATION NOTES

HIGH ACCEPTANCE - READ WHILE WRITE CONDITION

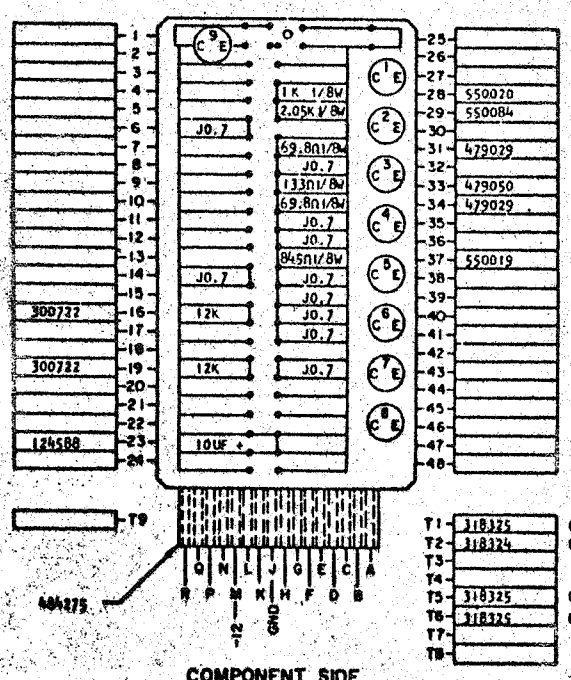
LOW SPEED TAPE
PIN F 0.0V +S — PIN B -3.07V TO -5.09V
PIN P -12.5V

HIGH SPEED TAPE
PIN F 0.0V +S — PIN B -.2V TO -.5V
PIN P 0.0V

READ CONDITION

HIGH AND LOW SPEED DRIVES
PIN F -12V — PIN B -11.1V TO -12.5V

LOW ACCEPTANCE — PIN H 0.0V
PIN F 0.0 VOLTS — PIN H -8.03 TO -12.5 DEPENDS
PIN F -12 VOLTS — ON WHAT PIN (A,C,D,E) B IS TIED TO



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-SENSE AMPLIFIER-CLIPPING LEVEL CONTROL				4-2-62	EC 815593						729952
DESIGN			MODEL	SMS	3.4.63	JTB3687						
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRWG	LTG 3-17-62								
APPRD			CHECK									

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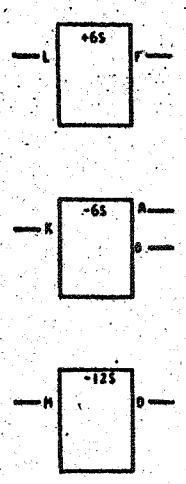
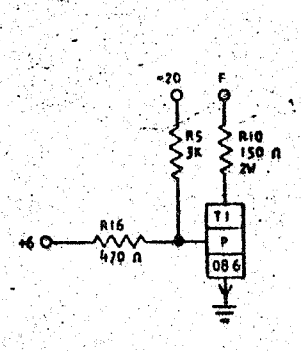
CARD CODE 729953
A J H -

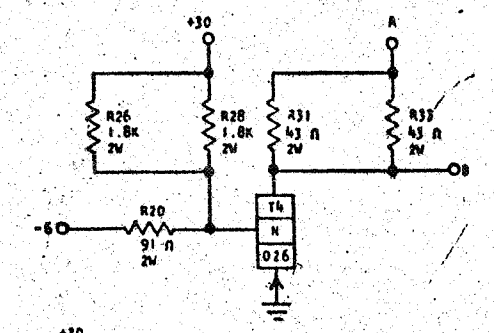
REFERENCE DRAWING

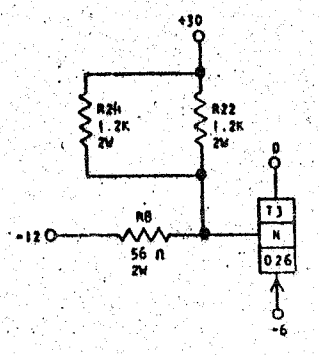
SEE PRODUCTION DRAWING 370429

POWER SUPPLY SEQUENCING









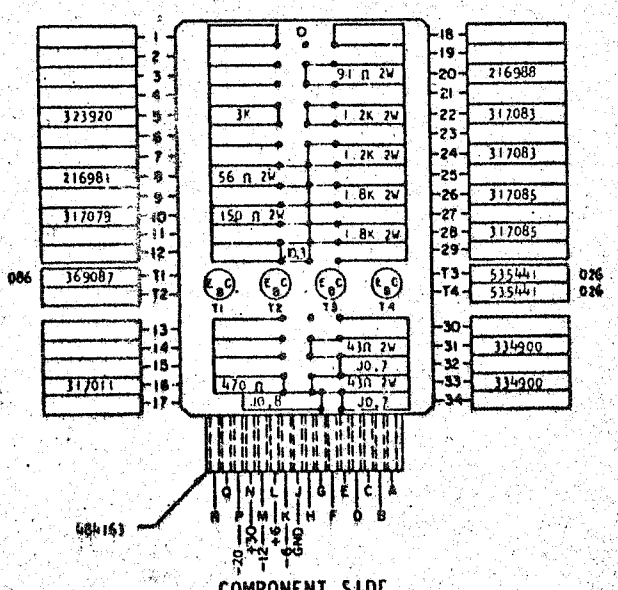
SEQUENCE OF OPERATIONS

1. THESE THREE CIRCUITS ARE SINGLE-STAGE RELAY DRIVERS, USED TO SENSE A GIVEN VOLTAGE. IF PRESENT, THIS VOLTAGE ALLOWS A TRANSISTOR TO CONDUCT AND OPERATE A RELAY IN THE COLLECTOR CIRCUIT. IF THIS VOLTAGE DROPS OUT DURING NORMAL OPERATIONS THE RELAY WILL ALSO DROP.

2. THE OUTPUT VOLTAGE LEVEL WHEN THE TRANSISTORS ARE OFF DEPENDS UPON THE RETURN VOLTAGE OF THE RELAY IN THE COLLECTOR CIRCUIT.

3. THE +6 VOLT SENSE (T1) MAY OPERATE A RELAY RETURNED TO NO MORE THAN 35 VOLTS, THE -6 VOLT SENSE (T4) 45 VOLTS, AND THE -12 VOLT SENSE (T3) 40 VOLTS.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
K	V	-6		UP	-1.1	+.24
				DOWN	-5.76	-6.24
B		OUTPUT	SEE NOTE 2	UP	-.24	+.24
				DOWN		
A		OUTPUT	SEE NOTE 2	UP	-.24	+.24
				DOWN		
L	V	+6		UP	+5.76	+6.24
				DOWN	+1.8	-.24
F		OUTPUT	SEE NOTE 2	UP		
				DOWN	+.24	-.24
H	V	-12		UP	-1.0	+.24
				DOWN	-11.52	-12.48
D		OUTPUT	SEE NOTE 2	UP	-6.24	-5.76
				DOWN		



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR-					4-19-62	EC 115599						729953
POWER SUPPLY SEQUENCING						30.4.63	JT 83687						
DESIGN			MODEL	SMS									
DETAIL	RG	3-1-62	SCALE	NONE									
CHECK	WM	3-1-62	DRAW	LIG	3-12-62								
APPRO			CHECK										

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729954 | STANDARDS CODE

CARD CODE 729954

SDTDL LOGIC FAMILY DELAY INFORMATION

GENERAL

THE TURN ON, TURN OFF DELAYS OF THE CIRCUITS USED IN A PARTICULAR MACHINE ARE COMPLEX FUNCTIONS OF MANY VARIABLES SUCH AS THE TRANSISTOR DELAY, INPUT-OUTPUT LOADING, FALL AND RISE TIME, ETC.

THE DELAY SPECIFICATIONS ARE GIVEN BELOW AND ARE CLASSIFIED BY CIRCUIT TYPE.

WHEN POSSIBLE, REPRESENTATIVE RANGES OF DELAYS ARE GIVEN ON EACH INDIVIDUAL CIRCUIT SHEET AND SHOULD BE USED AS A GUIDE. SPECIFIC CIRCUIT APPLICATION AND/OR CAPACITIVE LOAD (EXAMPLE: WIRE CAPACITANCE) MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES.

THE FOLLOWING INFORMATION IS PROVIDED FOR THOSE CASES WHERE CARD REPLACEMENT DOES NOT RESULT IN IMPROVEMENT AND A MORE DETAILED ANALYSIS IS NECESSARY.

HIGH SPEED, LOW SPEED CIRCUITS

THE SDTDL CIRCUITS ARE CLASSIFIED INTO TWO MAJOR FAMILIES, THE LOW SPEED AND THE HIGH SPEED CIRCUITS. THE DIFFERENCE BETWEEN THE TWO FAMILIES CONSISTS OF THE INPUT SPEED UP CAPACITOR THAT IS USED ONLY IN THE HIGH SPEED LOGIC BLOCKS.

DELAY CHARTS:

NUMEROUS CHARTS GIVING DELAY INFORMATION HAVE BEEN INCLUDED IN THIS DOCUMENT. BOTH MINIMUM AND MAXIMUM DELAYS ARE GIVEN AS A FUNCTION OF SOME VARIABLE OR VARIABLES. NOMINAL DELAYS HAVE BEEN AVOIDED DUE TO POSSIBLE MISINTERPRETATIONS. THE MAXIMUM DELAYS GIVEN ARE SLIGHTLY LESS THAN THE THEORETICAL MAXIMUM DELAY. THE MAXIMUM DELAYS GIVEN SHOULD NOT BE EXCEEDED IN PRACTICAL APPLICATIONS.

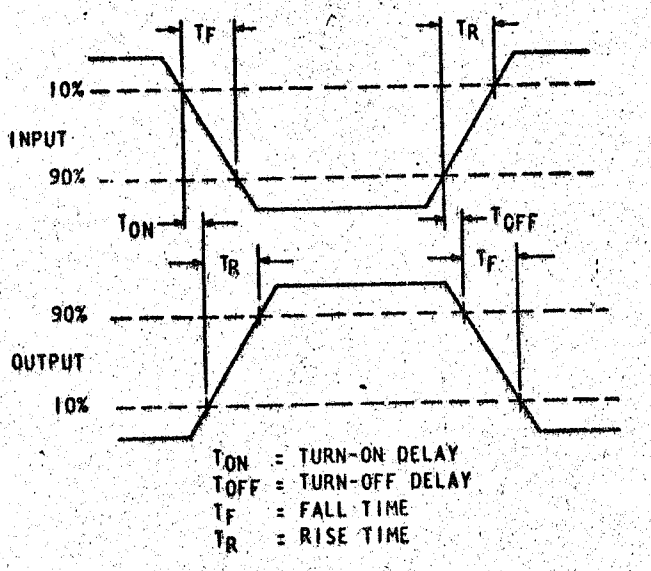
USE OF GRAPHS

THE FOLLOWING STEPS ARE RECOMMENDED FOR USING THE INFORMATION PROVIDED IN THE ACCOMPANYING GRAPHS.

1. GIVEN A LOAD CONFIGURATION REFER TO THE GRAPH OUTPUT FALL TIME VS. LOADING TO DETERMINE THE OUTPUT FALL TIME.
2. GIVEN THE INPUT FALL TIME, THE OUTPUT RISE IS DETERMINED FROM THE GRAPH OF OUTPUT RISE TIME VS. INPUT FALL TIME.
3. KNOWLEDGE OF THE RISE TIME AND USE OF THE GRAPH OF TURN-OFF DELAY VS. INPUT RISE TIME RESULTS IN TURN-OFF LIMITS.
4. KNOWLEDGE OF INPUT FALL TIME AND USE OF THE GRAPH OF TURN-ON DELAY VS. INPUT FALL TIME RESULTS IN TURN-ON LIMITS.

DEFINITIONS

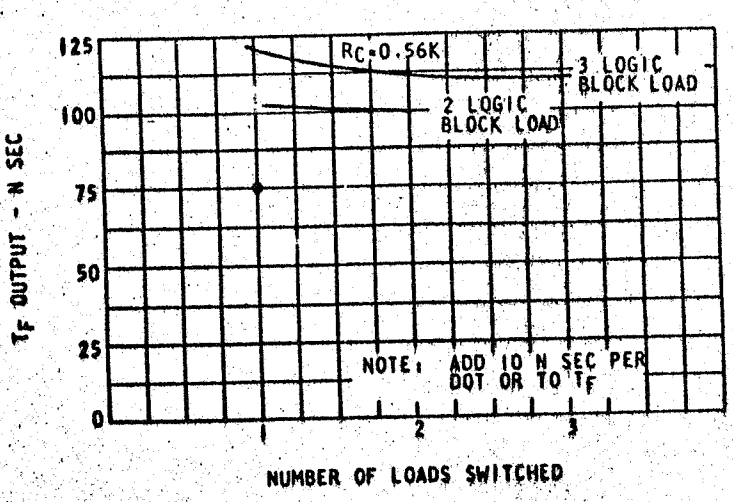
THE RISE AND FALL TIMES WERE MEASURED FROM THE 10% TO 90% POINTS OF THE INPUT AND OUTPUT WAVEFORM. THE TURN-ON DELAY WAS MEASURED AS THE TIME INTERVAL BETWEEN 10% DOWN AT THE INPUT TO 10% UP AT THE OUTPUT. THE TURN-OFF DELAY WAS MEASURED AS THE TIME INTERVAL BETWEEN 10% UP AT THE INPUT TO 10% DOWN AT THE OUTPUT. UNLESS OTHERWISE STATED THE RISE, FALL AND DELAY TIMES ARE GIVEN IN N SEC (NANOSECONDS).



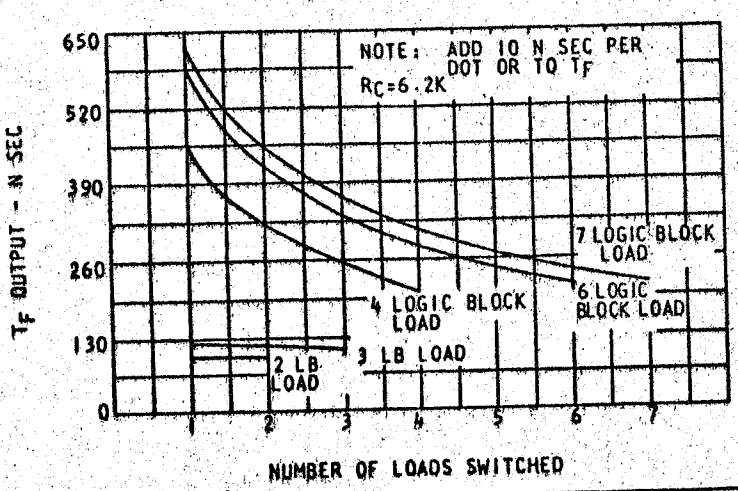
T_{ON} = TURN-ON DELAY
T_{OFF} = TURN-OFF DELAY
T_F = FALL TIME
T_R = RISE TIME

HIGH SPEED SINGLE LEVEL LOGIC BLOCK

OUTPUT FALL TIME VS LOADING



OUTPUT FALL TIME VS LOADING



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME SDTDL LOGIC DELAY INFO. - REF. Dwg				6-11-62	EC115599					729954
				10.4.63	ITB3687					
DESIGN			MODEL							
DETAIL	WDL	3-1-62	SCALE							
CHECK	RG	3-1-62	DRAW							
APPRD			CHECK							

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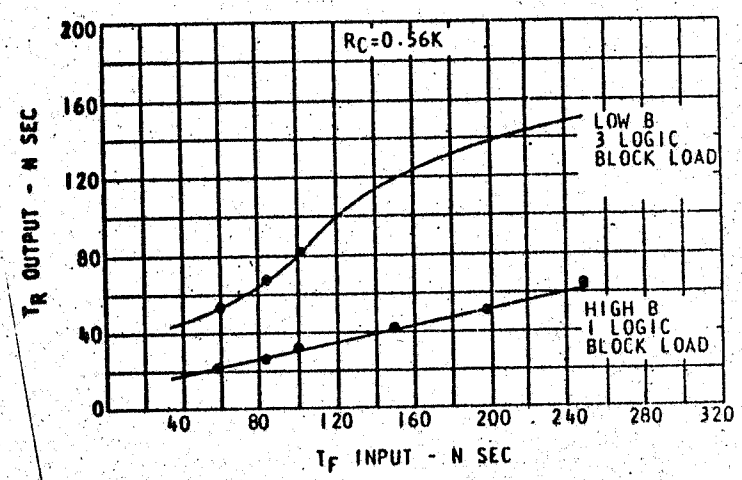
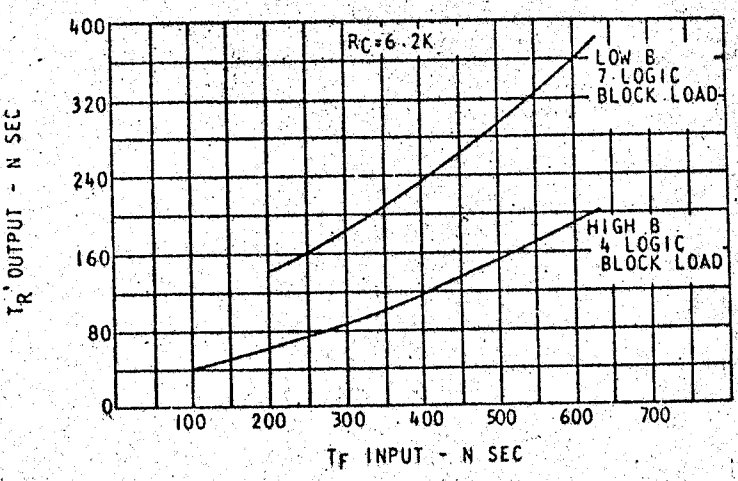
CARD CODE 729954

SHEET 2 OF 4

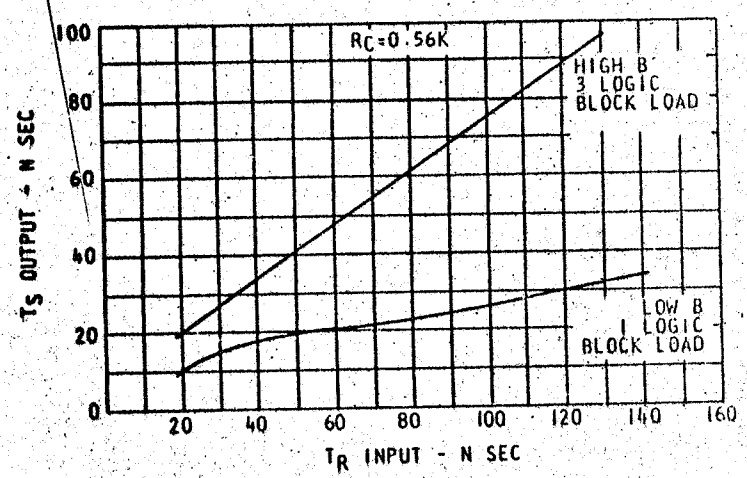
OUTPUT RISE TIME VS INPUT FALL TIME



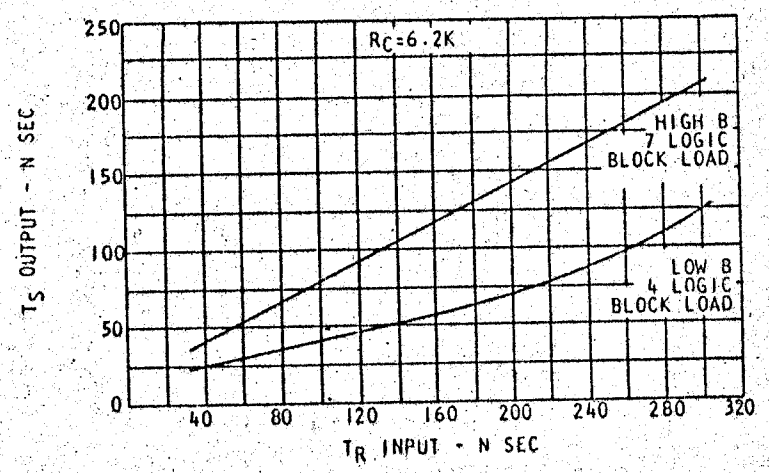
OUTPUT RISE TIME VS INPUT FALL TIME



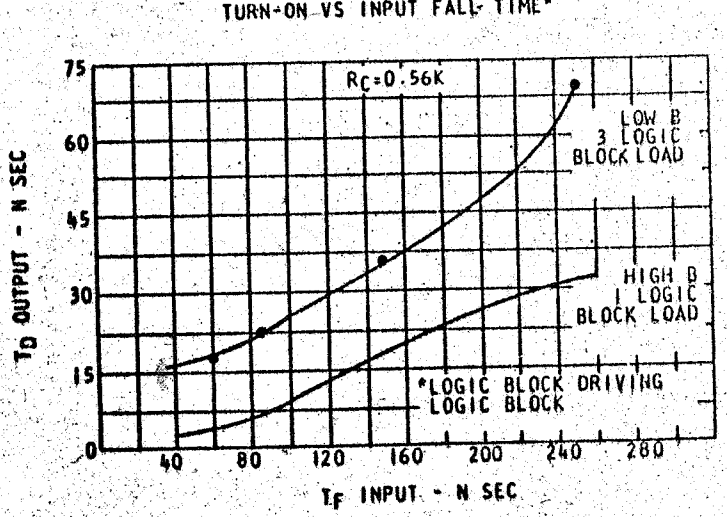
TURN-OFF VS INPUT RISE TIME



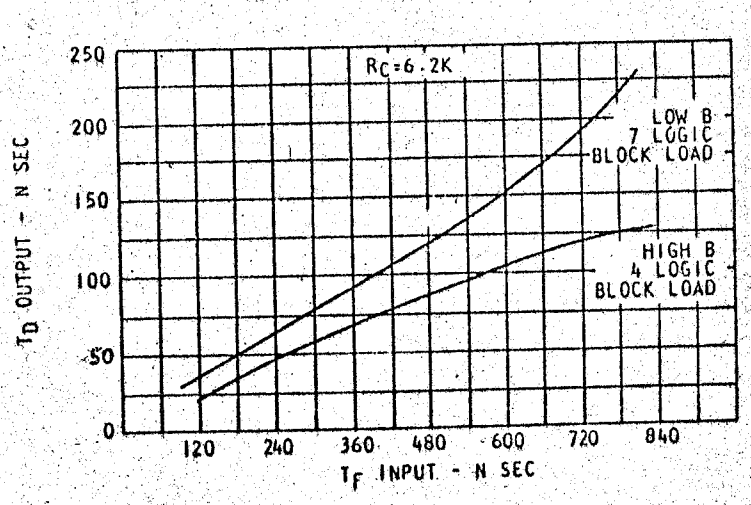
TURN-ON VS INPUT FALL TIME*



TURN-ON VS INPUT FALL TIME



TURN-OFF VS INPUT FALL TIME



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME SDTL Logic Penny				30.4.63	EC 115593					
2 NEG. - REC PULS				30.4.63	TT 83687					
DESIGN			MODEL							
DETAIL	WH	3-1-62	SCALE							
CHECK	RG	3-1-62	DRAW							
APPRD			CHECK							

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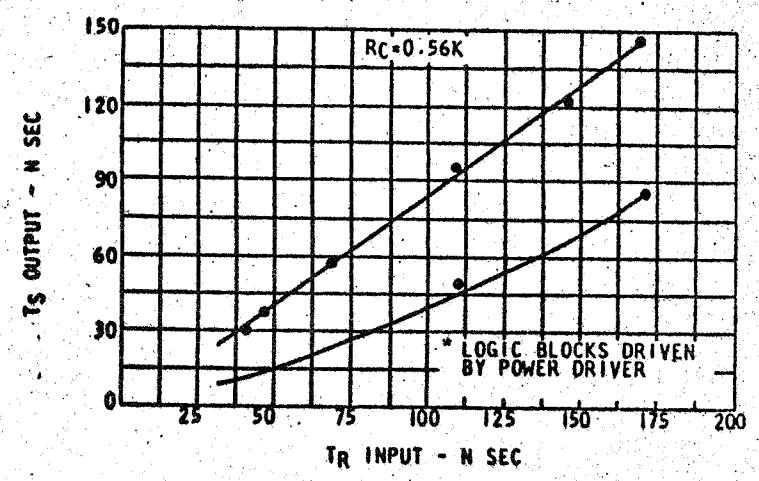
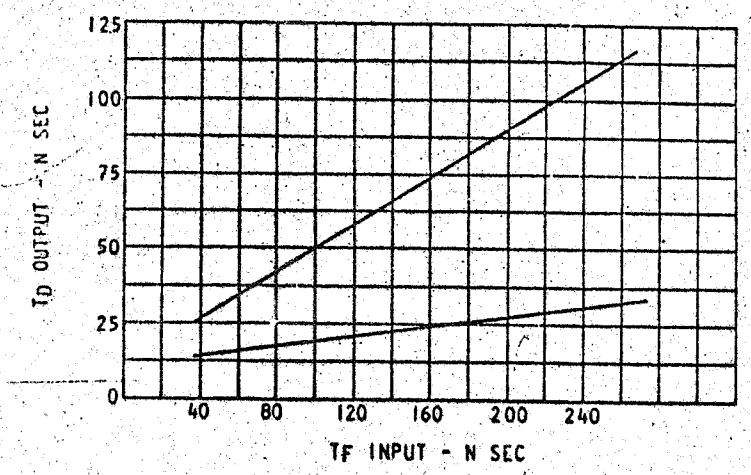
CARD CODE 729954

SHEET 3 OF 4

TURN-OFF VS RISE TIME INPUT*



TURN-ON VS FALL TIME INPUT (LOGIC BLOCK DRIVEN BY POWER DRIVERS)



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LOGIC DELAY				4-11-62	FC115599					
INFO - REF DWG.					30.4.62	TT83687					
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RG	3-1-62	DRAW								
APPRO			CHECK								

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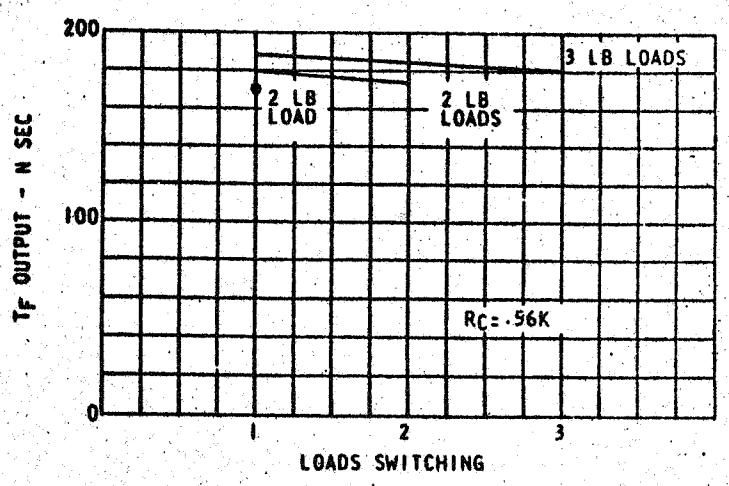
CARD CODE 729954

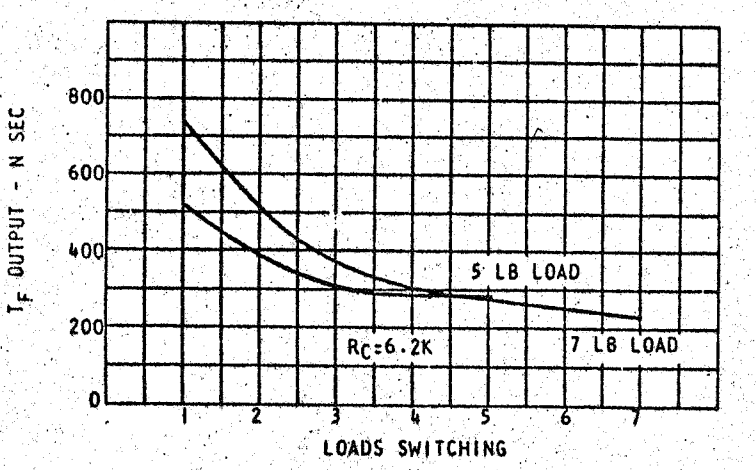
SHEET 4 OF 4

LOW SPEED SINGLE LEVEL LOGIC BLOCKS

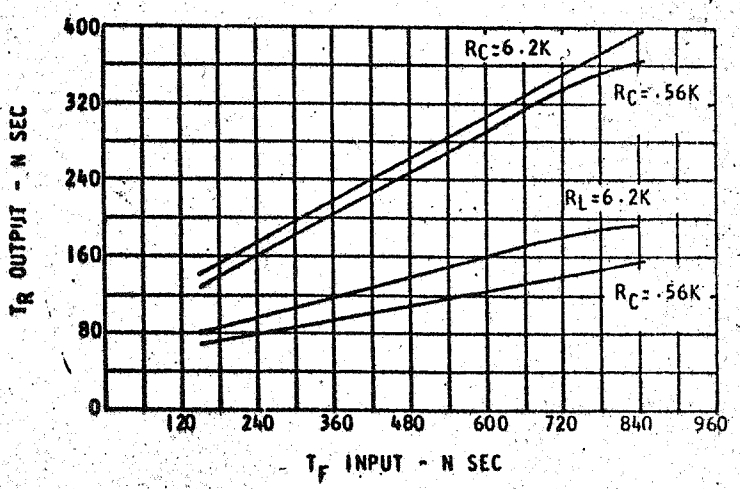
FALL TIME VS LOADING



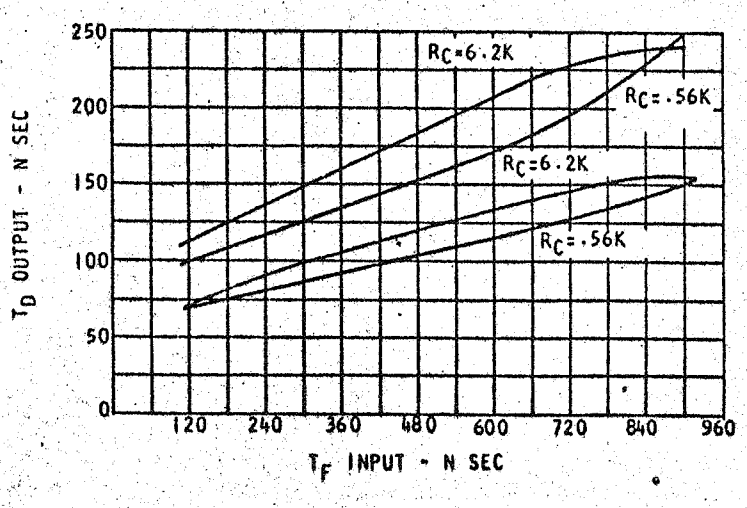
FALL TIME VS LOADING



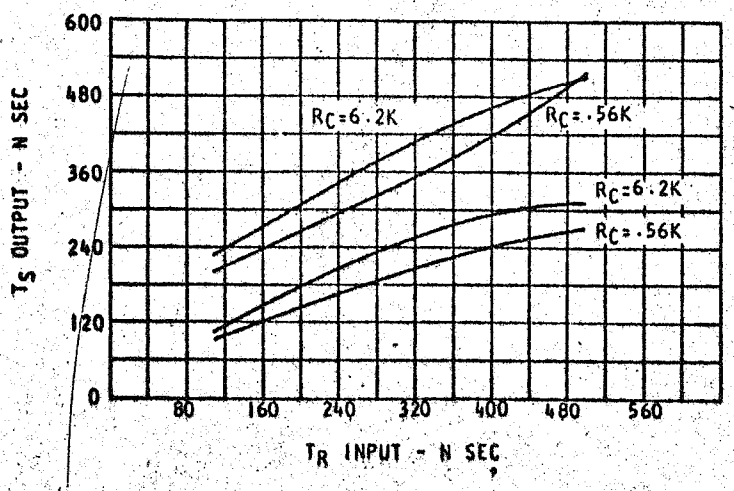
OUTPUT RISE TIME VS INPUT FALL TIME



TURN-OFF VS INPUT FALL TIME



TURN-OFF VS INPUT RISE TIME



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME SDTDL LOGIC DELAY					-62	EC 115599					729954
INFO. - REF DWG					30.463	JT 83687					
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RQ	3-1-62	DRAW								
APPRO			CHECK								

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STANDARDS CODE

CTDL DELAY INFORMATION

CARD CODE 729955

SHEET 1 OF 3

GENERAL

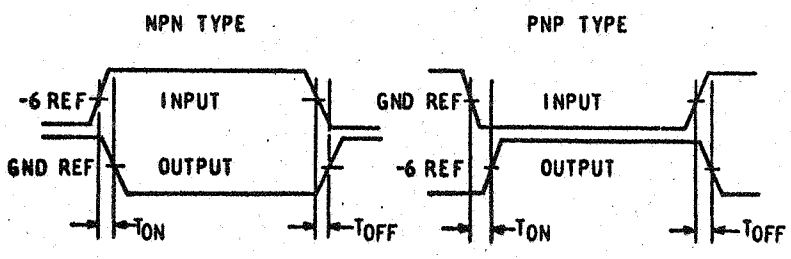
THE TURN ON, TURN OFF DELAYS OF THE CIRCUITS USED IN A PARTICULAR MACHINE ARE COMPLEX FUNCTIONS OF MANY VARIABLES SUCH AS THE TRANSISTOR DELAY, INPUT-OUTPUT LOADING, FALL AND RISE TIME, ETC.

THE DELAY SPECIFICATIONS ARE GIVEN BELOW AND ARE CLASSIFIED BY CIRCUIT TYPE.

WHEN POSSIBLE, REPRESENTATIVE RANGES OF DELAY ARE GIVEN ON EACH INDIVIDUAL CIRCUIT SHEET AND SHOULD BE USED AS A GUIDE. SPECIFIC CIRCUIT APPLICATION AND/OR CAPACITIVE LOAD (EXAMPLE: WIRE CAPACITANCE) MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES.

THE FOLLOWING INFORMATION IS PROVIDED FOR THOSE CASES WHERE CARD REPLACEMENT DOES NOT RESULT IN IMPROVEMENT AND A MORE DETAILED ANALYSIS IS NECESSARY.

THE DELAY OF THE SIGNAL IN THE CTDL BLOCKS IS A FUNCTION OF THE TRANSISTOR DELAYS PLUS THE LOADING EFFECTS OF THE INPUT AND OUTPUT CIRCUITS. DELAYS FOR SEVERAL STAGES IN CASCADE ARE NUMERICALLY EQUAL TO THE SUM OF INDIVIDUAL STAGES. UNLESS OTHERWISE STATED, DELAYS ARE MEASURED FROM THE TIME THE INPUT SIGNAL CROSSES ITS REFERENCE VOLTAGE TO THE TIME THE OUTPUT SIGNAL CROSSES ITS REFERENCE VOLTAGE, AS SHOWN.



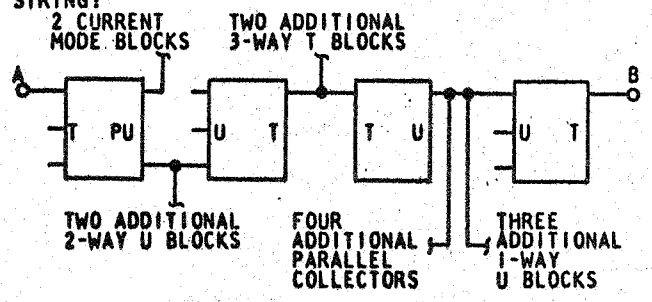
BASIC LOGIC BLOCK DELAY INFORMATION

DATA FOR CALCULATION OF DELAY IN A STRING OF LOGIC WHEN DRIVING CTDL BLOCKS FROM THE CTDL OUTPUT AND CURRENT MODE BLOCKS FROM THE CURRENT MODE OUTPUT.

	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX	MIN	MAX	MIN
DELAY PER PNP BLOCK IN STRING	.70	.20	.18	.06
DELAY PER NPN BLOCK IN STRING	.52	.18	.12	.05
ADDITIONAL DELAY ON STRING				
FOR THE FIRST PNP TYPE LOAD	.00	-.03	.22	.06
FOR THE SECOND PNP TYPE LOAD	.00	-.03	.30	.07
FOR THE THIRD PNP TYPE LOAD	.00	-.03	.40	.08
FOR THE FOURTH PNP TYPE LOAD	.00	-.03	.50	.10
FOR THE FIRST NPN TYPE LOAD	-.01	-.03	.09	.01
FOR THE SECOND NPN TYPE LOAD	-.01	-.03	.13	.02
FOR THE THIRD NPN TYPE LOAD	-.01	-.03	.18	.03
FOR THE FOURTH NPN TYPE LOAD	-.01	-.03	.22	.04
DELAY PER PNP TYPE CS LOADS ON STRING	.02	.00	.02	.005
DELAY PER NPN TYPE CS LOADS ON STRING	.015	.00	.02	.005
DELAY PER PARALLEL COLLECTOR	.007	.00	.01	.004
DELAY PER DIODE INPUT	*.02	.00	.005	.000
DELAY PER 100 PF	.05	.02	.06	.03

* WIRES ASSUMED ON GATES -- INCLUDES WIRING CAPACITANCE EFFECT BETWEEN ADJACENT CARDS.

EXAMPLE OF CTDL DELAY LOGIC STRING. CONSIDER THE FOLLOWING LOGIC STRING:



IN THIS EXAMPLE ALL MAXIMUM DELAYS WILL BE USED:

TURN ON DELAY

2 T BLOCKS	2 X 0.7	= 1.4
2 U BLOCKS	2 X 0.52	= 1.04
5 ADDITIONAL U BLOCKS	5 X(-0.01)	= -0.05
2 ADDITIONAL T BLOCKS	0	= 0
2 P-TYPE CS BLOCK	2 X 0.015	= 0.03
4 PARALLEL COLLECTORS	4 X 0.007	= 0.028
23 INPUT DIODES	23 X 0.02	= 0.46
TOTAL TURN ON DELAY FROM A TO B		2.908 U SEC

TURN OFF DELAY

2 T BLOCKS	2 X 0.18	= 0.36
2 U BLOCKS	2 X 0.12	= 0.24
2 IST U BLOCK LOAD	2 X 0.09	= 0.18
2 2ND U BLOCK LOAD	2 X 0.13	= 0.26
1 3RD U BLOCK LOAD	0.18	= 0.18
1 IST T BLOCK LOAD	0.22	= 0.22
1 2ND T BLOCK LOAD	0.30	= 0.30
2 P-TYPE CS BLOCK	2 X 0.02	= 0.04
4 PARALLEL COLLECTORS	4 X 0.01	= 0.04
23 INPUT DIODES	23 X 0.005	= 0.115
TOTAL TURN OFF DELAY FROM A TO B		1.935 U SEC

LOGIC INVERTER

	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX	MIN	MAX	MIN
DELAY PER PNP INVERTER IN STRING	-.08	-.14	.55	.06
DELAY PER NPN INVERTER IN STRING	0	+.06	.41	-.02
ADDER LOGIC INVERTER DELAY:				
PER PNP INPUT LOAD	0	0	.015	.01
PER PNP OUTPUT LOAD	0	-.005	.01	.006
PER NPN INPUT LOAD	-.02	-.01	.04	.02
PER NPN OUTPUT LOAD	0	0	.01	0
DELAY ACROSS PNP BLOCK DRIVING LOGIC INVERTER IN STRING	.81	.26	.30	.26
DELAY ACROSS NPN BLOCK DRIVING LOGIC INVERTER IN STRING	.38	.28	.20	.14
ADDITIONAL DRIVING BLOCK DELAY				
PER PNP INPUT LOAD	0	0	0	0
PER PNP OUTPUT LOAD	0	-.02	.01	0
PER NPN INPUT LOAD	0	0	0	0
PER NPN OUTPUT LOAD	-.013	-.043	.01	.01
DELAY ACROSS PNP BLOCK DRIVEN BY LOGIC INVERTER	.74	.32	.22	.20
ADDITIONAL DELAY DUE TO INVERTER OUTPUT LOADING				
1ST PNP BLOCK	0	0	.16	.07
2ND PNP BLOCK	0	-.02	.22	.08
3RD PNP BLOCK	0	-.02	.33	.09
4TH PNP BLOCK	0	-.01	.39	.11
DELAY ACROSS NPN BLOCK DRIVEN BY LOGIC INVERTER	.35	.28	.17	.09
ADDITIONAL DELAY DUE TO INVERTER OUTPUT LOADING				
1ST NPN BLOCK	-.02	-.02	.18	.08
2ND NPN BLOCK	-.01	-.01	.21	.10
3RD NPN BLOCK	-.01	-.02	.22	.10
4TH NPN BLOCK	-.01	-.02	.42	.15

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CTDL DELAY INFO. - REF. DWG.			6-29-62	EC 115599					729955
DESIGN			MODEL	30.4-63	JT83687					
DETAIL	WH	3-1-62	SCALE							
CHECK	RO	3-1-62	DRAW							
APPRO			CHECK							

C

LIG 6-4-62

729955 /1

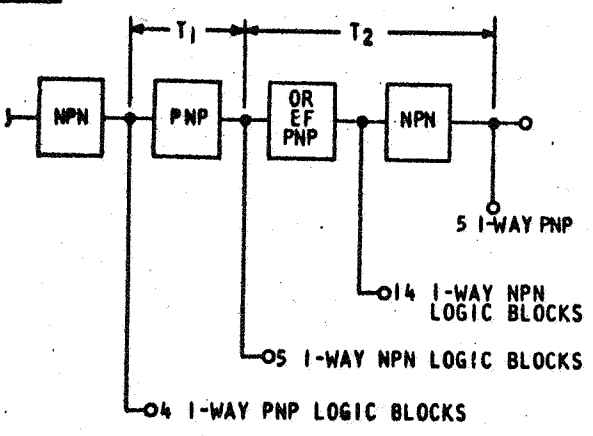
729955 STANDARDS CODE

729955 CARD CODE

E, F "OR" CIRCUITS

DELAY INFORMATION

TEST CIRCUIT



PNP EMITTER "OR" DELAY (U SEC)

	T_1 T_{ON} MAX.	T_1 T_{ON} MIN.	T_1 T_{OFF} MAX.	T_1 T_{OFF} MIN.	T_2 T_{ON} MAX.	T_2 T_{ON} MIN.	T_2 T_{OFF} MAX.	T_2 T_{OFF} MIN.
DELAY PER BLOCK	.92	.28	.15	.10	.50	.12	.12	.12
DELAY PER ADDED BLOCK ON DRIVER INPUT	.00	.00	.06	.03	.00	.01	.02	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER OUTPUT	.00	-.01	.00	.00	.01	-.02	.04	.06
DELAY PER ADDED CTDL BLOCK ON E.F.	.01	-.008	.00	.00	.00	-.01	.006	.01
DELAY PER ADDED CTDL BLOCK ON DRIVER BLOCK	.01	.00	.00	.00	-.03	-.01	.00	.00
DELAY W/3 E.F. ON DRIVER - NO LOAD R IN DRIVER	.29	.28	.30	.10	.50	.25	.24	.12
DELAY PER ADDED E.F.	.00	-.02	.02	.00	.00	.00	-.01	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER INPUT	.00	-.01	.02	.00	.00	-.005	-.005	.00
DELAY PER ADDED BLOCK ON E.F. OUTPUT	.00	.002	.002	.00	.00	-.01	.015	.00
DELAY PER ADDED BLOCK ON DRIVER BLOCK	.00	.00	.004	.00	.00	-.02	.00	.00

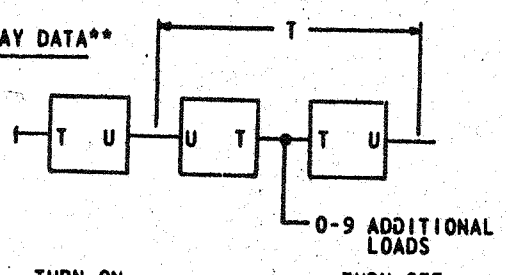
NPN EMITTER "OR" DELAY (U SEC)

	T_1 T_{ON} MAX.	T_1 T_{ON} MIN.	T_1 T_{OFF} MAX.	T_1 T_{OFF} MIN.	T_2 T_{ON} MAX.	T_2 T_{ON} MIN.	T_2 T_{OFF} MAX.	T_2 T_{OFF} MIN.
DELAY PER BLOCK	.42	.36	.15	.14	.70	.19	.10	.06
DELAY PER ADDED BLOCK ON DRIVER	-.02	.01	.05	.08	.00	.00	.01	.02
DELAY PER ADDED CTDL BLOCK ON DRIVER OUTPUT	-.01	-.01	.005	.00	.00	.00	.03	.01
DELAY FER ADDED CTDL BLOCK ON E.F.	.00	.00	.00	.00	.00	.002	.005	.005

	T_{ON} MAX.	T_{ON} MIN.	T_{OFF} MAX.	T_{OFF} MIN.	T_{ON} MAX.	T_{ON} MIN.	T_{OFF} MAX.	T_{OFF} MIN.
DELAY PER ADDED CTDL BLOCK ON DRIVER BLOCK	.00	.00	.00	.00	-.04	.00	.00	.00
DELAY W/3 E.F. ON DRIVER - NO LOAD R IN DRIVER	.32	.36	.15	.14	.70	.20	.16	.06
DELAY PER ADDED E.F.	.02	.00	-.02	.00	.00	.00	.00	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER INPUT	.00	-.02	.02	.00	.00	.00	.01	.00
DELAY PER ADDED BLOCK ON E.F. OUTPUT	.005	.00	.00	.00	-.005	.00	.01	.00
DELAY PER ADDED BLOCK ON DRIVER BLOCK	.01	.00	.00	.00	-.01	-.00	.00	.00

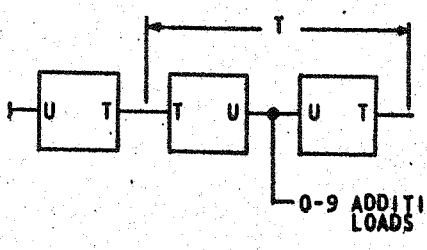
TRANSLATE BLOCK DELAY DATA

NPN BLOCK



TOTAL NUMBER OF LOADS	TURN ON (U SEC) MAX.	TURN ON (U SEC) MIN.	TURN OFF (U SEC) MAX.	TURN OFF (U SEC) MIN.
1	.70	.16	.34	.12
2	.70	.16	.36	.13
3	.70	.16	.40	.14
4	.70	.17	.43	.15
5	.70	.17	.46	.16
6	.70	.18	.48	.17
7	.70	.18	.50	.18
8	.70	.18	.51	.19
9	.70	.19	.57	.20
10	.70	.20	.60	.21

PNP BLOCK



TOTAL NUMBER OF LOADS	TURN ON (U SEC) MAX.	TURN ON (U SEC) MIN.	TURN OFF (U SEC) MAX.	TURN OFF (U SEC) MIN.
1	.52	.17	.26	.14
2	.52	.17	.31	.16
3	.52	.17	.35	.17
4	.52	.18	.38	.19
5	.53	.18	.41	.20
6	.53	.18	.44	.21
7	.53	.19	.47	.22
8	.53	.19	.50	.23
9	.53	.19	.54	.24
10	.53	.20	.56	.25

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CTDL DELAY INFO. - REF. DWG.				6-28-62 30.4.53	FC113599 TT83687					729955
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RG	3-1-62	DRAW								
APPRO			CHECK								

C

LIG 6-4-62

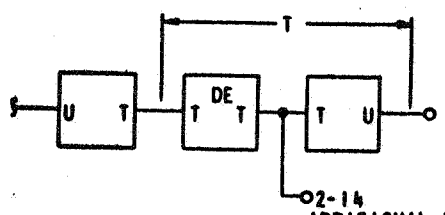
729955

729955 STANDARDS CODE

CARD CODE 729955

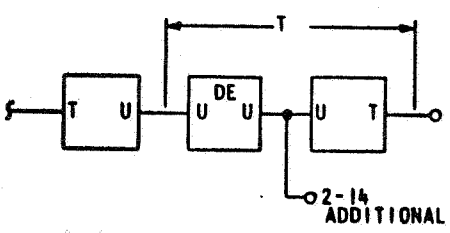
EMITTER FOLLOWER DELAY

NPN



TOTAL NUMBER OF LOADS	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX.	MIN.	MAX.	MIN.
3	.68	.14	.25	.05
4	.68	.15	.26	.06
5	.68	.16	.27	.06
6	.68	.17	.27	.07
7	.68	.18	.29	.07
8	.68	.19	.30	.08
9	.68	.20	.31	.08
10	.68	.21	.32	.08
11	.68	.21	.33	.08
12	.68	.21	.34	.08
13	.68	.22	.35	.09
14	.68	.22	.36	.09
15	.68	.23	.37	.09

PNP



TOTAL NUMBER OF LOADS	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX.	MIN.	MAX.	MIN.
3	.48	.18	.17	.06
4	.50	.19	.18	.06
5	.52	.20	.19	.07
6	.54	.21	.21	.07
7	.56	.22	.22	.08
8	.58	.23	.23	.08
9	.59	.24	.24	.09
10	.59	.24	.26	.09
11	.60	.25	.28	.09
12	.60	.26	.29	.10
13	.61	.26	.30	.10
14	.61	.27	.31	.10
15	.62	.27	.33	.10

CURRENT MODE BLOCK WITH CTDL COUPLING NETWORK

DELAY DATA

	TURN ON (U SEC) IN PHASE MIN	IN PHASE MAX	INVERTED MIN	INVERTED MAX
BASIC N BLOCK DELAY	.100	.100	.150	.200
PER CTDL BLOCK LOAD	-.010	-.005	-.020	-.005
PER ADDED FAN-IN DIODE	-.002	-.002	-.001	-.001
BASIC P BLOCK DELAY	.080	.110	.210	.240
PER CTDL BLOCK LOAD	.000	.010	-.020	-.005
PER ADDED FAN-IN DIODE	-.001	-.001	-.002	-.002
BASIC CTDL PNP DELAY	.230	.560	.200	.500
PER CTDL BLOCK LOAD	.000	.020	.000	.020
PER ADDED FAN-IN DIODE	-.020	-.020	-.022	-.012
BASIC CTDL NPN DELAY	.200	.450	.180	.400
PER CTDL BLOCK LOAD	.020	.020	-.010	-.010
PER ADDED FAN-IN DIODE	.015	.030	-.018	-.006

	TURN OFF (MU SEC) IN PHASE MIN	IN PHASE MAX	INVERTED MIN	INVERTED MAX
BASIC N BLOCK DELAY	.090	.090	.090	.130
PER CTDL BLOCK LOAD	.010	.010	.010	.010
PER ADDED FAN-IN DIODE	.001	.001	.001	.001
BASIC P BLOCK DELAY	.060	.130	.100	.120
PER CTDL BLOCK LOAD	.000	.020	.010	.010
PER ADDED FAN-IN DIODE	.002	.002	-.001	-.001
BASIC CTDL PNP DELAY	.060	.340	.140	.350
PER CTDL BLOCK LOAD	.020	.100	.000	.100
PER ADDED FAN-IN DIODE	.002	.021	.012	.020
BASIC CTDL NPN DELAY	.160	.220	.140	.170
PER CTDL BLOCK LOAD	.100	.260	.060	.290
PER ADDED FAN-IN DIODE	.005	.010	.005	.010

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CTDL DELAY INFO. - REF. DWG				6-29-62	EC 115599					729955
					30.4.63	JT 83687					
DESIGN			MODEL								
DETAIL	WM	3-1-62	SCALE								
CHECK	RG	3-1-62	DRAW								
APPRD			CHECK								

C

LIG 6-4-62

729956

STANDARDS CODE

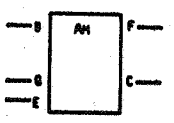
CARD CODE A S U - 729956

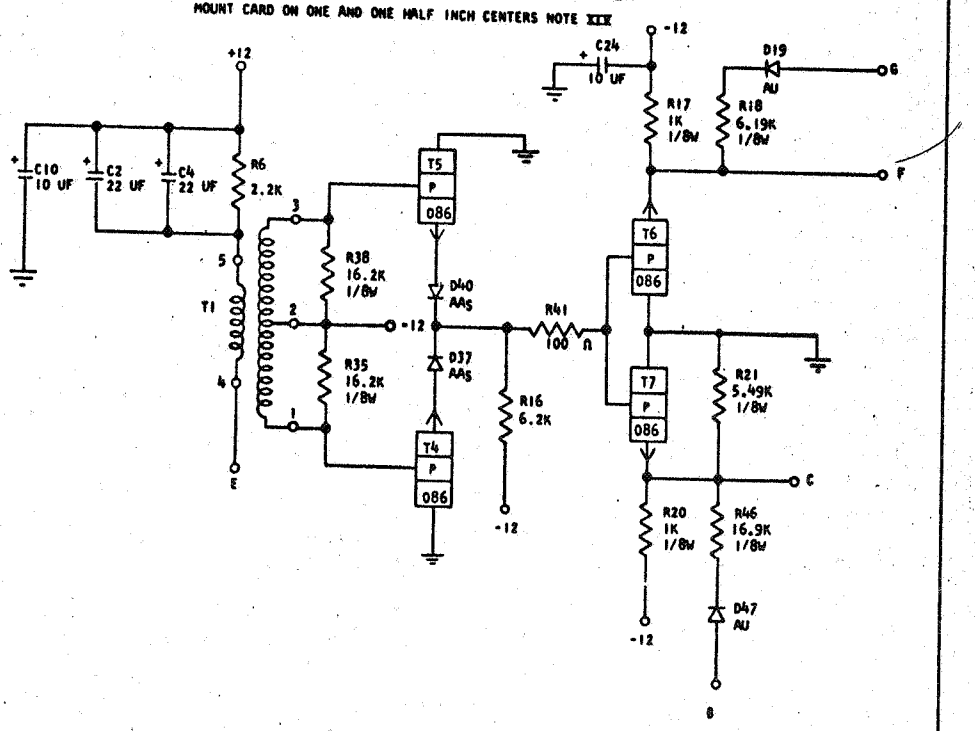
REFERENCE DRAWING

SEE PRODUCTION DRAWING 372285

SENSE AMPLIFIER-RECTIFIER AND CLIPPER

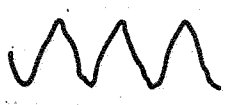
MOUNT CARD ON ONE AND ONE HALF INCH CENTERS NOTE XIX

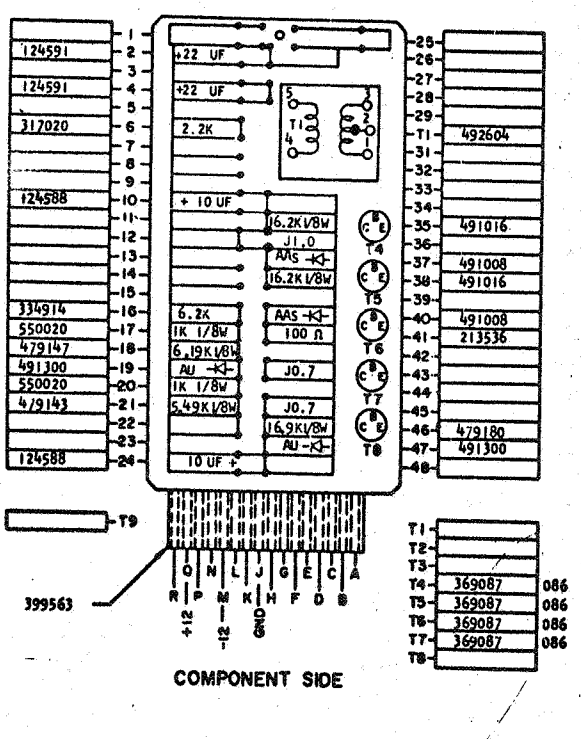




APPLICATION NOTES

VOLTAGES AT PIN G AND B FROM CLIPPING CARD

	INPUT WAVE FORM AT PIN E 8.0VP-P NOMINAL 11.5VP-P MAXIMUM REFERENCE LEVEL +1.59V TO -3.88V
	OUTPUT WAVE FORM AT PIN C OR F 1. LOW ACCEPTANCE CHANNEL 0V TO 13V P-P READ CONDITIONS 0V TO 11.1V P-P READ WHILE WRITE CONDITIONS 2. HIGH ACCEPTANCE CHANNEL 0V TO 10.7V P-P READ CONDITIONS 0V TO 11.5V P-P READ WHILE WRITE CONDITION



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729956
NAME	CARD ASM TSTR - SENSE AMPLIFIER-RECTIFIER AND CLIPPER					6-29-62	115599						
DESIGN			MODEL	SMS		30.4.63	JT83687						
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRO			CHECK										

C

STANDARDS CODE

729957

CARD CODE | 729957

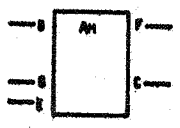
D Z A -

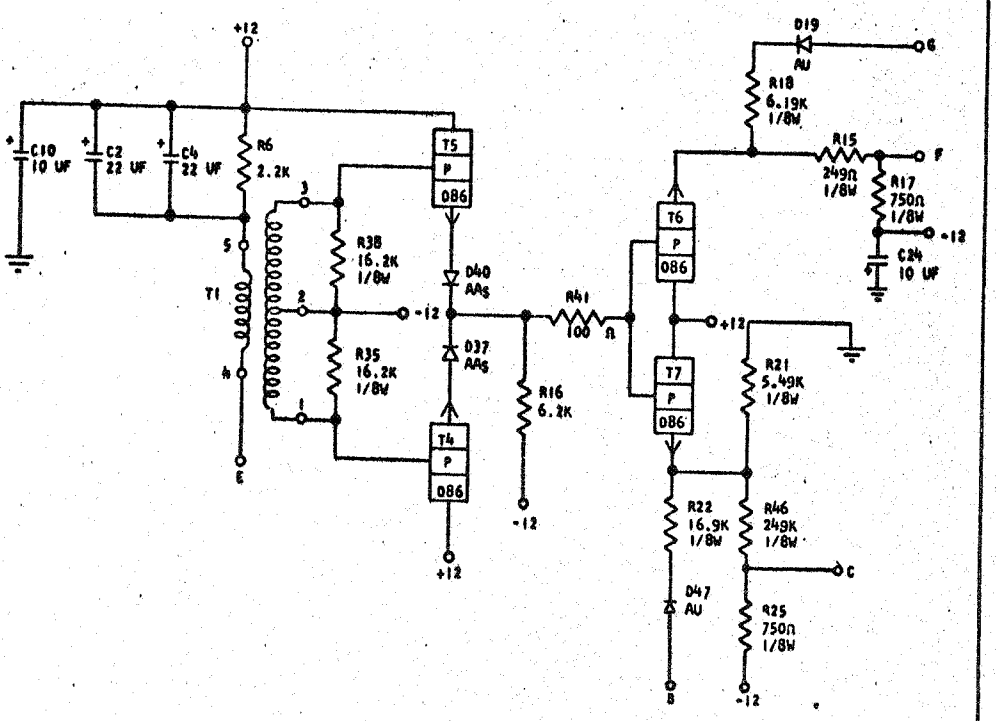
REFERENCE DRAWING

SEE PRODUCTION DRAWING 372359

SENSE AMPLIFIER-RECTIFIER AND CLIPPER

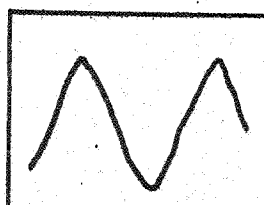
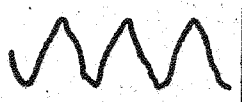
MOUNT CARD ON ONE AND ONE HALF INCH CENTERS NOTE XXX

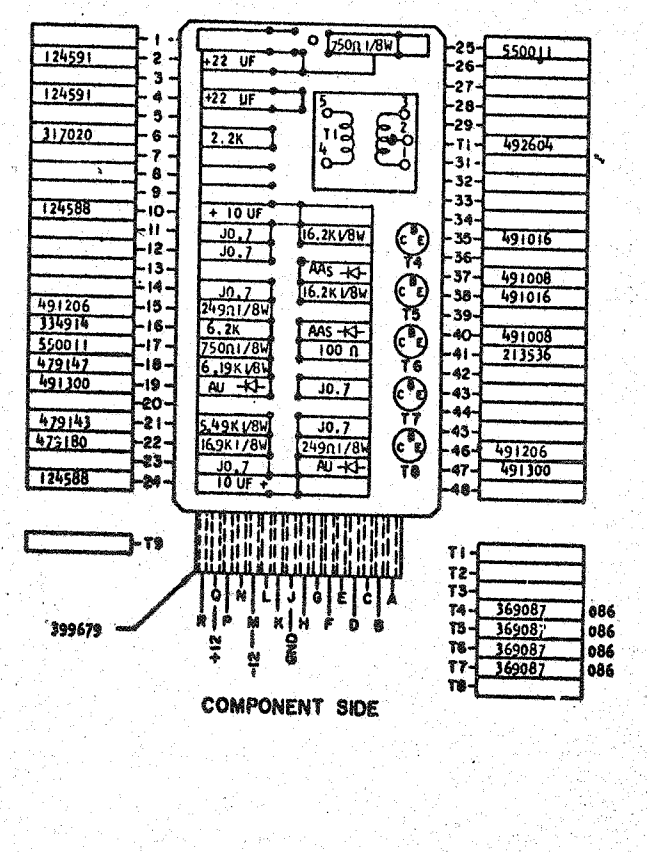




APPLICATION NOTES

VOLTAGES AT PIN B AND G FROM CLIPPING CARD

	INPUT WAVE FORM AT PIN E 10.1VP-P NOMINAL 11.2VP-P MAXIMUM REFERENCE LEVEL +1.59V TO -3.88V
	OUTPUT WAVE FORM AT PIN C OR F 1. LOW ACCEPTANCE CHANNEL 0V TO .05V REF TO -12V, READ COND. 1.55V TO 1.91V REF TO -12V, READ WHILE WRITE CONDITION. 2. HIGH ACCEPTANCE CHANNEL 1.92V TO 2.18V REF TO -12V, READ CONDITION. 2.53V TO 2.90V REF TO -12V, READ WHILE WRITE CONDITION.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR - SENSE AMPLIFIER-RECTIFIER AND CLIPPER					6-21-62	EC115599						729957
DESIGN			MODEL	SMS		30.4.63	JT83687						
DETAIL	RG	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIG	3-17-62								
APPRO			CHECK										

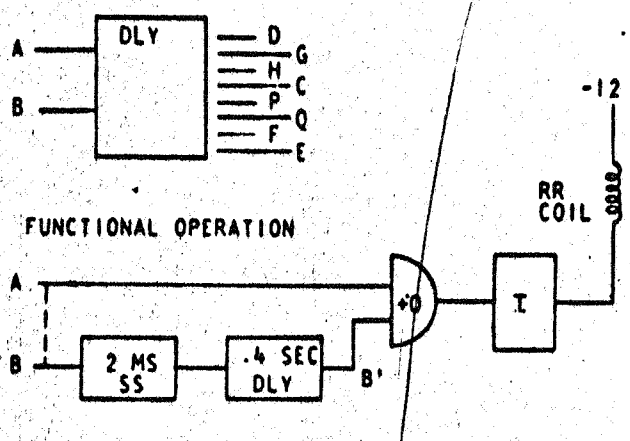
C

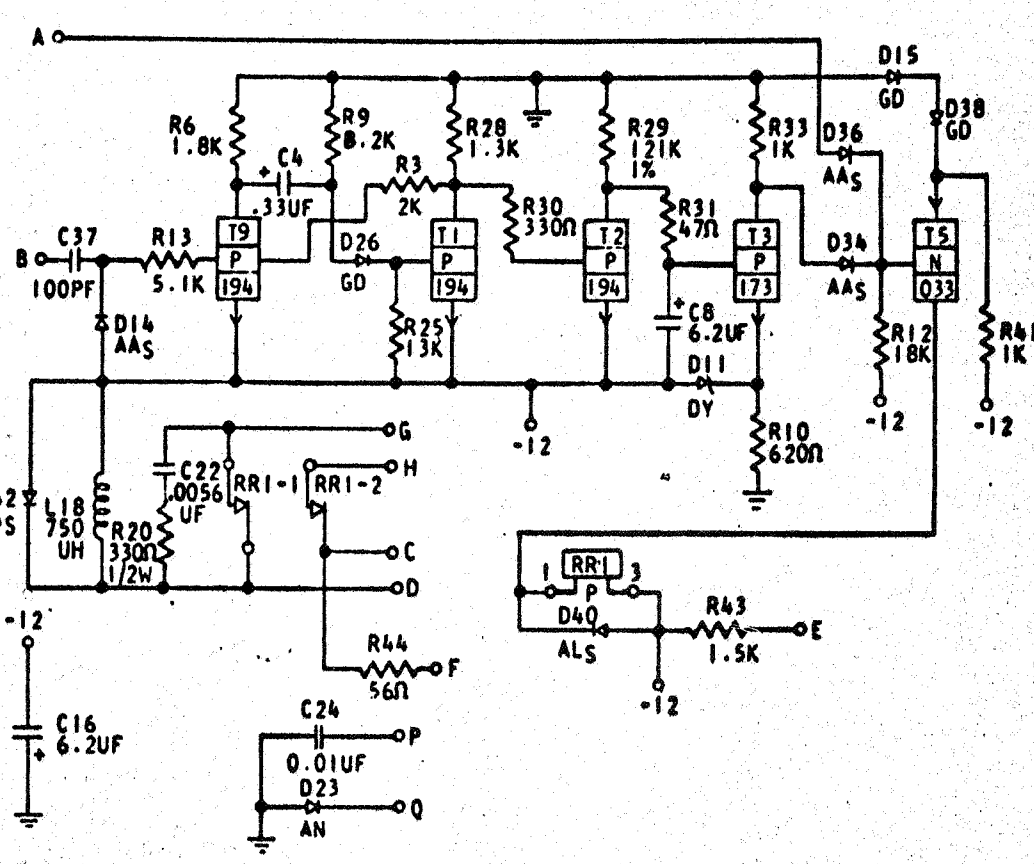
740601 | STANDARDS CODE

CARD CODE 740601 | Z K V -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 372687





SEQUENCE OF OPERATION

1. NORMAL OPERATION PINS A AND B TIED TOGETHER (DRIVE ETMS FROM PIN G).
2. POSITIVE GOING INPUT ON PIN B CAUSES B' TO TIME OUT 400 MILLSEC. (SEE TIMING CHART).
3. THE N.C. REED RELAY IS DE-ENERGIZED (POINTS CLOSED) FOR A OR B' UP (METER RUN CONDITION).
4. FOR A ONLY. IN THE UP LEVEL THE NC REED RELAY IS DE-ENERGIZED (POINTS CLOSED). FOR A ONLY, IN THE DOWN N.C. REED RELAY IS ENERGIZED (POINTS OPEN).
5. THE LEVEL OF THE WAVE FORM APPEARING AT RR1-2 IS DEPENDENT ON TYPE OF LOGIC BEING DRIVEN.

A. FOR DRIVING INTO CTRL, CTDL, SDTDL AND SDTRL CONNECT THE FOLLOWING:

FROM	TO
E	F
F	P
H	J

DRIVE FROM PIN E

B. FOR DRIVING CURRENT MODE, CONNECT THE FOLLOWING:

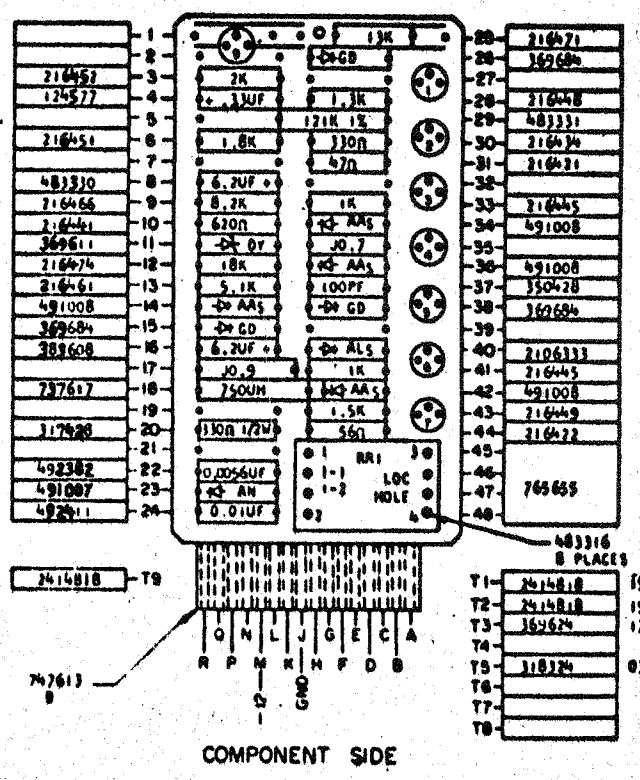
FROM	TO
C	-36 OR -48
H	UNIV INTEGRATOR WITH "P" OR "N" OUTPUT

C. FOR DRIVING INTO DDTL LOGIC, CONNECT THE FOLLOWING:

FROM	TO
E	C
H	O
O	P

DRIVE FROM PIN H

PIN	SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A ONLY	DIODE INPUT		UP	-.81	+6.27
			DOWN	-3.0	-15
G	RR1-1 OUTPUT		UP	--	--
			DOWN	-11.00	-12.48
A TO B	INPUT	T>.4 SEC, T<.4 SEC	POS. GOING SHIFT	5.1	13.20
B'-G	RR1-1 OUTPUT	.4 SEC, .4 SEC, .4 SEC	DOWN	-11.00	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASSEMB. Y TSTR - ETM			9-20-63	11898						740601
	DELAY CIRCUIT			16263	TA1841C						
DESIGN	FVL	8-8-63	MODEL								
DETAIL	FVL	8-8-63	SCALE								
CHECK	---	"	DRAW								
APPRO	GWS	8-9-63	CHK								

C

V8476 C

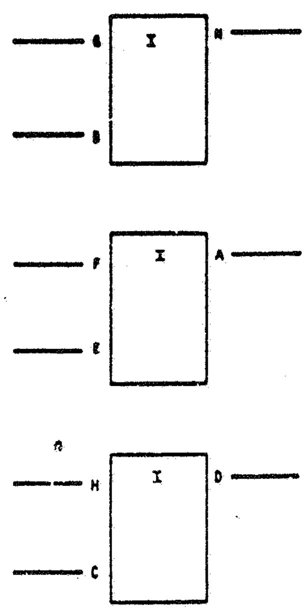
741416

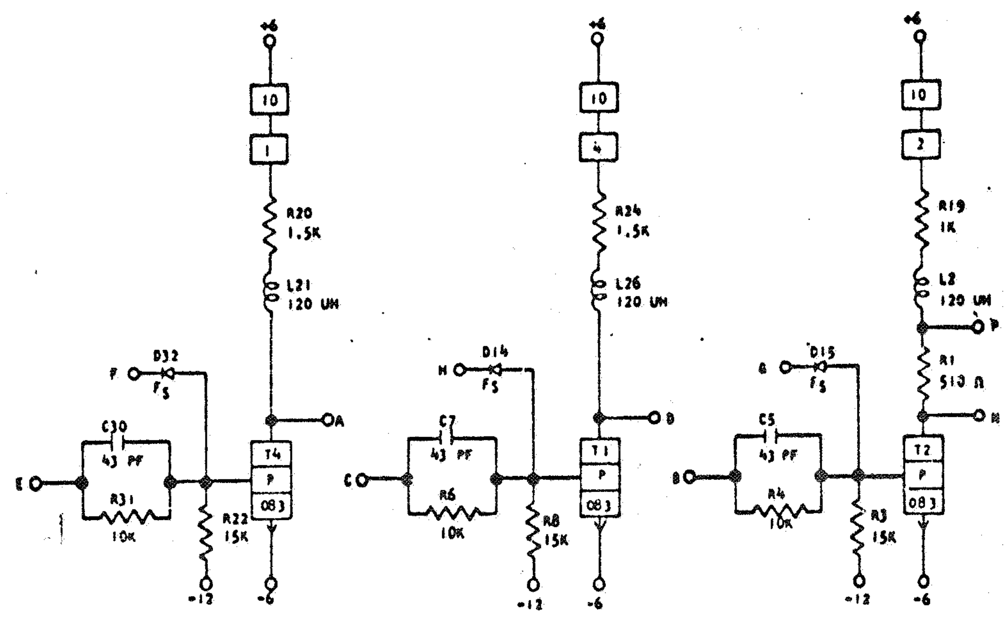
CARD CODE	741416
H B W W	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371500

CAP SENSE AMPLIFIER





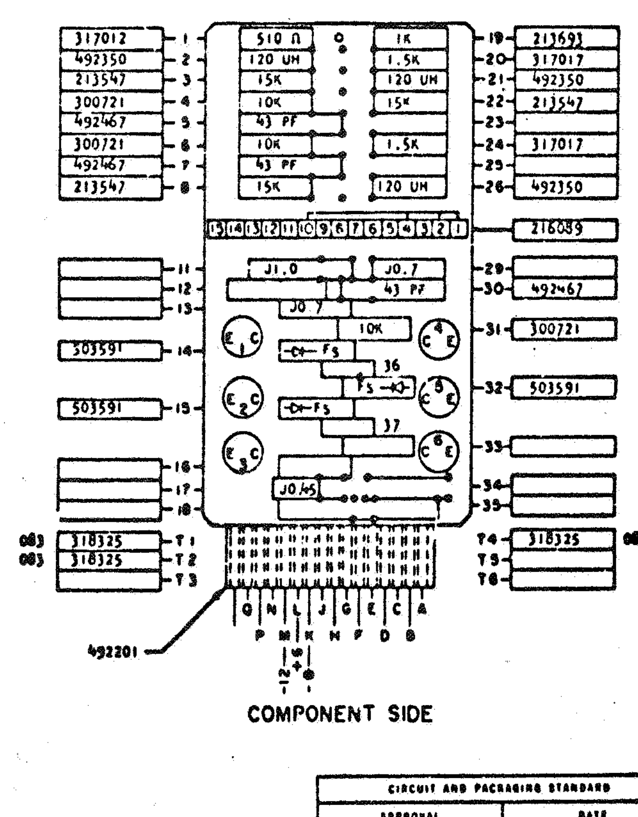
SEQUENCE OF OPERATION

1. GATE AND SIGNAL UP, TRANSISTOR ON, DOWN OUTPUT.
2. GATE OR SIGNAL DOWN, TRANSISTOR OFF, UP OUTPUT.
3. INPUT DOWN, TRANSISTOR OFF, OUTPUT UP.
4. INPUT UP, TRANSISTOR ON, OUTPUT DOWN.
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
B, E, C	T	INPUT SIGNAL		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
G, F, H	U	INPUT GATE		UP	-5.46	+0.24
				DOWN	-7.44	-12.48
N, A, D	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24

DELAYS - USEC

	MINIMUM	MAXIMUM
TURN ON	0	0.07
TURN OFF	0.20	0.55



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

APPROVAL	CHECK	MAT. LAB.	COMP. LAB.
	[signature]		
26.6.	64		

C

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-CAP SENSE AMPLIFIER.	3-25-64	120123	[signature]				
DESIGN / MODEL	26.6.64	TA 769					
DETAIL / SCALE							
CHECK / DRAW VE 2-12-64							
APPRO [signature] 64 / CHECK							

741416

741416

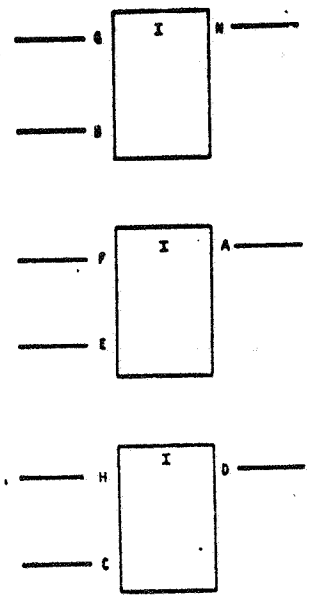
CARD CODE	741800
H B - -	

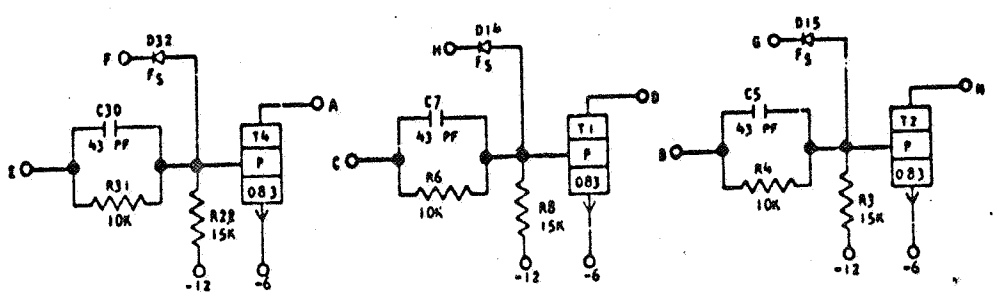
741800 STANDARDS CODE

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371561

CAP SENSE AMPLIFIER - NO LDS





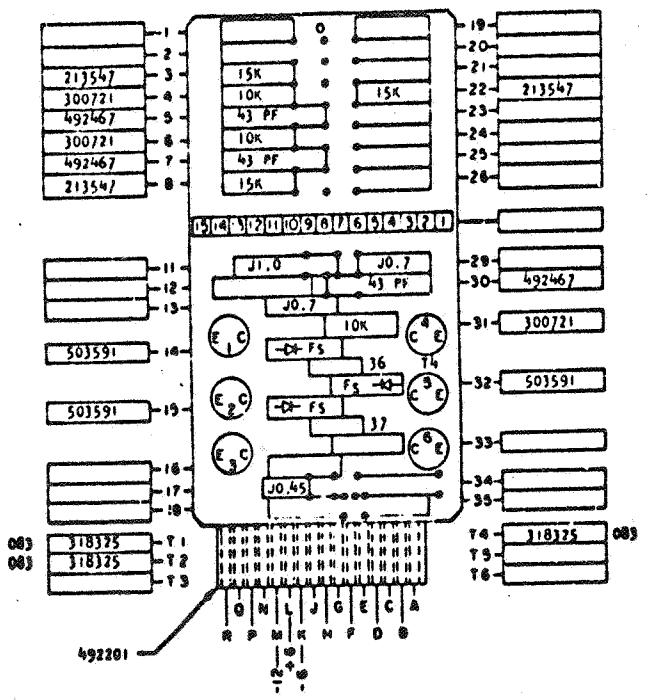
SEQUENCE OF OPERATION

1. GATE AND SIGNAL UP, TRANSISTOR ON, DOWN OUTPUT
2. GATE OR SIGNAL DOWN, TRANSISTOR OFF, UP OUTPUT
3. INPUT DOWN, TRANSISTOR OFF, OUTPUT UP.
4. INPUT UP, TRANSISTOR ON, OUTPUT DOWN.
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PIN	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
B, E, C	T	INPUT SIGNAL		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
G, F, H	U	INPUT GATE		UP	-5.46	+0.24
				DOWN	-7.44	-12.48
N, A, D	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24

DELAYS - USEC

	MINIMUM	MAXIMUM
TURN ON	0	0.07
TURN OFF	0.20	0.55



COMPONENT SIDE

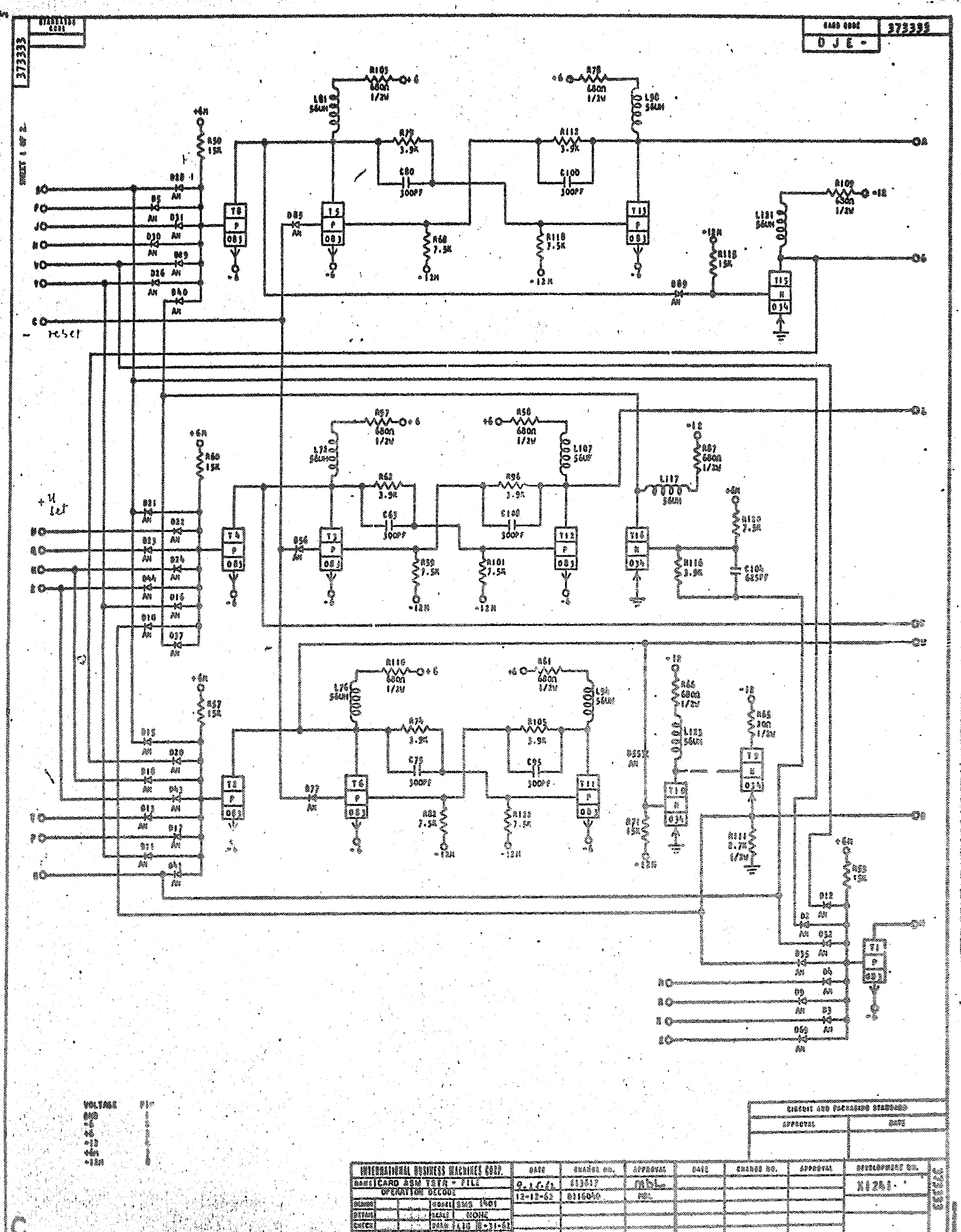
CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

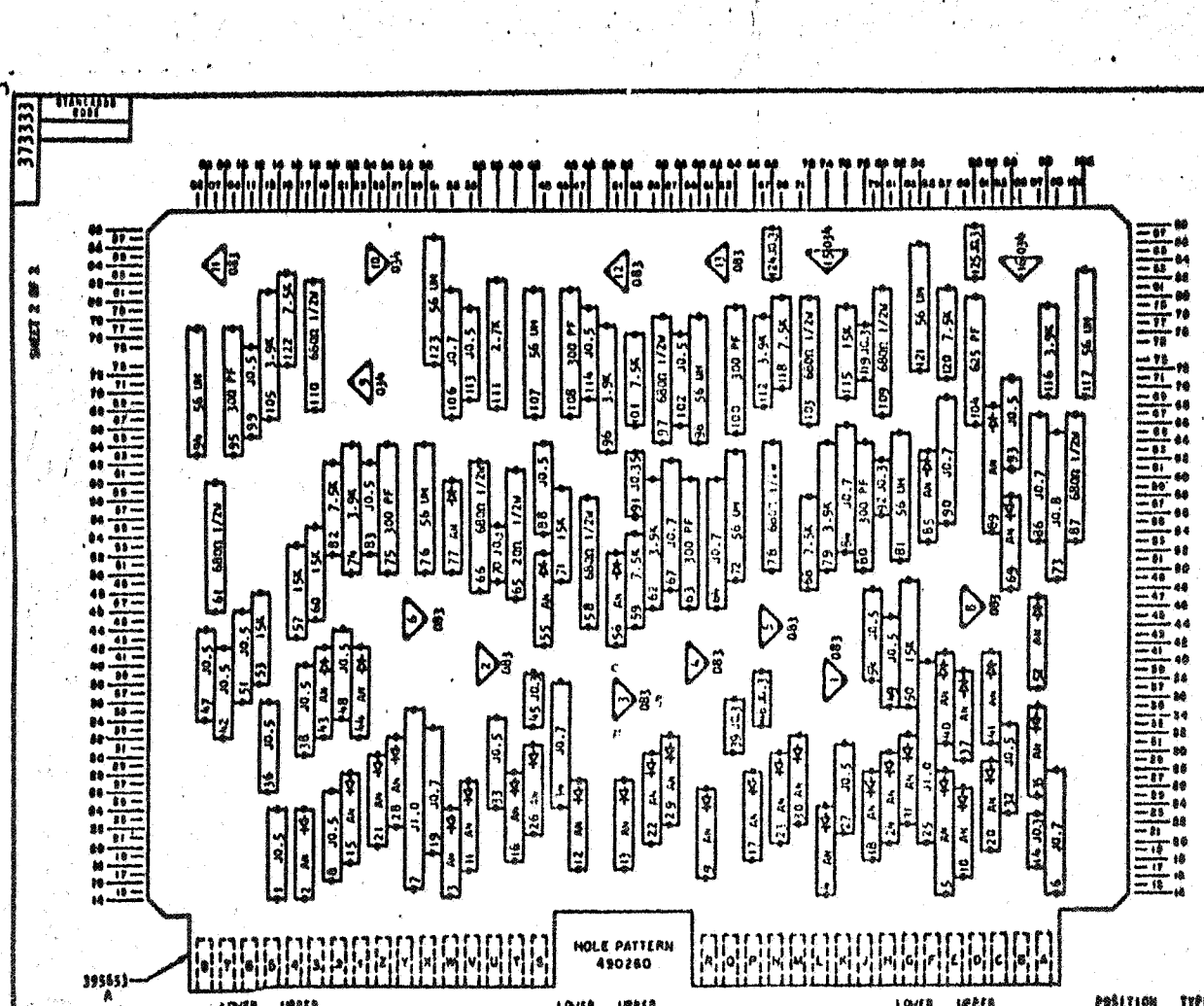
APPROVAL	CHECK	MAT. LAB.	COMP. LAB.
26.6	64		

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHARGE NO.	APPROVAL	DATE	CHARGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CAP SENSE AMPLIFIER - NO LDS				3-25-64	120123					
					26.6.64	TA 769					
DESIGN		MODEL									
DETAIL		SCALE									
CHECK		DRAW	VE	2-12-64							
APPRO		CHECK									

741800

C


373333
CARD CODE
373335
D J E -
reset
+U set
R103 680Ω 1/2W
R78 680Ω 1/2W
L81 56UH
L98 56UH
R72 3.9K
R112 3.9K
C80 300PF
C100 300PF
R50 15K
T8 P 083
T5 P 083
T13 P 083
T15 N 034
R68 7.5K
R118 7.5K
R109 630Ω 1/2W
L131 56UH
D89 AN
R57 680Ω 1/2W
R58 680Ω 1/2W
L73 56UH
L107 56UH
R62 3.9K
R96 3.9K
C63 300PF
C140 300PF
R60 15K
T4 P 083
T3 P 083
T12 P 083
T16 N 034
R87 680Ω 1/2W
L117 56UH
R120 7.5K
R116 3.9K
C104 685PF
R59 7.5K
R101 7.5K
R110 680Ω 1/2W
R81 680Ω 1/2W
L76 56UH
L96 56UH
R74 3.9K
R105 3.9K
C75 300PF
C95 300PF
R57 15K
T2 P 083
T6 P 083
T11 P 083
T10 N 034
T9 N 034
R66 680Ω 1/2W
L123 56UH
R82 7.5K
R133 7.5K
R71 15K
R111 2.7K 1/2W
R53 15K
T1 P 083
VOLTAGE
PIN
GND
-6
+6
-12
+6N
-12N
CIRCUIT AND PACKAGING STANDARD
APPROVAL
DATE
INTERNATIONAL BUSINESS MACHINES CORP.
NAME CARD ASM TSTR - FILE
OPERATION DECODE
DESIGN
DETAIL
CHECK
APPVD
MODEL SMS 1401
SCALE NONE
DRAW
CHECK
DATE
CHANGE NO.
APPROVAL
12-12-62
B116040
MBL
DEVELOPMENT NO.
X1261
C



PART NO	VALUE	QTY
216458	3.9K	7
216465	7.5K	7
216472	15K	8
317014	680n 1/2W	9
317021	2.7K 1/2W	1
334949	200 1/2W	1
350439	300 PF	6
491007	AM	36
491311	56 UH	9
492414	625 PF	1
318326	083	18
335009	034	4

POSITION	VALUE	LOWER HOLE	UPPER HOLE	POSITION	VALUE	LOWER HOLE	UPPER HOLE	POSITION	VALUE	LOWER HOLE	UPPER HOLE
1	J0.3	1414	1424	43	AM	1932	1942	85	AM	8553	8563
2	AM	1714	1724	44	AM	2332	2342	86	J0.7	9753	9763
3	AM	3314	3324	45	J0.5	4133	4139	87	680n 1/2W	10153	10163
4	AM	7414	7424	46	J0.3	6733	6739	88	J0.5	4354	4364
5	AM	8714	8728	47	J0.5	0634	0644	89	AM	9254	9268
6	J0.7	9914	9928	48	J0.5	2134	2144	90	J0.7	8755	8769
7	J1.0	2915	2935	49	J0.5	8135	8145	91	J0.35	5356	5363
8	J0.5	2016	2026	50	15K	8315	8349	92	J0.3	8056	8062
9	AM	6116	6126	51	J0.5	1036	1046	93	J0.5	9461	9471
10	AM	8916	8926	52	AM	9717	9747	94	56 UH	0563	0577
11	AM	3517	3527	53	15K	1218	1248	95	300 PF	0963	0977
12	AM	4717	4727	54	J0.5	7938	7948	96	3.9K	5063	5077
13	AM	5217	5227	55	AM	4342	4352	97	680n 1/2W	5664	5678
14	J0.3	9713	9723	56	AM	5142	5152	98	56 UH	6064	6078
15	AM	2218	2228	57	15K	1643	1653	99	J0.5	1165	1175
16	AM	4018	4028	58	680n 1/2W	4844	4858	100	300 PF	6465	6479
17	AM	6618	6628	59	7.5K	5344	5354	101	7.5K	5366	5376
18	AM	7918	7928	60	15K	1845	1855	102	J0.5	5866	5876
19	J0.7	3119	3133	61	680n 1/2W	0746	0760	103	680n 1/2W	7266	7280
20	AM	9219	9229	62	3.9K	5546	5560	104	625 PF	9066	9080
21	AM	2520	2530	63	300 PF	5946	5960	105	3.9K	1367	1381
22	AM	5520	5530	64	J0.7	6246	6260	106	J0.7	3367	3381
23	AM	6920	6930	65	200 1/2W	4047	4061	107	56 UH	4267	4281
24	AM	8120	8130	66	680n 1/2W	3648	3662	108	300 PF	4667	4681
25	J1.0	8520	8540	67	J0.7	5748	5762	109	680n 1/2W	8067	8081
26	AM	4231	4231	68	7.5K	7248	7258	110	680n 1/2W	1868	1882
27	J0.5	7631	7651	69	AM	9448	9458	111	2.7K	3868	3882
28	AM	8723	8733	70	J0.3	3849	3855	112	3.9K	6768	6778
29	AM	9723	9733	71	15K	4549	4559	113	J0.5	3569	3579
30	AM	7132	7132	72	56 UH	6449	6463	114	J0.5	4869	4879
31	AM	8322	8332	73	J0.8	9949	9965	115	15K	7669	7679
32	J0.8	9423	9439	74	3.9K	2250	2264	116	3.9K	9869	9879
33	J0.5	3824	3834	75	300 PF	2650	2664	117	56 UH	10269	10283
34	J0.7	4524	4538	76	56 UH	3050	3064	118	7.5K	6970	6980
35	AM	9725	9735	77	AM	3350	3360	119	J0.3	7871	7877
36	J0.5	1326	1336	78	680n 1/2W	6850	6864	120	7.5K	8771	8781
37	AM	8919	8919	79	3.9K	7450	7464	121	56 UH	8472	8486
38	J0.5	1730	1740	80	300 PF	7850	7864	122	7.5K	1573	1583
39	J0.3	6430	6436	81	56 UH	8251	8265	123	56 UH	3173	3187
40	AM	8731	8741	82	7.5K	2052	2062	124	J0.3	6882	6888
41	AM	9231	9241	83	J0.5	2452	2462	125	J0.3	9082	9088
42	J0.5	0832	0842	84	J0.7	7852	7866				

POSITION	TYPE	S	B	S
1	083	7436	7638	7640
2	083	3638	3840	3642
3	083	5134	5136	5138
4	083	5838	6140	5942
5	083	6742	6944	6746
6	083	2843	3045	2847
7	083	8944	9146	8948
8	034	1473	1271	1469
10	034	2482	2684	2486
11	083	0886	0684	0882
12	083	5285	5083	5281
13	083	6186	6184	6182
14	034	7286	7483	7685
15	034	8384	8582	8784

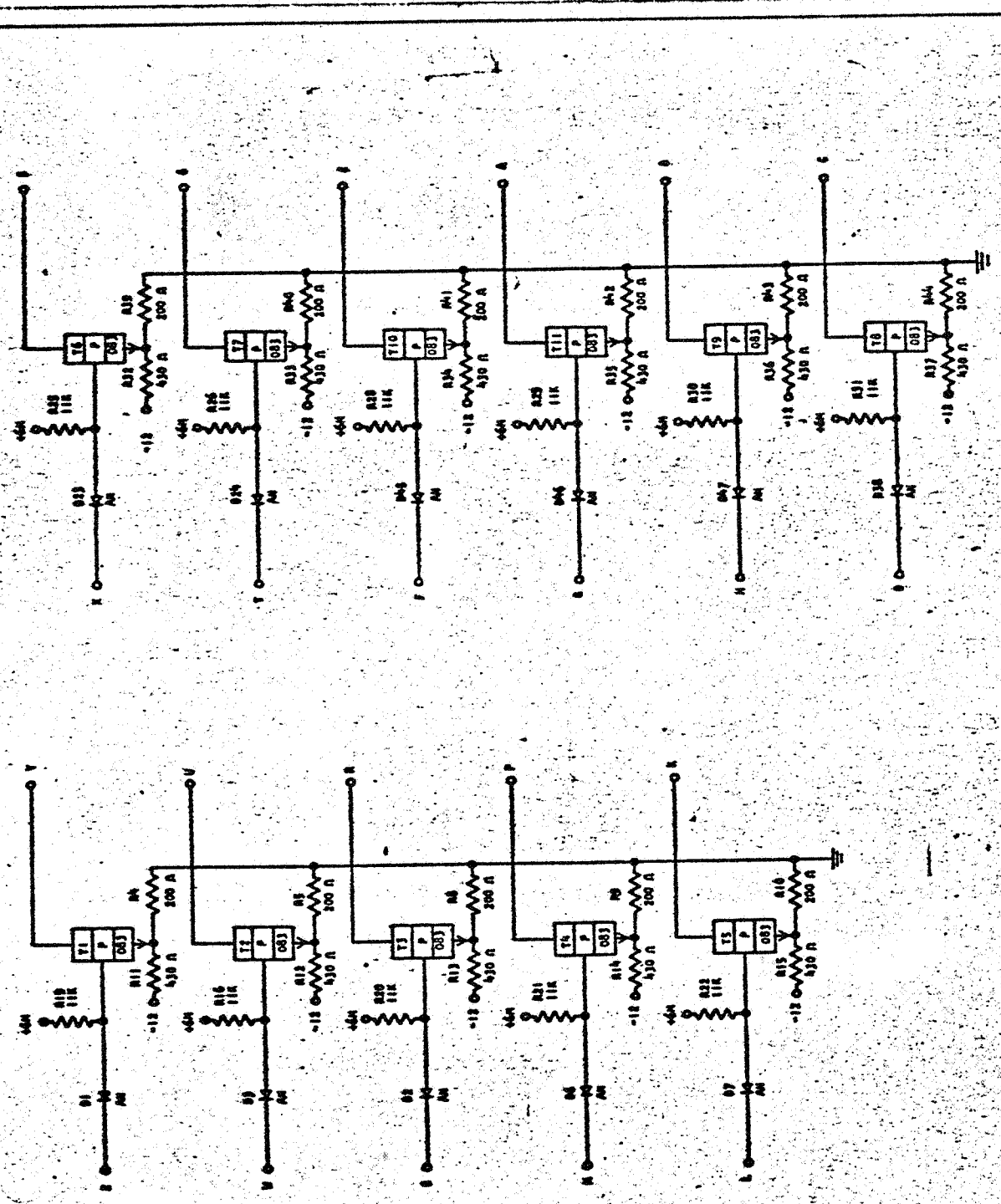
NOTES
- S CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 893157
- SS ASSEMBLE TO ENGINEERING SPECIFICATION 893001
- SSS "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296
- SSSS ALL RESISTORS ARE 1/4 W AND 95% UNLESS OTHERWISE NOTED

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
NAF	8-6-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	TWN CARD ASSEMBLY- FILE OPERATION DECODE					6-25-62	113617	MDL				X1241-1
DESIGN				MODEL	SMS 1401	8-13-62	0116040	NDL				
DETAIL				SCALE	NONE							
CHECK	E FC	7-9-62		DRAW	AJG	8-4-62						
APPRD	J.W.	7-9-62		CHECK								

373333

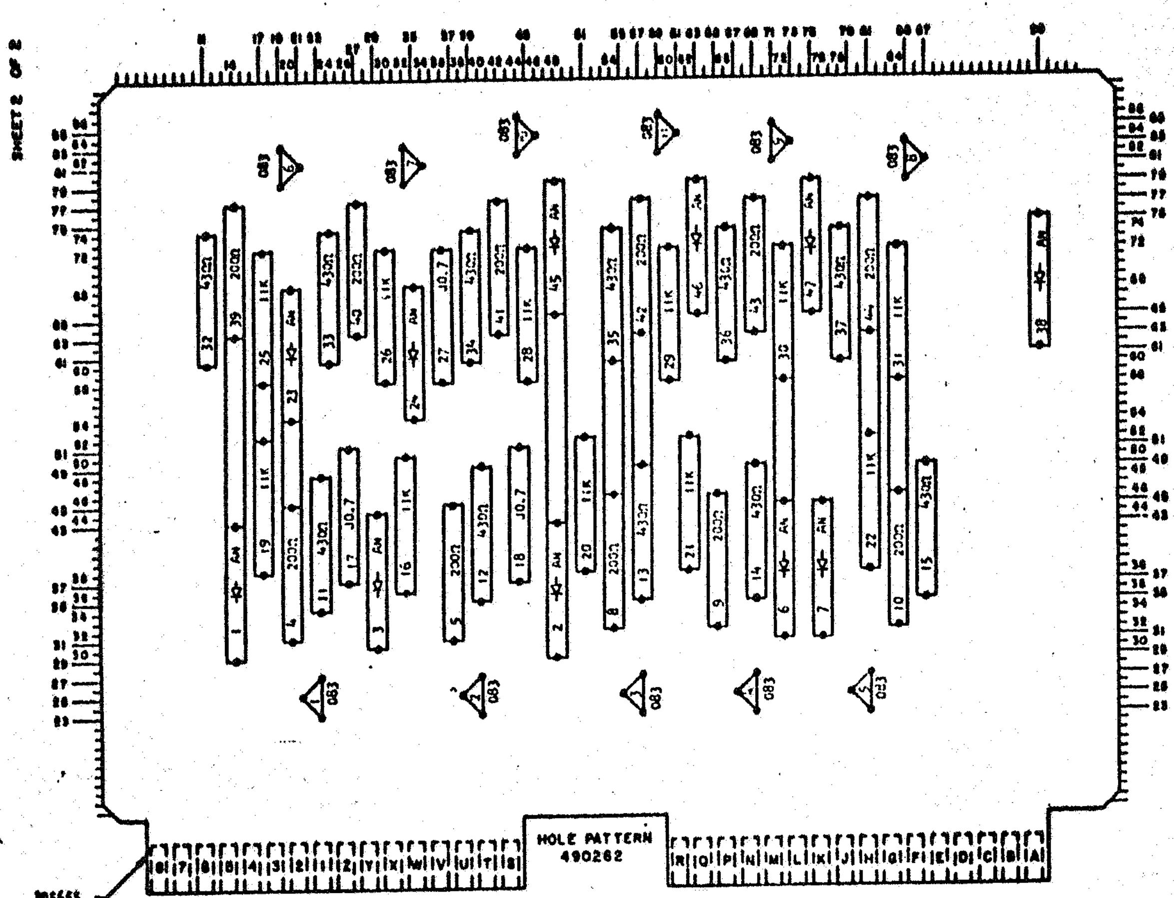
C



373335

STANDARD CODE	373335
2-7045	

CARD CODE	373335
D J F -	



PART NO	VALUE	QTY.
317006	200Ω	11
317010	430Ω	11
317027	11K	11
491007	AN	11
318325	083	11

POSITION	VALUE	LOWER HOLE	UPPER HOLE
1	AN	1429	1443
2	AN	4829	4843
3	AN	2930	2944
4	200Ω	2031	2045
5	200Ω	3731	3745
6	AN	7231	7245
7	AN	7631	7645
8	200Ω	5432	5446
9	200Ω	6532	6546
10	200Ω	8432	8446
11	430Ω	2334	2348
12	430Ω	4035	4049
13	430Ω	5735	5749
14	430Ω	6935	6949
15	430Ω	8735	8749
16	11K	3236	3250
17	J0.7	2637	2651
18	J0.7	4437	4451
19	11K	1738	1752
20	11K	5139	5152
21	11K	6238	6252
22	11K	8138	8152
23	AN	2054	2068
24	AN	3354	3368
25	11K	1758	1772
26	11K	3058	3072
27	J0.7	3658	3672
28	11K	4558	4572
29	11K	6058	6072
30	11K	7258	7272
31	11K	8458	8472
32	430Ω	1160	1174
33	430Ω	2460	2474
34	430Ω	3960	3974
35	430Ω	5460	5474
36	430Ω	6660	6674
37	430Ω	7860	7874
38	AN	9961	9975
39	200Ω	1463	1477
40	200Ω	2763	2777
41	200Ω	4263	4277
42	200Ω	5763	5777
43	200Ω	6963	6977
44	200Ω	8163	8177
45	AN	4865	4879
46	AN	6365	6379
47	AN	7565	7579

POSITION	TYPE	E	B	C
1	083	2327	2125	2323
2	083	4027	3825	4023
3	083	5727	5525	5723
4	083	6927	6725	6923
5	083	8127	7925	8123
6	083	1979	2181	1983
7	083	3279	3481	3283
8	083	8579	8781	8583
9	083	7181	7383	7185
10	083	4482	4684	4486
11	083	5982	6184	5986

NOTES

I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 893159

II ASSEMBLE TO ENGINEERING SPECIFICATION 893001

III "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296

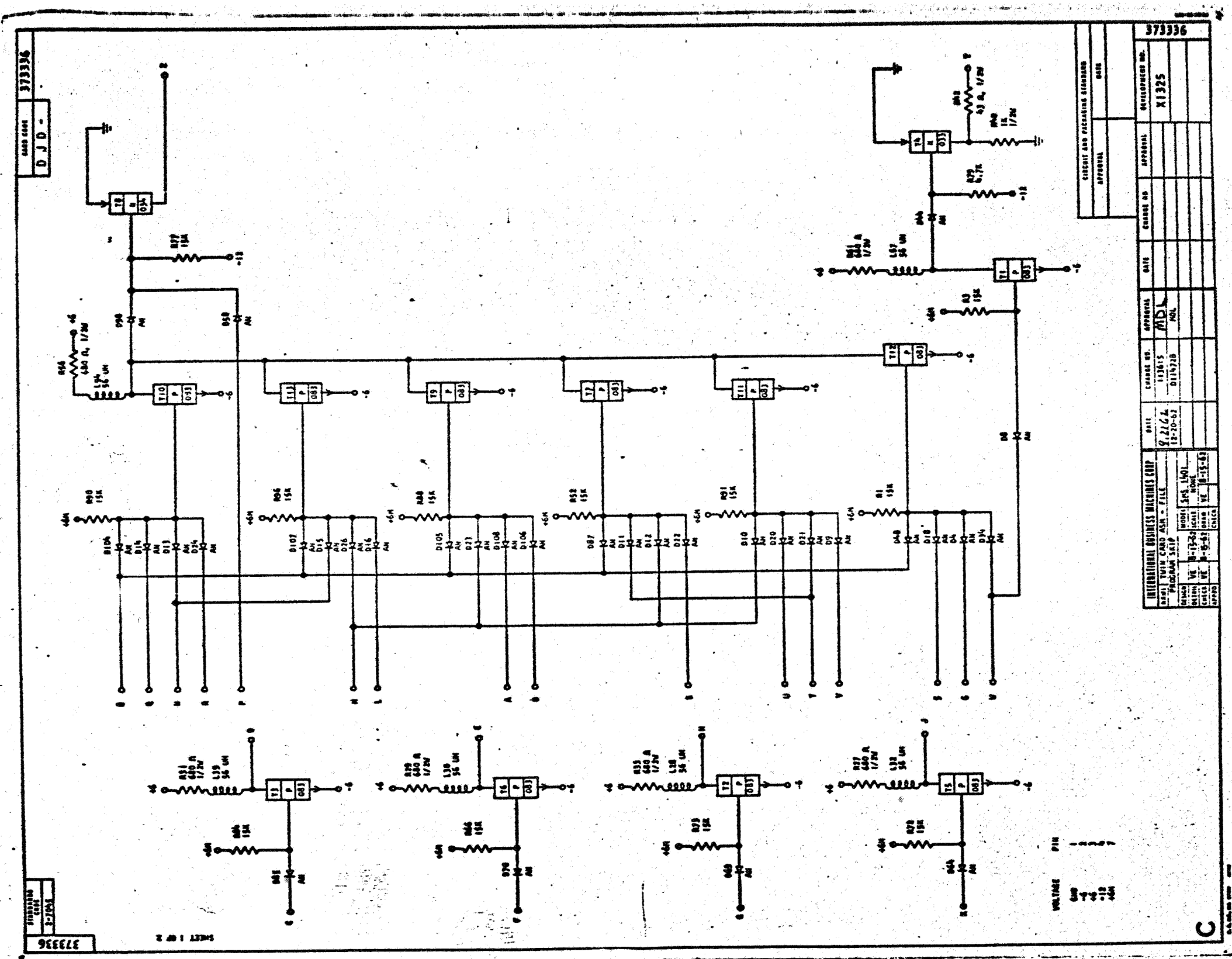
IIII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
NAF GS	8-6-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	TWIN CARD ASM- LINE DRIVERS			7-27-62	113615	MDL				X 1242
				12-20-62	0114728	NDL				
DESIGN		MODEL	SMS 1401							
DETAIL	VE 8-20-62	SCALE	NONE							
CHECK	VE 8-20-62	DRAW	VE 8-20-62							
APPRO	SWS 7-1-62	CHECK								

373335

C

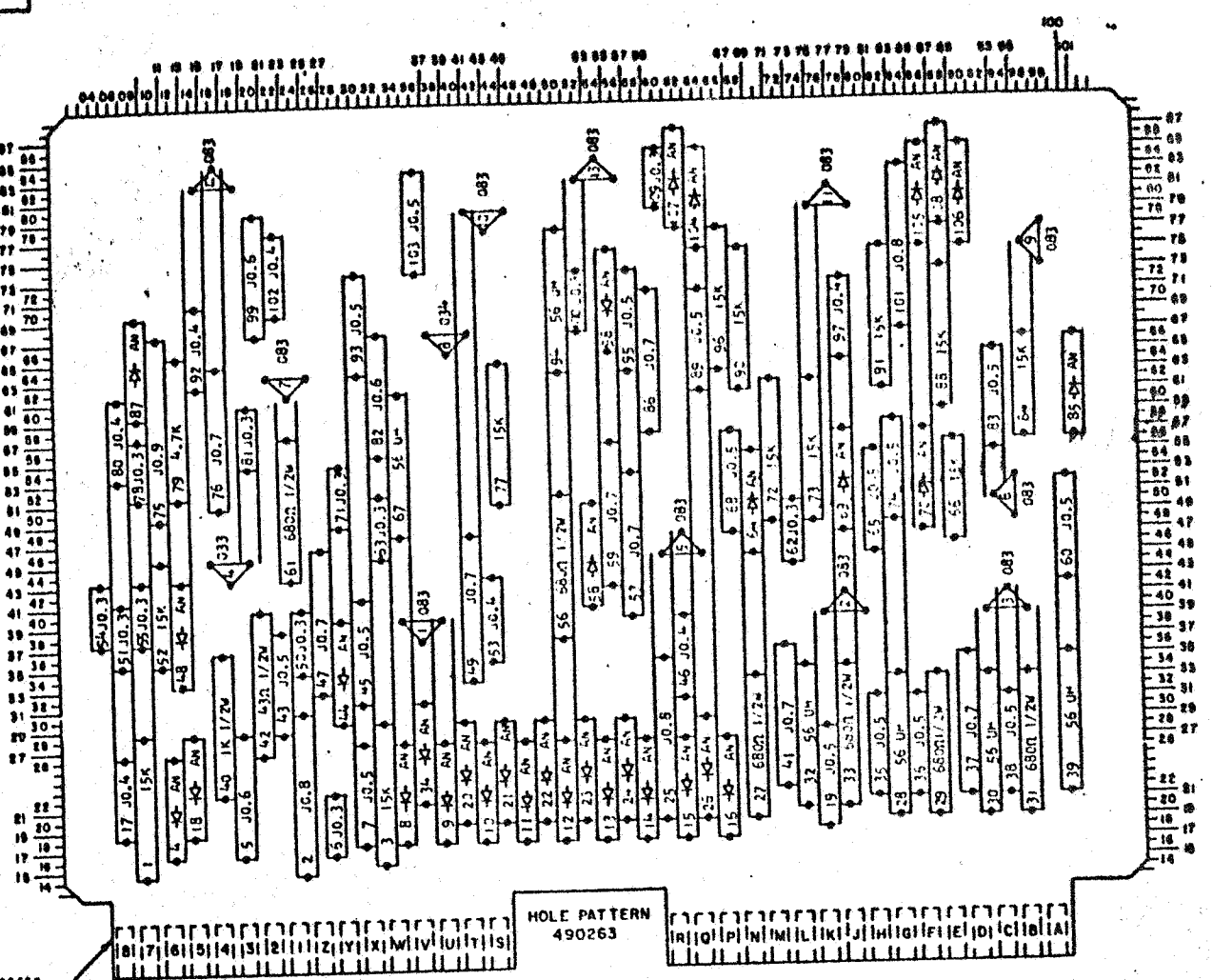

373336
DJD -
373336
INTERNATIONAL BUSINESS MACHINES CORP
373336
X1325
C

STANDARDS CODE
3-7045

dash code	373336
D J D -	

373336

SHEET 2 OF 2



PART NO	VALUE	QTY.
133359	43Ω 1/2W	1
213693	1K 1/2W	1
216460	4.7K	1
216472	15K	12
317014	680Ω 1/2W	6
491007	AN	32
491311	56 UH	6
318324	033	1
318325	083	33
535009	034	4

POSITION	VALUE	LOWER HOLE	UPPER HOLE
1	15K	0814	0828
2	J0.8	2414	2430
3	15K	3215	3229
4	AN	1116	1126
5	J0.6	1816	1828
6	J0.3	2716	2722
7	J0.5	3017	3027
8	AN	3417	3427
9	AN	3817	3827
10	AN	4217	4227
11	AN	4617	4627
12	AN	5017	5027
13	AN	5417	5427
14	AN	5817	5827
15	AN	6217	6227
16	AN	6617	6627
17	J0.4	0618	0626
18	AN	1318	1328
19	J0.5	7618	7628
20	AN	4019	4029
21	AN	4419	4429
22	AN	4819	4829
23	AN	5219	5229
24	AN	5619	5629
25	J0.8	6019	6035
26	AN	6419	6429
27	680Ω 1/2W	6919	6933
28	56 UH	8319	8333
29	680Ω 1/2W	8719	8733
30	56 UH	9219	9233
31	680Ω 1/2W	9619	9633
32	56 UH	7420	7434
33	680Ω 1/2W	7820	7834
34	AN	3621	3631
35	J0.5	8121	8131
36	J0.5	8521	8531
37	J0.7	9021	9035
38	J0.5	9421	9431
39	56 UH	10021	10035
40	1K 1/2W	1622	1636
41	J0.7	7222	7236
42	43Ω 1/2W	2026	2040
43	J0.5	2228	2238
44	AN	2829	2839
45	J0.5	3031	3041
46	J0.4	6231	6239
47	J0.7	2632	2646
48	AN	1233	1243
49	J0.7	4133	4147
50	J0.3	2434	2440
51	J0.3	0635	0641
52	15K	1035	1045
53	J0.4	4335	4343
54	J0.3	0437	0443
55	J0.3	0837	0843
56	680Ω 1/2W	5037	5051
57	J0.7	5739	5753
58	AN	5340	5350
59	J0.7	5542	5556
60	J0.5	10042	10052
61	680Ω 1/2W	2343	2357
62	J0.3	7344	7350
63	J0.3	3245	3251
64	AN	6945	6955
65	J0.5	8145	8155
66	15K	8946	8956
67	56 UH	3447	3461
68	J0.5	6747	6757
69	AN	7847	7857
70	AN	8647	8657
71	J0.3	2848	2854
72	15K	7148	7162
73	15K	7548	7562
74	J0.5	8348	8358
75	J0.9	1049	1067
76	J0.7	1650	1664
77	15K	4450	4464
78	J0.3	0851	0857
79	4.7K	1251	1265
80	J0.4	0653	0661
81	J0.3	1954	1960
82	J0.6	3255	3267
83	J0.5	9355	9365
84	15K	9656	9666
85	AN	10156	10166
86	J0.7	5957	5971
87	AN	0859	0869
88	15K	8859	8873
89	J0.5	6461	6471
90	15K	6861	6875
91	15K	8261	8275
92	J0.4	1462	1470
93	J0.5	3063	3073
94	56 UH	5063	5077
95	J0.5	5763	5773
96	15K	6663	6677
97	J0.4	7864	7872
98	AN	5565	5575
99	J0.6	2067	2079
100	J0.3	5267	5273
101	J0.8	8467	8483
102	J0.4	2269	2277
103	J0.5	3673	3683
104	AN	6475	6485
105	AN	8675	8685
106	AN	9075	9085
107	AN	6277	6287
108	AN	8877	8887
109	J0.3	6079	6085

POSITION	TYPE	E	B	C
1	083	3439	3637	3839
2	083	8039	7841	7639
3	083	9639	9441	9239
4	033	1545	1743	1945
5	083	6445	6247	6045
6	083	9552	9350	9548
7	083	2163	2361	2563
8	034	3767	3965	4167
9	083	9877	9675	9873
10	083	4179	4377	4579
11	083	7979	7781	7579
12	083	1882	1684	1482
13	083	5682	5484	5282

NOTES

I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 893160

II ASSEMBLE TO ENGINEERING SPECIFICATION 893001

III "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296

IIII ALL RESISTORS ARE 1/4 WATT AND 5% UNLESS OTHERWISE NOTED

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
NAF G3	9-6-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	373336
NAME	TWIN CARD ASM- FILE PROGRAM					9.21.62	113615	JDL				X 1325	
	SKIP					12-20-62	0114728	RBL					
DESIGN				MODEL	SMS 1401								
DETAIL	VE	8-20-62		SCALE	NONE								
CHECK	VE	8-20-62		DRAW	VE 8-20-62								
APPRO	-11			CHECK									

C